2019S2 - HW Syn. Lab
Skill Test

Set 1

No. _____

Name: _____Student ID: _____

(**Synthesis Skill**: 20 points, *divided into 12.5% of the total score*)

You have been given 40 minutes in order to create a counter using 7-segment display with two display modes.

Default 7-segment display behavior on BASYS3 is a display showing four numbers starts from 0 to 9 then go back to 0 again. Each digit shown also has dot beside it.

For this task, you are going to create 7-segment display showing three numbers in hexadecimal, starts from A (10 in decimal), then change to C (12 in decimal), and then E (14 in decimal). After the counter reaches E, the counter must go back to A again. The interval between each state should be about 0.3s (about 2^{25} times slower than board clock speed). Also, dots after digits should **not** be shown.

Beside the counter, while SW0 is enabled, the counter should show only one digit at a time, while also changing number on it. The position of digit should be move from left to right every about 0.3s. And after we turn off SW0, the counter should show 4 same numbers, repeating its cycle again.

P.S. You don't have to debounce the switch in order to get perfect score in this task.

Group (circle 1) A B C D

Description	**Time**	**Score**
Clock Divider for 7-segment Display (8%) *(1-point deduction on showing dots)* *You may obtain score on this section by displaying 8 on four seven-segment displays*		
4-Digits Counter (5%) *You may obtain 2.5% on this section by completing transition between any two states*		
Clock Divider for State Transition Delaying (5%)		
1-Digit Alternating Counter (2%)		

Grader: _____ (name/signature)

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Set 2

No. _____

Name: _____Student ID: _____

(**Synthesis Skill**: 20 points, *divided into 12.5% of the total score*)

You have been given 40 minutes in order to create a loading spinner using 7-segment display with two display modes.

You may have seen loading spinner which widely used in GUI. Now you are going to create it on your FPGA board. Four 7-segment displays should show the same spinner. The expected state of the spinner is shown in Figure 1 (from left to right). After the spinner reach last states, the spinner should go back to the first state and repeat the same transition again. The interval between each state should be about 0.1s (about 2^{24} times slower than board clock speed). Also, dots after digits should **not** be shown. If BTNL was pressed, please hide all the loading spinner and show it again after the button released.

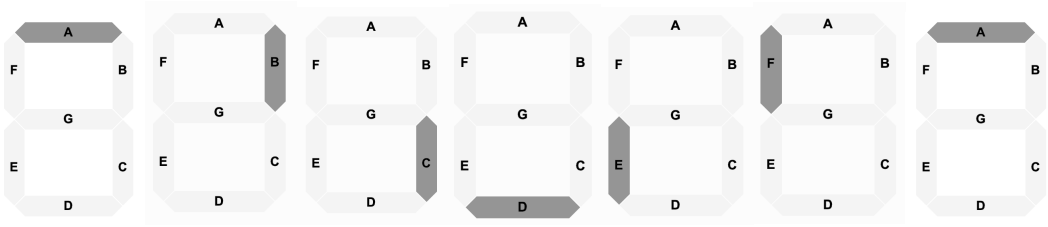

Figure 1: *6 states of loading spinner*

Group (circle 1) A B C D

Description	**Time**	**Score**
Clock Divider for 7-segment Display (8%) *(1-point deduction on showing dots)* *You may obtain score on this section by displaying 8 on four seven-segment displays*		
4-Digits Loading Spinner (5%) *You may obtain 2.5% on this section by completing transition between any two states*		
Clock Divider for State Transition Delaying (5%)		
Spinner Hide Button (2%)		

Grader: _____ (name/signature)

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Set 3

No. _____

Name: _____Student ID: _____

(**Synthesis Skill**: 20 points, *divided into 12.5% of the total score*)

You have been given 40 minutes in order to create a stick counter using 7-segment display with two display modes.

For this task, you are going to make eights states stick counter using 7-segment displays. The counter should show zero stick, one stick, two sticks, three sticks, and four sticks sequentially (The example of stick counter is shown in Figure 1). After the counter reach last states, the counter should stop at eight sticks. The interval between each state should be about 0.6s (about 2^{26} times slower than board clock speed).

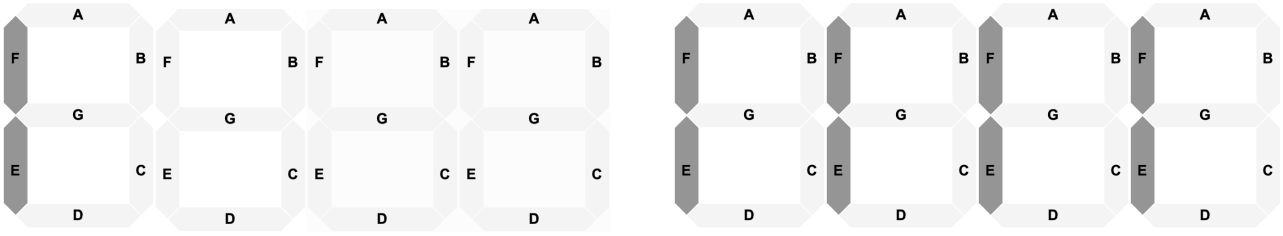

Figure 1: *Stick counter with one stick (left) and counter with four sticks (right)*

And while BTNC is pressed, please reset the counter to zero stick and continue counting with interval between each state of 1.2s instead of 0.6s after the button is released.

Group (circle 1) A B C D

Description	**Time**	**Score**
Clock Divider for 7-segment Display (8%) *(1-point deduction on showing dots)* *You may obtain score on this section by displaying 1 on four seven-segment displays*		
Clock Divider for State Transition Delaying (5%)		
4-States Counter (5%) *You may obtain 2.5% on this section by completing transition between any two states*		
Counter Reset & Interval Change Button (2%)		

Grader: _____ (name/signature)

2019S2 - HW Syn. Lab
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Set 4

No. _____

Name: _____Student ID: _____

(**Synthesis Skill**: 20 points, *divided into 12.5% of the total score*)

You have been given 40 minutes in order to create a shift number counter using 7-segment display with two display modes

The shift number counter you are going to make is a counter which start with 1234 on 7-segment display, then it will change to 2345, 3456, …, 6789, 8910, 1011, 1112, and end with 1920. The interval between each state should be about 0.6s (about 2^{26} times slower than board clock speed). Also, dots after digits should **not** be shown. And while BTND is pressed, your counter change period should be 1.2s instead of 0.6s.

Group (circle 1) 1A 1B 2A 2B

Description	**Time**	**Score**
Clock Divider for 7-segment Display (8%) *(1 point penalty for showing dots)*		
Clock Divider for State Transition Delaying (5%)		
4-Digits Shift Counter (5%) *You may obtain 2.5% on this section by completing transition between any two states*		
Interval Increase Button (2%)		

Grader: _____ (name/signature)