3 months run CT verification (ECC/ECM).

4 months learning ECM/ECC

Create document + learning

CT for BUS module

Synthesis

• Create detailed design specifications based on architecture and micro-architecture specifications.

• Design RTL and coding for high-speed design

• Develop RTL Linting and CDC scripts, evaluation of results, and corrective actions.

• Support silicon bring-up and silicon validation.

What you’ll bring

• Minimum 2+ years of digital SoC logic design experience

• Knowledge of SOC architecture, microarchitecture, logic and RTL design concepts

• Experience with SoC AMBA bus architectures such as CHI, AXI, AHB, APB and advanced

connectivity implementations such as Network-on-Chip (NoC)

• Good in System Verilog RTL design, design for bandwidth and latency optimization

• Good in scripting languages (PERL, Python, shell, etc.)

• RTL & gate simulation experience and good debugging skills

• Experience with Lint and CDC tools and flows

• Experience with synthesis and STA flows

• Good English communications skills and ability to communicate technical concepts clearly and

work collaboratively in a team to get things done in a fast-paced environment.