Indian Institute of Technology, Delhi

FALL, 2013

CSL 211: COMPUTER ARCHITECTURE

Remajor

Two Hours

NOTE:
- All answers need to be brief and to the point.
- Please make any assumptions that you deem to be reasonable.
- We need exquisite detail, and clarity in every answer.
- You need to write your answer in the answer box (Ans:). We will **NOT GRADE** your answer, if it is not written in the box.
- Every answer needs to be written neatly and cleanly in the space provided for it.
- Use proper handwriting, and do not write anything in the margins.
- Note that in most questions, there is no part marking.
- You can use rough sheets. Do not attach them with this paper.
- You are not allowed to carry any electronic gadget including calculators.
- This question paper **NEEDS TO BE SUBMITTED**. Do not take it with you.

Total Marks: 100
Total Number of Pages : 3
Pass Marks: 40

1. Answer the following questions: (10 marks)

i Define coherence.

ii Define memory consistency.

iii What is the basic difference between coherence and consistency.

2. Consider a fully associative cache following the LRU replacement scheme and consisting of only 8 words. Consider the following sequence of memory accesses (the numbers denote the word address):
20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 22, 30, 21, 23, 31

Assume that we begin when the cache is empty. What are the contents of the cache after the end of the sequence of memory accesses. (10 marks)

3. Consider a two-level cache using a write back policy. The L1 cache can store 2 words, and the L2 cache can store 4 words. Assume the caches to be fully associative and following the LRU replacement scheme. Consider the following sequence of memory accesses. The format of a write access is *write* <*address*> <*value*>, and the format for a read access is *read* <*address*> . (10 marks)

```
write 20 200
write 21 300
write 22 400
write 23 500
write 20 201
write 21 301
read 22
read 23
write 22 401
write 23 501
```

What are the contents of the caches at the end of the sequence of memory accesses? What are the contents of the caches, if we assume a write through policy ?

4. Consider a direct mapped cache with 16 cache lines, indexed 0 to 15, where each cache line can contain 32 integers (block size : 128 bytes).

Consider a two-dimensional, 32×32 array of integers a. This array is laid out in memory so that $a[0,0]$ is next to $a[0,1]$, and so on. Assume the cache is initially empty, but that $a[0,0]$ maps to the first word of cache line 0. (10 marks)

Consider the following *column-first* traversal:

```
int sum = 0;
for (int i = 0; i < 32; i++) {
    for( int j=0; j < 32; j++) {
          sum += a[i,j];
    }
}
```

and the following *row-first* traversal:

```
int sum = 0;
for (int i = 0; i < 32; i++) {
    for( int j=0; j < 32; j++) {
         sum += a[j,i];
    }
}
```

Compare the number of cache misses produced by the two traversals, assuming the oldest cache line is evicted first. Assume that i, j, and *sum* are stored in registers. Assume that no part of array, a, is saved in registers. It is always stored in the cache.

5. Is the outcome (t1,t2) = (2,1) allowed in a system with coherent memory? Explain your answer in detail. (10 marks)

Thread 1:

```
x = 1;
x = 2;
```

Thread 2:

```
t1 = x;
t2 = x;
```

6. Is the outcome (t1 = 0) allowed in a system with coherent memory with atomic writes? Consider both sequential and weak consistency? Explain your answer in detail. (10 marks)

Thread 1:	Thread 2:	Thread 3:
`x = 1;`	`while(x != 1) {}` `y = 1;`	`while (y != 1) {}` `t1 = x;`

7. Assume that two nodes desire to transition from the S state to the M state at exactly the same point of time. How will the snoopy protocol ensure that only one of these nodes enters the M state, and finishes its write operation? What happens to the other node? (10 marks)

8. Assume that we are transmitting the bit sequence: 01101110001101. Show the voltage on the bus as a function of time for the following protocols: RZ, NRZ, Manchester, NRZI. (10 marks)

9. What are the basic differences between NAND and NOR flash? (10 marks)

10. Explain *wear levelling*, and *read disturbance*? How are these issues typically handled in modern Flash devices? (10 marks)
