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COL216 Computer Architecture Quiz 2 (Set A) 16.03.2017

Q 1. While carrying out a multi-cycle design for ARM processor, it is required to figure out how various instructions will be broken up into cycles. Show how will you break up the instructions given below into cycles, considering the following datapath constraints - (a) the register file has only 2 read ports and 1 write port, (b) the ALU is used to do all arithmetic and logical operations as well as address calculations (there are no separate adders), (c) multiplication and shifting/rotation cannot be done in the same cycle in which ALU is being used. Assume that PC is a separate register, rather than R15.

LDREQ Rd, [Rn, - Rm, LSL #2] ! {Load if equal, with auto (pre) decrement}
ANDS Rd, Rn, Rm, LSR Rs {Perform bit-wise AND and set flags}
MUL Rd, Rm, Rs {Multiply Rd = Rm * Rs}

3 I D E

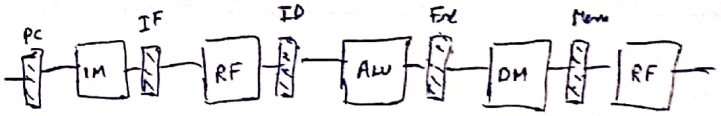
① update PC & fetch instruction → Load Rm, Rm → Shift Rm → Calculate Ad = Rn - Rm×4 → Store Ad to Rm in RF → fetch from memory → Store in RF at Rd

② update PC & fetch ins → Load Rm, Rm → Load Rs → Shift (Rm) → ALU → write to RF & set flags (Re value of Rd)

P.T.O

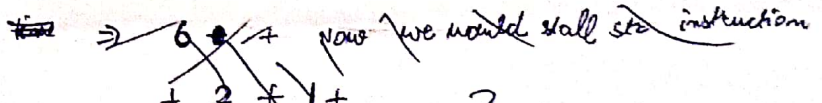
Q 2. Consider a classical 5-stage pipeline to implement ARM instructions DP, DT and B. For DP instructions, no shift/rotate is allowed. For DT instructions, offset is always 0. Writing into Register file takes place at the end of a clock cycle. When a branch instruction is detected, any instructions entered in pipeline after the branch instructions are flushed. When the branch completes the 3rd stage, its correct successor is fetched. Find the number of clock cycles required to execute the code below in two cases - (a) there are no data forwarding paths and (b) all possible data forwarding paths are there. Show how you obtain your answer. Assume that the loop executes 10 times.

Loop: ① LDR R4, [R1]
② LDR R5, [R2]
③ ADD R4, R4, R5
④ STR R4, [R1]
5 ADD R1, R1, #4
6 ADD R2, R2, #4
7 CMP R1, R6
8 BLT Loop



a) Handling Hazards by stalling

Clock cycles ⇒ We have to stall add R4, R4, R5 at IF stage bcz of its dependence on previous ldr instruction



Delay = 3 + 3 + 2 + 3 = 11

Total time = 11 + 12 = 23 × 10 = 230 cycles

b) Add instruction (line 3) would be stalled for one clock cycle. & 3 cycles are used for flushing instruction after branch. One loop thus takes = 12 + 1 + 3 = 16.
Total clock cycle = 160