Indian Institute of Technology, Delhi

FALL, 2011

CSL 211: COMPUTER ARCHITECTURE

Major Exam

Time: Two Hours

NOTE: – All answers need to be brief and to the point.

– No questions will be answered. Make any reasonable assumptions.

Total Marks: 50
Total Number of Pages : 3

Definitions

Bisection Bandwidth The minimum number of links that need to be cut to divide a network into two equal halves. Here equality is in terms of the number of nodes.

Diameter The largest shortest path between any two nodes in the network.

Easy

1. (10 marks)

(a) What is Amdahl's law?

(b) Why don't you have an instruction – Arithmetic Shift Left?

(c) What is the purpose of the *lr* register?

(d) Which instruction set has better instruction cache performance? ARM or X86, and why?

(e) Why is a TLB required?

2. We have a hard disk with the following parameters: (5 marks)

Seek Time	50 ms
Rotational Speed	600 RPM
Bandwidth	100 MB/s

How long will it take to read 25 MB on an average.

Medium

3. (10 marks)

(a) What is the diameter of a ring containing n nodes? Give a precise answer that holds for even and odd n.

(b) What is the advantage of RAID?

(c) In the snoopy protocol, why do you write back data to the main memory upon a $M \rightarrow S$ transition?

(d) What is the difference between a SMT and a hyper-threaded machine?

(e) What is the difference between a fine grained and coarse grained multi-threaded machine?

4. A machine has a 32-bit virtual address space and a 16KB page size. It has 1GB of physical memory. (Total: 5 marks)

(a) What is the maximum number of pages that a process can have? Your answer should be in the format "2^x". (2 marks)

(b) Assume a two level page table that splits the number of page id bits into two equal parts between the primary and secondary page tables. Further assume that we require 8 secondary page tables. Calculate the size of the entire page table in bits. You can assume that all the secondary page tables are full, and it takes 1 bit to store a null pointer in the primary page table. (3 marks)

5. We have a $MESI$ protocol with the following specifications. The E state refers to the "exclusive" state, in which a processor is sure that no other cache contains the block in a valid state. Secondly, in the E state, the processor hasn't modified the block yet. (Total: 5 marks)

(a) What is the advantage of having the E state? (2 marks)

(b) How are evictions handled in the E state? (3 marks)

You don't have to draw any state diagrams, or explain the MSI protocol.

Hard

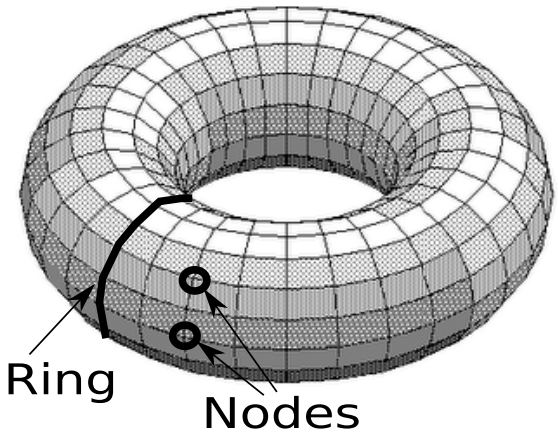

Figure 1: Tube Network

6. Figure 1 shows a tube network. It consists of a set of n rings, each consisting of m nodes. Each node in a ring is connected to two adjacent nodes in the same ring, and to two other corresponding nodes in adjacent rings (see the Figure). (Total: 7 marks)

(a) What is the bisection bandwidth of this network, and why? (3 marks)

(b) What is the diameter, and why? (4 marks)

Please give a precise and compact answer that holds for both the even and odd cases, along with a brief yet rigorous proof.

7. Assume that you are given a machine with an unknown configuration. You need to find out a host of cache parameters by measuring the time it takes to execute different programs. These programs will be tailor made in such a way that they will reveal something about the underlying system. For answering the set of questions, you need to broadly describe the approach. (Total: 8 marks)

(a) How will you estimate the size of the L1 cache? (2 marks)

(b) How will you estimate the L1 block size? (2 marks)

(c) How will you estimate the L1 cache associativity? (4 marks)
