Indian Institute of Technology, Ropar

FALL, 2011

CSL 211: COMPUTER ARCHITECTURE

Midterm Exam

Time: One and Half Hours

NOTE:

- All answers need to be brief and to the point.
- Whenever we ask you to write ARM code, write the basic functionality.
  - ∗ You need not write ldmfd and stmfd instructions. E.g. An ARM program to perform an add is: ADD R3, R1, R2
- No questions will be answered. Make any reasonable assumptions.

Total Marks: 50
Total Number of Pages : 2

[NO PART MARKING in QUESTIONS 1, 2, 3 and 5]

1 Easy

1. What is the range of positive and negative denormalized numbers? (5 marks)

2. Very briefly answer the following(1-2 lines): (10 marks)

(a) If machine A runs at 5 Ghz, and machine B runs at 4 GHz. Can we say that machine A is faster than machine B?

(b) What is Moore's Law?

(c) The power dissipated by a processor is proportional to a function of three variables. What is the relationship?

(d) What is the structure of the CPSR in ARM?

(e) What do ldmfd an stmfd instructions do?

3. If I increase the average CPI (Cycles per Instruction) by 5%, decrease the instruction count by 20% and double the clock rate, what speedup should I expect, if any, and why? (5 marks)

2 Medium

4. You are given a 32 bit binary number in register $R1$. You want to check if the number is a *palindrome*. This means that the number is the same if it is read forwards or backwards. For example, the 4-bit sequence, 1001 is a palindrome. The 8 bit sequence 11011011 is a palindrome. You need to save 0 in $R7$ if the value is not a palindrome, and 1 if it is. Try to reduce the number of ARM instructions. (7 marks)

5. Very briefly answer the following:(1-2 lines) (8 marks)

(a) Given the ratio of execution times of n tasks on your processor and a reference processor, will you summarize the speed of your processor by the Arithmetic Mean, Harmonic Mean, or Geometric Mean of these ratios ?

(b) Why can't we use DRAMs for register files?

(c) Given two unsigned numbers, A and B, how do we compute if A is greater than B using four or less than four instructions in ARM?

(d) How many transistors are there in a SRAM cell, and what is pre-charging?

3 Hard

[Hint :]

$$(ab)(mod\,n) = ((a\,mod\,n) \times b)mod\,n = ((a\,mod\,n) \times (b\,mod\,n))mod\,n$$
$$(a+b)mod\,n = ((a\,mod\,n) + (b\,mod\,n))mod\,n$$

6. Given an arbitrarily long unsigned binary number, n, find the remainder if you divide it by 7 (not the quotient) using an $O(log(n))$ time algorithm. Just write the algorithm, don't write any ARM code. (5 marks)

7. A 32 bit value is saved in register, $R1$. A 32 bit value is a sequence of 4 bytes, where each byte represents an unsigned number. Write ARM code to find the largest byte (unsigned), in this sequence of 4 bytes, and save it in $R7$. For example, if the 32 bit value in $R1$ is [0x32 A9 E0 99], you need to save $0xE0$ in $R7$. (5 marks)

4 Research

8. How frequently does the carry propagate to the end for most numbers? Answer: Very infrequently. In most cases, the carry does not propagate beyond a couple of bits. Chen and Liu [1] were the first to observe that we can design an approximately correct adder. The observation was that a carry does not propagate by more than k positions most of the time. Formally, we have:
Assumption 1: While adding two numbers, the largest length of a chain of propagates is at most k.

In this case a propagate function for adding two bits a and b is defined as (a XOR b) (Propagate does not include generate). Design an optimal adder(circuit 1) in this case that has time complexity $O(log\,k)$ assuming that Assumption 1 holds all the time. Now design a circuit(circuit 2) to check if assumption 1 has ever been violated. Verma et. al.[2] proved that k is equal to $\theta(log(n))$ with very high probability. Voila, we have an exactly correct adder by fusing circuit 1, 2, and a minimal amount of extra logic, which runs most of the time in $O(log(log(n)))$ time.!!! (5 marks)

[1] Performance Improvement with Circuit Level Speculation, Tong Liu and Shen Lu, International Symposium on Micro-Architecture, 2000.

[2] Variable Latency Speculative Adder: A New Paradigm for Arithmetic Circuit Design, Ajay Verma, Philip Brisk, Paolo Ienne, Design Automation and Test in Europe, 2008.