XDC (Xilinx Design Constraints) file for the Digital Clock Project.

This template is optimized for the Digilent Basys 3 board (Artix-7 FPGA).

If you are using a different board, you must update the PACKAGE_PIN values.

Clock Signal

set_property PACKAGE_PIN W5 [get_ports clk] set_property IOSTANDARD LVCMOS33 [get_ports clk] # Define the clock period for the tool (10ns for 100MHz) create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]

7 Segment Display Cathodes (seg[6:0] map to gfedcba)

set_property PACKAGE_PIN W7 [get_ports {seg[0]}] # A set_property IOSTANDARD LVCMOS33 [get_ports {seg[0]}] set_property PACKAGE_PIN W6 [get_ports {seg[1]}] # B set_property IOSTANDARD LVCMOS33 [get_ports {seg[1]}] set_property PACKAGE_PIN U8 [get_ports {seg[2]}] # C set_property IOSTANDARD LVCMOS33 [get_ports {seg[2]}] set_property PACKAGE_PIN V8 [get_ports {seg[3]}] # D set_property IOSTANDARD LVCMOS33 [get_ports {seg[3]}] set_property PACKAGE_PIN U5 [get_ports {seg[4]}] # E set_property IOSTANDARD LVCMOS33 [get_ports {seg[4]}] set_property PACKAGE_PIN V5 [get_ports {seg[5]}] # F set_property IOSTANDARD LVCMOS33 [get_ports {seg[5]}] set_property PACKAGE_PIN U7 [get_ports {seg[6]}] # G set_property IOSTANDARD LVCMOS33 [get_ports {seg[6]}]

7 Segment Display Anodes (an[3:0] map to D3 D2 D1 D0)

set_property PACKAGE_PIN U2 [get_ports {an[0]}] # D0 (Minutes Ones) set_property IOSTANDARD LVCMOS33 [get_ports {an[0]}] set_property PACKAGE_PIN U4 [get_ports {an[1]}] # D1 (Minutes Tens) set_property IOSTANDARD LVCMOS33 [get_ports {an[1]}]

set_property PACKAGE_PIN V4 [get_ports {an[2]}] # D2 (Hours Ones) set_property IOSTANDARD LVCMOS33 [get_ports {an[2]}] set_property PACKAGE_PIN W4 [get_ports {an[3]}] # D3 (Hours Tens) set_property IOSTANDARD LVCMOS33 [get_ports {an[3]}]

Push Buttons (Mapping to BTN[U], BTN[C], BTN[L] on Basys3)

set_property PACKAGE_PIN T18 [get_ports btn_h] # BTN U (Increment Hour) set_property IOSTANDARD LVCMOS33 [get_ports btn_h] set_property PACKAGE_PIN W19 [get_ports btn_m] # BTN C (Increment Minute) set_property IOSTANDARD LVCMOS33 [get_ports btn_m] set_property PACKAGE_PIN T17 [get_ports rst] # BTN R (Reset) set_property IOSTANDARD LVCMOS33 [get_ports rst]