



Computer Architecture   
ASSIGNMENT

**Assignment Topic:** Cache Replacement Policy Optimization in Industrial Systems

**Section:** 64-B

**Submitted To**

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## Introduction

In modern computer architecture, cache memory plays a critical role in bridging the speed gap between the processor and main memory. Efficient cache utilization is essential to achieving high system performance, as cache misses can significantly increase latency and reduce throughput. One of the key factors affecting cache performance is the **cache replacement policy,** which determines which data to evict when the cache is full.

Common replacement strategies include **First-In-First-Out (FIFO), Least Recently Used (LRU),** and **Least Frequently Used (LFU),** each with distinct advantages and trade-offs depending on workload characteristics. Selecting an appropriate policy is crucial in industrial systems, especially in high-load environments such as enterprise servers, real-time systems, and embedded applications, where inefficient cache management can lead to bottlenecks and performance degradation.

The objective of this assignment is to **evaluate various cache replacement policies** using trace-driven simulations, measure their impact on cache miss rates and overall performance, and propose strategies to optimize cache behavior for real-world workloads. By analyzing these policies in an industrial context, we aim to provide recommendations for improving system efficiency and responsiveness.

## 2. Background Study

#### **1. Cache Memory in Modern Systems**

Cache memory is a small, high-speed memory located close to the CPU that stores frequently accessed data to reduce access latency to the main memory. Modern processors use multi-level caches (L1, L2, L3) to exploit **temporal locality** (recently accessed data is likely to be accessed again) and **spatial locality** (data near recently accessed addresses is likely to be accessed soon). Efficient cache management is critical to minimizing cache misses, which directly impact system performance and throughput.

#### **2. Cache Replacement Policies**

When a cache is full, a **replacement policy** decides which data block to evict. Common policies include:

* **First-In-First-Out (FIFO):** Evicts the oldest data in the cache. Simple to implement but may evict frequently used data.
* **Least Recently Used (LRU):** Evicts the block that has not been used for the longest time. Performs well for workloads with temporal locality but requires tracking access history.
* **Least Frequently Used (LFU):** Evicts the block with the lowest access frequency. Useful for workloads with frequently reused data but requires counters and aging mechanisms to prevent stale data retention.

Hybrid or adaptive policies such as **LRU-K, Adaptive Replacement Cache (ARC),** and **CLOCK-Pro** have been proposed to combine the strengths of multiple strategies and dynamically adapt to changing workloads.

#### **3. Simulation and Performance Metrics**

Cache replacement policies are often evaluated using **trace-driven simulations**, which replay memory access sequences from real workloads. Key metrics include:

* **Cache Miss Rate:** Percentage of memory accesses not found in the cache.
* **Hit Time:** Time taken to access data in the cache.
* **Overall System Throughput:** Effect of cache performance on program execution.

#### **4. Literature Review**

* Smith (1982) introduced fundamental cache concepts and highlighted the importance of replacement policies in minimizing miss rates.
* Jiang and Zhang (2002) proposed the **LRU-K algorithm**, showing superior performance over traditional LRU in workloads with irregular access patterns.
* Industry reports by Intel and AMD emphasize that modern server architectures often employ **adaptive replacement policies** to optimize high-load, multi-threaded workloads.
* Recent studies suggest that hybrid approaches combining LRU and LFU often outperform single-strategy caches in enterprise and real-time systems.

#### **5. Significance in Industrial Systems**

In industrial applications such as high-performance computing, enterprise servers, and embedded real-time systems, **inefficient cache management can cause significant performance bottlenecks**. Selecting the appropriate replacement policy and optimizing cache behavior directly improves system responsiveness, reduces latency, and enhances throughput.

**References:**

1. Smith, A. J. (1982). Cache Memories. ACM Computing Surveys, 14(3), 473–530.
2. Jiang, S., & Zhang, X. (2002). LIRS: An Efficient Low Inter-reference Recency Set Replacement Policy to Improve Buffer Cache Performance. SIGMETRICS.
3. Intel Corporation. (2020). Intel® 64 and IA-32 Architectures Optimization Reference Manual.
4. AMD. (2019). AMD Software Optimization Guide for Processors.

## 3. Methodology

#### **1. Research Approach**

The study focuses on evaluating the performance of different cache replacement policies (FIFO, LRU, LFU) under real-world workloads. The approach involves **trace-driven simulation** of cache operations, measurement of key performance metrics, and comparison of policy effectiveness. The methodology follows these steps:

1. **Workload Selection:** Realistic memory access traces are collected from industrial applications, such as enterprise databases, high-performance computing tasks, or synthetic benchmarks representing typical workloads.
2. **Policy Simulation:** Cache replacement policies are simulated under identical conditions, including cache size, associativity, and block size.
3. **Performance Measurement:** Metrics such as cache miss rate, hit rate, and execution time impact are measured for each policy.
4. **Analysis:** Data from simulations are analyzed to identify which policies perform best under different workload conditions, and potential improvements are suggested.

#### **2. Hardware/Software/Tools Used**

* **Simulation Tools:**
  + **gem5 Simulator:** Provides detailed modeling of CPU, cache hierarchy, and memory access behavior.
  + **Custom Python/C++ Simulators:** Used to implement simple FIFO, LRU, and LFU algorithms for trace analysis.
* **Workload Traces:** Memory access traces from SPEC CPU benchmarks or real industrial workloads.
* **Hardware (Optional):** Standard desktop/server CPU for simulation execution. For hardware-level evaluation, **FPGA boards** can be used to test replacement strategies in embedded or low-latency systems.
* **Data Analysis Tools:** Python libraries such as pandas, matplotlib, and seaborn are used for performance metric calculation and visualization.

#### **3. Data Collection**

* Memory access traces are obtained either from benchmark suites or real application logs.
* Each access record includes the memory address, timestamp, and type of operation (read/write).
* Simulations replay these traces, applying the replacement policy logic to update cache state and track hits/misses.

#### **4. Data Analysis**

* **Cache Miss Rate:** Calculated as the ratio of cache misses to total memory accesses.
* **Hit Rate:** Complement of the miss rate; indicates the effectiveness of the cache policy.
* **Performance Comparison:** Metrics from different policies are compared across workloads to determine which performs best in terms of throughput and latency.
* **Visualization:** Graphs and tables illustrate performance differences among FIFO, LRU, LFU, and potential hybrid strategies.

## 4. Findings & Analysis

#### **1. Step-by-Step Execution**

The evaluation of cache replacement policies was carried out in a structured manner:

1. **Trace Collection:** Memory access traces were collected from real-world workloads and benchmark suites (e.g., SPEC CPU).
2. **Simulator Setup:** A cache simulator was configured with parameters such as cache size, block size, and associativity. FIFO, LRU, and LFU policies were implemented.
3. **Policy Simulation:** Each trace was replayed through the simulator for all three policies. Cache hits and misses were tracked at each memory access.
4. **Data Recording:** Metrics including cache miss rate, hit rate, and effective memory access latency were logged for analysis.
5. **Comparison & Visualization:** Performance results were compared using graphs and tables to identify trends and differences among policies.

#### **Results & Findings**

* **FIFO:**
  + Miss rate was moderate across most workloads.
  + Simple implementation with low computational overhead.
  + Occasionally evicted frequently accessed data, leading to suboptimal performance in workloads with temporal locality.
* **LRU:**
  + Consistently produced the lowest miss rates in workloads with strong temporal locality.
  + Required additional memory and tracking overhead for maintaining access order.
  + Performed well in enterprise server traces, where repeated access patterns were common.
* **LFU:**
  + Performed best in workloads with highly frequent accesses to a subset of data.
  + Struggled with sudden shifts in workload patterns, as old “frequent” data could remain in cache unnecessarily.
  + Required counter maintenance, which increased simulation complexity.

**Sample Simulation Data (Illustrative):**

|  |  |  |  |
| --- | --- | --- | --- |
| **Policy** | **Cache** | **Miss Rate (%)** | **Hit Rate (%)** |
| FIFO | 64 KB | 12.5 | 87.5 |
| LRU | 64 KB | 9.8 | 90.2 |
| LFU | 64 KB | 11.2 | 88.8 |

#### **3. Analysis**

* **Trends:**
  + LRU outperformed FIFO in workloads with repeated accesses to recent data.
  + LFU is beneficial in workloads with consistently “hot” data but requires counter management.
  + FIFO, while simple, can be suboptimal in high-load, real-world workloads.
* **Insights:**
  + **Hybrid policies** or **adaptive replacement strategies** can combine the benefits of LRU and LFU, dynamically adjusting to workload patterns.
  + Cache size and associativity significantly impact policy effectiveness; larger caches reduce misses but increase management overhead.
  + Real-world workload characteristics must guide policy selection rather than relying solely on theoretical performance.

#### **4. Challenges & Limitations**

* **Challenges:**
  + Collecting representative real-world memory traces was time-consuming.
  + Simulating large cache sizes or complex policies increased computational overhead.
  + LFU implementation required counter aging to prevent stale data accumulation.
* **Limitations:**
  + Simulations may not fully capture hardware-level nuances such as prefetching, multi-threading, or memory controller behavior.
  + Results are dependent on the selected workloads; other industrial applications may exhibit different access patterns.
* **Possible Improvements:**
  + Implement adaptive or hybrid policies such as LRU-K, ARC, or CLOCK-Pro.
  + Evaluate policies under multi-core or multi-level cache architectures.
  + Incorporate hardware-based simulation (e.g., FPGA or gem5 detailed CPU model) to validate real-world applicability.

## Industry Consultation & Expert Opinions

* 1. **Industry Professionals Contacted**

We consulted the following professionals to gain practical perspectives on cache replacement strategies in industrial contexts:

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| **Expert Name** | **Role** | **Organization** | **Relevance to Topic** |
| Al Asad Nur Riyad | Software Engineer | FIELD NATION | Designs large-scale, high-load server architectures with expertise in cache optimization |

* 1. **Key Insights Gained from Experts**
* **Commonly used policies:** LRU is the default in most enterprise systems due to its efficiency in capturing recency and maintaining high hit rates.
* **Real-time systems preference:** FIFO or adaptive LRU is used where predictable latency is more critical than absolute hit rate.
* **Workload-specific effectiveness:**
  + - Read-heavy workloads → LRU is preferred.
    - Write-heavy workloads → LFU provides better results.
* **Challenges in practice:** Experts highlighted false sharing, memory contention, and unpredictable access patterns as major hurdles.
* **Performance impact:** Lower miss rates increase throughput, but excessive evictions can lead to higher latency.
* **Future directions:** AI/ML-driven predictive caching is expected to play a major role in future cache optimization strategies.
  1. **Comparison with Our Findings**
* Alignment: Our simulation confirmed that LRU generally offers the best performance for read-heavy workloads, consistent with expert feedback.
* Differences: Experts emphasized that FIFO can be superior in real-time systems due to predictable latency—an aspect underestimated in our initial analysis.
* Implications: Based on expert opinions, we recommend adaptive or hybrid cache policies (e.g., LRU + LFU, or admission-controlled caching) to handle heterogeneous and dynamic workloads effectively.
  1. **Evidence of Consultation**

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**Figure-1: Visiting Card of Al Asad Nur Riyad.**



**Figure-2: Meeting screenshots**



**Figure-3: Meeting screenshots**

## 6. Discussion & Conclusion

#### **1. Summary of Major Findings**

The study evaluated three primary cache replacement policies—FIFO, LRU, and LFU—using trace-driven simulations of real-world workloads. Key findings include:

* **LRU** consistently achieved the lowest miss rates in workloads with temporal locality, making it suitable for enterprise systems with repeated data access patterns.
* **LFU** excelled in workloads with frequently accessed “hot” data but was less effective when workload patterns changed rapidly.
* **FIFO** was simple to implement but underperformed in high-load systems due to indiscriminate eviction of frequently used data.
* **Hybrid and adaptive policies** offer potential improvements by combining the strengths of multiple strategies and dynamically adjusting to workload changes.

These results highlight that the **choice of cache replacement policy directly impacts system performance**, particularly in high-demand industrial applications.

#### **2. Practical Applications and Future Directions**

* **Industrial Relevance:** The findings are applicable to enterprise servers, real-time systems, embedded applications, and high-performance computing, where efficient cache management reduces latency and improves throughput.
* **Policy Selection:** System architects can select or design cache policies tailored to workload characteristics. For example, LRU for temporal locality, LFU for frequency-heavy workloads, or adaptive policies for mixed patterns.
* **Future Work:**
  + Implement and evaluate hybrid or adaptive policies such as LRU-K, ARC, or CLOCK-Pro.
  + Extend analysis to multi-core or multi-level cache architectures.
  + Explore hardware-level validation using FPGA boards or detailed CPU simulators to measure real-world latency improvements.

#### **3. Reflection on Learning**

This study provided valuable insights into the**interplay between cache design and system performance**. By simulating multiple replacement policies and analyzing their impact on real workloads, key lessons include:

* Understanding the **trade-offs between simplicity and performance**in cache policy selection.
* Recognizing the importance of **workload-specific analysis** rather than relying on theoretical assumptions.
* Gaining practical experience with **trace-driven simulations and performance metrics,** enhancing skills relevant to system architecture and optimization.

## 7. References (IEEE Style)

## [1] [Smith, A. J. (1982). Cache memories. ACM Computing Surveys, 14(3), 473–530.](https://doi.org/10.1145/356924.356930)

[2] [Jiang, S., & Zhang, X. (2002). LIRS: An efficient low inter-reference recency set replacement policy to improve buffer cache performance. Proceedings of SIGMETRICS, 31(1), 31–42.](https://doi.org/10.1145/511334.511337)

[3] [Intel Corporation. (2020). Intel® 64 and IA-32 architectures optimization reference manual. Intel.](https://www.intel.com/content/www/us/en/developer/articles/technical/intel-sdm.html)

[4] [AMD. (2019). AMD software optimization guide for processors. AMD.](https://developer.amd.com/resources/developer-guides-manuals/)

[5] Expert Interview: Enterprise System Architect (2025, August 15). Insights on cache replacement policies in high-load industrial systems.

[6] **Memory Systems: Cache, DRAM, Disk** – Bruce Jacob, Spencer Ng, David Wang, 3rd Edition, Morgan Kaufmann, 2010.

[7] **Computer Architecture and Organization** – William Stallings, 10th Edition, Pearson, 2020.

[8] <https://fieldnation.com/>

## 8. Appendix (If Applicable)

**A. Sample Cache Simulator Code Snippet (Python)**

# Simple LRU Cache Simulation

class LRUCache:

def \_\_init\_\_(self, capacity):

self.cache = {}

self.capacity = capacity

self.order = []

def access(self, key):

if key in self.cache:

# Move key to end to show recent use

self.order.remove(key)

self.order.append(key)

return True # Hit

else:

if len(self.cache) >= self.capacity:

# Remove least recently used item

lru\_key = self.order.pop(0)

del self.cache[lru\_key]

self.cache[key] = True

self.order.append(key)

return False # Miss

# Example usage

cache = LRUCache(capacity=4)

trace = [1, 2, 3, 2, 4, 1, 5]

misses = 0

for addr in trace:

if not cache.access(addr):

misses += 1

print(f"Total misses: {misses}")

**B. Sample Simulation Table**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Trace ID** | **Policy** | **Cache** | **Miss Rate (%)** | **Hit Rate (%)** |
| Trace 1 | FIFO | 64 KB | 12.5 | 87.5 |
| Trace 2 | LRU | 64 KB | 9.8 | 90.2 |
| Trace 3 | LFU | 64 KB | 11.2 | 88.8 |