Mitul Tandon

Electrical Engineering
Indian Institute of Technology Bombay

B.Tech+M.Tech
Dual Degree
EE5: Electronic Systems

Examination	University	Institute	Year	CPI/%
Graduation	IIT Bombay	IIT Bombay	2027	8.70
Intermediate	CBSE	JNV Devrala, Bhiwani	2022	96.6
Matriculation	CBSE	JNV Devrala, Bhiwani	2020	96.2

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I am broadly interested in Computer Systems and Architecture, with a focus on **Architectures for AI Datacenters** and **Machine Learning Accelerators**. My work has involved **hardware-based performance optimizations for graph analytics**, **cache replacement policies**, and **3D DRAM caches**, where I have explored novel techniques to improve computational efficiency, optimize memory hierarchies, and enhance overall system performance.

Publication

- Varun Venkitaraman, Tejeshwar Thorawade, **Mitul Tandon**, Keerthisagar Kokkiligadda, Virendra Singh, and Janak Patel. "LiC: Low-Cost Cache Replacement Algorithm for All Cache Levels." *33rd IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC 2025)*, Puerto Varas, Chile, October 12–15, 2025. **(Accepted, to appear)**

Research Experience

Improving Memory Subsystem Efficiency for Graph Analytics *(Dec'24-May'25)*

Research Project | CADSL | Prof. Virendra Singh, IIT Bombay

- Analyzed **hardware-based prefetching mechanisms** such as DROPLET, along with cache management techniques like GRACE to optimize on-chip **cache utilization** and **accelerate graph processing**.
- Proposed and modeled a hardware-based, **data-aware prefetching mechanism** designed for graph analytics applications.
- Achieved up to 78% performance improvement over the baseline and 16% improvement over the state-of-the-art hardware prefetcher **DROPLET** across applications in the GAP Benchmark Suite, using the **Sniper simulator**.

Low Cost Cache Replacement Policy *(Jan'25-Mar'25)*

EE 691: R & D Project | CADSL | Prof. Virendra Singh, IIT Bombay

- Proposed a **lightweight cache replacement policy** for the **entire cache hierarchy** (all levels), focusing on **reduced area**, **lower power consumption** and a simplified decision-making algorithm.
- Implemented **pseudo-LRU** (tree-based) and **NRU** (1-bit RRPV version of SRRIP) replacement policies and performed a comparative analysis of the proposed policy against various other replacement policies using the **ChampSim** simulator.
- Achieved **significant storage reduction**, lowering requirements by factors of 4x, 3.75x, 16x, 14x and 28x compared to NMRU, pseudo-LRU, LRU/SRRIP/DRRIP, SHiP and Hawkeye respectively with **negligible performance loss**.

Set Associative 3D DRAM Caches *(Aug'24-Nov'24)*

CS 490: R & D Project | CASPER | Prof. Biswabandan Panda, IIT Bombay

- Conducted a literature review on **3D DRAM technologies**, including **High Bandwidth Memory** and **Hybrid Memory Cube** to understand their architecture, core functionalities, and potential for high-bandwidth applications.
- Performed an in-depth analysis of SILO, which discusses the use of a **private die-stacked DRAM** cache similar to HMC.
- Developed a 64 MB **HMC tag array for an HBM cache** using the **ChampSim** simulator, enabling **set associativity** in HBM.
- Achieved an 8.5% improvement over the directly mapped HBM cache and a 24.27% speedup compared to the baseline.

Processing Data Where It Makes Sense *(Jun'24-Jul'24)*

Summer Research Project | CADSL | Prof. Virendra Singh, IIT Bombay

- Conducted an extensive **literature review** on **processing-in-memory**, and the **simulators** used to simulate PIM systems.
- Analyzed the **Ramulator** paper and reproduced its results using the corresponding simulator (Ramulator), involving a comparison of **IPC metrics** across various **DRAM** standards with **22 benchmarks** from the **SPEC2006** suite.
- Used **ZSim+Ramulator** to simulate multiple benchmarks from the **DAMOV** suite, comparing **IPC** and **cycle counts** across **host**, **PIM**, and **host with prefetcher** systems, with PIM systems leveraging computations in the **logic layer** of an **HMC**.

Technical Projects

Pipelined RISC Processor *(Mar'24-May'24)*

EE 309: Microprocessors | Prof. Virendra Singh, IIT Bombay

- Designed **IITB-RISC**, a **16-bit** computing system featuring a **6-stage pipelined processor**, enabling predicated instruction execution, **multiple load/store** operations, and **branch prediction** for improved instruction flow handling.
- Implemented **hazard mitigation** techniques, including **pipeline stalling**, **flushing**, and a **data forwarding mechanism**, combined with a **history-bit-based** branch predictor, resulting in reduced stalls and improved IPC.
- Employed **behavioural** and **structural modeling** techniques in **VHDL** to program the **datapath** including pipelines, branch predictor, hazard detection and mitigation systems, ALU, data & instruction memory and systems for multiple load/store.
- Developed an extensive instruction set for comprehensive system testing through simulations using **ModelSim**.

Multicycle Architecture Processor *(Nov'23-Jan'24)*

EE 224: Digital Systems | Prof. Virendra Singh, IIT Bombay

- Modeled **IITB-CPU**, a **16-bit computer system** with an **8-register architecture**, capable of interpreting three types of machine code instructions **(R, I, and J)** and supporting a Turing-complete ISA comprising of **14 instructions**.
- Programmed the **controller** and key processor components such as the **ALU**, **Register File**, and **Memory Unit**.
- Employed **VHDL** to implement **structural modeling** techniques for **code optimization**, which significantly enhanced testing efficiency on the **Xen-10 FPGA**, facilitating the thorough validation of all instructions and system functionalities.
- Drafted comprehensive digital documentation for the processor, including **FSM**, **flowcharts**, and **component designs**.

One Program To Outspeed Them All *(Jun'24-Jul'24)*

Summer Of Code 2024 | WnCC, IIT Bombay

- Implemented **multithreading** in a **SAT solver** to enable parallel processing of the search space for **Max-SAT** problems.
- Achieved a 2.2x performance gain through implementation of **SIMD** instructions, along with a **second-order** improvement via **memoization**, while enhancing overall efficiency by leveraging both **spatial** and **temporal locality** in the cache.
- Utilized **OpenCL** to achieve an approximate 300x performance speedup in **GPU-based vectorized matrix operations**, including multiplication, inversion, transposition, and discrete fast fourier transform.

Logic Analyser for PicoIRIS *(Jun'24-Jul'24)*

Summer Project | Wadhwani Electronics Lab | Prof. Siddharth Tallur, IIT Bombay

- Upgraded PicoIRIS, an in-house all-in-one PCB with Arbitrary Function Generator (AFG) and Digital Storage Oscilloscope (DSO) functionalities, by integrating **logic analyzer** capabilities to facilitate digital signal analysis in **academic labs**.
- Programmed **PIC32** for **Bluetooth-based UART** communication using a HC-05 bluetooth module, enabling data sampling from its ports at rates **upto 500 kHz** for effective debugging of **UART**, **I2C**, and **lower-speed SPI** data.
- Developed an interactive **Qt-based GUI**, integrating it with backend Python code for data processing, enhancing user experience and analysis capabilities for **data visualization**, with current support for **UART debugging** features.

Colorization of B/W Images using DNN *(Dec'23-Jan'24)*

WiDS 2023 | Analytics Club, IIT Bombay

- Utilized Python libraries **NumPy**, **Pandas**, **Matplotlib**, **Pillow**, and **Scikit-Learn** for preprocessing the **MNIST** dataset, and developed a **CNN** using **PyTorch** with **Batch Normalization** for efficient digit classification training.
- Evaluated and optimized the model's performance by thoroughly analyzing accuracy metrics such as **precision**, **recall**, **F1-score**, and **confusion matrices**, identifying areas for improvement to enhance overall predictive capability.
- Implemented colorization models: **Alpha**, **Beta**, and **Final**, incorporating **Transfer Learning** through the integration of the **Inception-ResNet-v2** classifier to enhance object understanding and improve **coloring accuracy**.

128-bit AES Encryption *(Dec'23-Jan'24)*

Self Learning Project

- Conducted an in-depth analysis of the **Official NIST-AES** documentation, leading to the successful implementation of **128-bit AES encryption** in **ECB** (Electronic Codebook) mode using **VHDL** in **Quartus Prime**.
- Designed and optimized the complete flow and key sub-processes including **Sub-Bytes**, **Shift Rows**, **Mix Columns**, **Add Round Key**, and **Key Expansion**, for the encryption algorithm using structural modeling.
- Developed a comprehensive **testbench** with a **trace file**, leveraging **ModelSim** for thorough model verification and testing.

Reinforcement Learning *(Jun'23-Jul'23)*

Self Learning Project

- Attended the course **MIT 6.S191: Introduction to Deep Learning** and reviewed the literature titled **'Playing Atari with Deep Reinforcement Learning'**, which helped build foundational knowledge in the field.
- Gained an in-depth understanding of the workings of **Deep Q-Networks** and the mechanisms of **Experience Replay**.
- Gained hands-on experience with **OpenAI Gymnasium** by setting up **Stable Baselines** and training various **Atari models**, including **cartpole**, **pendulum**, and **acrobot**, using algorithms such as **DQN**, **A2C**, **PPO**, and **DDPG**.

Microcontroller Interfacing and Programming *(Jan'24-Apr'24)*

EE 337: Microprocessors Lab | Prof. Nikhil Karamchandani, IIT Bombay

- Implemented algorithms such as Binary Search and Bubble Sort on the **8051 microcontroller** using **Assembly Language**.
- Developed an **8-key piano** on the 8051 microcontroller using **Embedded C** in the **Keil μvision5 IDE**, which involved utilizing **timers** and **interrupts** while interfacing with external hardware such as a **keyboard**, **LCD**, and **speaker**.
- Demonstrated a **Low-Pass Digital FIR Filter** by receiving data from an **ADC** via **SPI**, processing it on the microcontroller, and transmitting the output to a PC through a **USB-UART module**, where it was plotted using **Matplotlib**.

Digital Circuit Design *(Sep'23-Nov'23)*

EE 214: Digital Circuits Lab | Prof. Siddharth Tallur, IIT Bombay

- Developed various digital circuits, including **muxes**, **priority encoder**, **prime number detector**, **Fibonacci detector**, **BCD adder**, **ALU**, and **universal barrel shifter**, employing structural modeling using **VHDL** on **Quartus Prime**.
- Designed mealy or moore type **FSM**s to implement a **clock divider**, **tone generator**, and **traffic signal controller** using **dataflow** and structural modeling techniques, and utilized **testbenches** and **trace files** for verification of all circuits.
- Implemented **scan chain** for internal state testing of all designed combinational and sequential circuits on the **Xen10 FPGA**, and performed **pin planning** to ensure effective interfacing with external components.

Other Projects

Advanced Controller Design
(Aug'24-Nov'24)

EE 324: Control Systems Lab | Prof. Debraj Chakraborty, IIT Bombay

- Designed and implemented a **PID** control algorithm to achieve **accurate 180-degree** rotation of a motor using **Arduino**.
- Developed and fine-tuned an **LQR controller** based on a real-time state-space feedback system to balance an **inverted pendulum** using a rotary arm in a **two-degree-of-freedom** motion system, adhering to deviation constraints of **±3 degrees**.
- Implemented a **PID** controller for a line-following robot, enabling precise sharp turns and stable movement at high speeds.

Analog Circuit Design
(Jan'24-Apr'24)

EE 230: Analog Circuits Lab | Prof. Anil K.G. , IIT Bombay

- Implemented **sallen-key filter**, **multivibrator**, **precision rectifier** and **multi-feedback band-pass filter** on hardware.
- Simulated a range of circuits on **LTspice**, including differential amplifiers and **current mirrors** using MOSFETs, as well as **logarithmic amplifiers** using op-amps, to predict hardware behavior and subsequently implemented them on hardware.
- Implemented a combined filter circuit consisting of a second-order filter and **notch filter**, integrated with an **instrumentation amplifier** and right-leg drive circuit to develop an **Electrocardiogram** (ECG) **amplifier**.

Radio-Controlled Plane
(Oct'23-Nov'23)

RC Plane Competition | Aeromodelling Club, IIT Bombay

- Engineered a Radio Controlled **Flying Wing** with **ESC**s, **Servos** and **BLDC** motors, controlled via 4-channel transmitter.
- Innovated a new design by placing two **BLDC motors vertically** within the wings for **smoother take-offs and landings**.
- Featured in the **Aeromodelling Club's** exhibit at the **Tech and RnD Expo '23**, organised by the *Institute Technical Council* (*IIT Bombay*), highlighting the innovative design and technological prowess of our Radio Controlled plane.

Technical Skills

Languages	C++, Embedded C, Python, VHDL, Verilog, 8051 Assembly, LaTeX
Software	Git, Quartus, Fusion360, MATLAB, KeilIDE, GNU Radio, LTSpice, NGSpice, KiCad
Python Libraries	NumPy, Matplotlib, Pandas, Scikit-Learn, PyTorch, pySerial, ftd2xx
Simulators	ChampSim, Sniper, Zsim+Ramulator, Ramulator, ModelSim

Scholastic Achievements

- Awarded a **Change of Department** to **Electrical Engineering** in recognition of outstanding academic performance. *(2023)*
- Ranked in the **top 1.2%** among over **160,000+** candidates in the **Joint Entrance Examination Advanced 2022**. *(2022)*
- Ranked in the **top 1.1%** among over **1 million+** candidates in the **Joint Entrance Examination Main 2022**. *(2022)*
- Achieved a **centum** in **Computer Science** (Intermediate), ranking among the **top 0.1%** of students nationwide. *(2022)*
- Attained a **perfect score** in **Mathematics** (Marticulation), ranking among the **top 0.1%** of students nationwide. *(2020)*

Teaching Assistantship

EE 224 [Digital Systems]
(Aug'24-Nov'24)

Instructor: Prof. Virendra Singh, IIT Bombay

- Serving as the **sole Undergraduate Teaching Assistant** for EE 224 [Digital Systems], guiding **95+ sophomore** students, managing weekly test invigilation, grading answer scripts, and assisting with **course evaluation** processes.
- Helping in developing **quiz solutions** and providing **academic mentorship**, assisting students with course-related queries by organizing **doubt-solving sessions** to enhance their understanding of the course material.

Courses Undertaken

Electrical Engineering	Processor Design, Algorithmic Design of Digital Systems, Microprocessors, Electronic Design Lab, Digital Signal Processing, Digital Systems, Microprocessors Laboratory, Digital Circuits Lab, Signal Processing, Electromagnetic Waves, Analog Circuits, Communication Systems, Control Systems, Communications Lab, Control Systems Lab, Analog Circuits Lab, Signal Processing - I, Power Engineering - I & II.
CS & AI	Introduction to Data Science and Machine Learning, Programming for Data Science, Discrete Structures, Computer Programming and Utilization.
Mathematics	Probability and Random Processes, Calculus - I & II, Differential Equations, Linear Algebra.

Extracurriculars

- Successfully completed the course **Python for Data Science** at Learner's Space '23 organised by *ITC, IIT Bombay*. *(2023)*
- Completed a **1 Year Military Training** at **National Cadet Corps** in the 2 Maharashtra Engineering Regiment. *(2023)*
- Won the inter-company **Training General Championship** as part of a **9 Cadet Contingent** at *NCC, IIT Bombay*. *(2023)*
- Won the inter-company **Cultural General Championship** through participation in the **group dance** and **drama**. *(2023)*
- Served as **Captain** for the company **Basketball** team, securing **2nd** place in the **Sports General Championship**. *(2023)*
- Attended a rigorous **10-day training program** at **CATC** as part of the 11 Haryana Battalion, organised by NCC. *(2019)*
- Participated in the **29th NVS Regional Basketball Meet** as part of a **7-member team** in the Under-14 category. *(2018)*
- **Proficient** in playing the **synthesizer** and regularly performed at **school assemblies** and various **cultural events**. *(2018)*
- Awarded an **Orange Belt** by the Goju-Ryu Karate-Do Sports Federation for demonstrating proficiency in **Karate**. *(2017)*
- Completed a comprehensive **3-month** dance course focused on **Salsa**, **Hip-Hop**, and **Bollywood** dance forms. *(2016)*