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COMP 4300: Homework 2

Points Possible: 100

Note: You do not need to submit hard copies.

Goals:

•To learn general-purpose register architectures.

•To learn encoding an instruction set.

Questions: 100 points: (1) 30 points, (2) 70 points

1.[30 points] The design of MIPS provides for 32 general-purpose registers and 32floating-point registers. If registers are good, are more registers better? List and discuss as many trade-offs as you can that should be considered by instruction set architecture designers examining whether to, and how much to, increase the numbers of MIPS registers.

- Implementing the CPU becomes more complicated with more registers.
- When we switch between programs, a task must save the contents of registers
    - This would take longer with more registers
    - An advantage though is that more registers means main memory will not have to be accessed as much
- Increasing the number of registers typically increases instruction size
- Little to be gained form having more data in registers as opposed to the cache

2.[70 points] Consider the case of a processor with an instruction length of 12 bits and with 32 general purpose registers so the size of the address fields is 5 bits.

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2.1 [35points] Is it possible to have instruction encodings for the following? You must provide encoding details to explain your answers.

•3 two-address instructions

The two address fields consume 10 bits.

With the remaining two bits there are four possible values, 00, 01, 10, and 11

Since there are four combinations, then we can fit 3 two address instructions and still have 1 remaining. Two-Address = 00, 01, 10. Remaining = 11 (reserved)

•30 one-address instructions

The remaining "11" will be used for the remaining one-address and zero-address instructions.

There are 32 possible combinations

11, 00000, 11, 00001, ..., 11,11101. Will be used for the one-bit addresses.

The last 2 11,11110 and 11,11111 will be used in the next section.

•45 zero address instructions

11,11110, last five bits will be used for zero address instructions

11,11111, last five bits will be used for zero address instructions

For each there are 2^5 possible combinations.

So, total there are 2 * 2^5 combinations = 64 combinations.

Since we only need room for 45, there is enough room.

TO ANSWER THE QUESTION YES, WE CAN FIT THE FOLLOWING

2.2 [35points] Is it possible to have instruction encodings for the following? You must provide encoding details to explain your answers.

•3 two-address instructions

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The two address fields consume 10 bits.

With the remaining two bits there are four possible values, 00, 01, 10, and 11

Since there are four combinations, then we can fit 3 two address instructions and still have 1 remaining. Two-Address = 00, 01, 10. Remaining = 11 (reserved)

•31 one-address instructions

The remaining "11" will be used for the remaining one-address and zero-address instructions.

There are 32 possible combinations

11, 00000, 11, 00001, ..., 11,11110. Will be used for the one-bit addresses.

The last 1 11,11111 will be used in the next section.

•35 zero address instructions

11,11111, last five bits will be used for zero address instructions

For each there are 2^5 possible combinations = 32.

We need room for 35 but there is only room for 32.

TO ANSWER THE QUESTION NO, WE CAN'T FIT THE FOLLOWING