

Number Systems

System	Value	-x	Negation	Addition	Overflow
Sign & Magnitude	Invert first bit				
1s Complement	+ve: same as 2s -ve: $2s + 1$	$2^n - x - 1$	Invert all bits	If MSB carry out: $\oplus=1$	Result opposite sign of A and B
2s Complement	if $x[i]==1: \oplus= 2^i$ except 1st num: minus	$2^n - x$	Invert all bits + 1	Ignore MSB carry out	MSB carry in != MSB carry out Result opposite sign of A and B
Excess-n	$x-n$				
IEEE 754	(Sign) (1.Mantissa) $\times 2^{\text{Exponent}}$	Invert first bit		1: Sign 8: Ex-127 Exp	--- 23: Mantissa
System	-2	-1	0	1	2
Sign & Magnitude	10000010	10000001	00000000	00000001	00000010
1s Complement	11111101	11111110	0000/1111	00000001	00000010
2s Complement	11111110	11111111	00000000	00000001	00000010
Excess-127	01111101	01111110	01111111	10000000	10000001

MIPS

Operation	RR1	RR2	WR	WD	Opr1	Opr2	Address	Write Data
lw \$a, x(\$b)	\$b	\$a	\$a	Mem([\$b] + x)	[\$b]	x	[\$b] + x	[\$a]
beq \$a,\$b, immd	\$a	\$b	\$b	?	[\$a]	[\$b]	[\$a] - [\$b]	[\$b]
sub \$a, \$b, \$c	\$b	\$c	\$a	[\$b] - [\$c]	[\$b]	[\$c]	[\$b] - [\$c]	[\$c]
addi \$a, \$b, immd	\$b	\$a	\$a	[\$b] + immd	[\$b]	immd	[\$b] + immd	[\$a]

MIPS Reference Data

(1)



CORE INSTRUCTION SET

NAME, MNEMONIC	FOR-MAT	OPERATION (in Verilog)	OPCODE / FUNCT (Hex)
Add	add	R[Rd] = R[rs] + R[rt]	(1) 0 / 20 _{hex}
Add Immediate	addi	I R[rt] = R[rs] + SignExtImm	(1,2) 8 _{hex}
Add Imm. Unsigned	addiu	I R[rt] = R[rs] + SignExtImm	(2) 9 _{hex}
Add Unsigned	addu	R R[Rd] = R[rs] + R[rt]	0 / 21 _{hex}
And	and	R R[Rd] = R[rs] & R[rt]	0 / 24 _{hex}
And Immediate	andi	I R[rt] = R[rs] & ZeroExtImm	(3) c _{hex}
Branch On Equal	beq	I if(R[rs]==R[rt]) PC=PC+4+BranchAddr	(4) 4 _{hex}
Branch On Not Equal	bne	I if(R[rs]!=R[rt]) PC=PC+4+BranchAddr	(4) 5 _{hex}
Jump	j	J PC=JumpAddr	(5) 2 _{hex}
Jump And Link	jal	J R[31]=PC+8;PC=JumpAddr	(5) 3 _{hex}
Jump Register	jr	R PC=R[rs]	0 / 08 _{hex}
Load Byte Unsigned	lbu	I R[rt]={24'b0,M[R[rs]]+SignExtImm(7:0)}	(2) 24 _{hex}
Load Halfword Unsigned	lhu	I R[rt]={16'b0,M[R[rs]]+SignExtImm(15:0)}	(2) 25 _{hex}
Load Linked	ll	I R[rt] = M[R[rs]]+SignExtImm	(2,7) 30 _{hex}
Load Upper Imm.	lui	I R[rt] = {imm, 16'b0}	f _{hex}
Load Word	lw	I R[rt] = M[R[rs]]+SignExtImm	(2) 23 _{hex}
Nor	nor	R R[Rd] = ~ (R[rs] R[rt])	0 / 27 _{hex}
Or	or	R R[Rd] = R[rs] R[rt]	0 / 25 _{hex}
Or Immediate	ori	I R[rt] = R[rs] ZeroExtImm	(3) d _{hex}
Set Less Than	slt	R R[Rd] = (R[rs] < R[rt]) ? 1 : 0	0 / 2a _{hex}
Set Less Than Imm.	slti	I R[rt] = (R[rs] < SignExtImm) ? 1 : 0 (2)	a _{hex}
Set Less Than Imm. Unsigned	sltiu	I R[rt] = (R[rs] < SignExtImm) ? 1 : 0	(2,6) b _{hex}
Set Less Than Unsigned	sltu	R R[Rd] = (R[rs] < R[rt]) ? 1 : 0	(6) 0 / 2b _{hex}
Shift Left Logical	sll	R R[Rd] = R[rt] << shampt	0 / 00 _{hex}
Shift Right Logical	srl	R R[Rd] = R[rt] >> shampt	0 / 02 _{hex}
Store Byte	sb	I M[R[rs]]+SignExtImm(7:0)=R[rt](7:0)	(2) 28 _{hex}
Store Conditional	sc	I M[R[rs]]+SignExtImm = R[rt]; R[rt] = (atomic) ? 1 : 0	(2,7) 38 _{hex}
Store Halfword	sh	I M[R[rs]]+SignExtImm(15:0)=R[rt](15:0)	(2) 29 _{hex}
Store Word	sw	I M[R[rs]]+SignExtImm = R[rt]	(2) 2b _{hex}
Subtract	sub	R R[Rd] = R[rs] - R[rt]	(1) 0 / 22 _{hex}
Subtract Unsigned	subu	R R[Rd] = R[rs] - R[rt]	0 / 23 _{hex}
		(1) May cause overflow exception (2) SignExtImm = { 16{immediate[15]}, immediate } (3) ZeroExtImm = { 16{1b'0}, immediate } (4) BranchAddr = { 14{immediate[15]}, immediate, 2'b0 } (5) JumpAddr = { PC+4[31:28], address, 2'b0 } (6) Operands considered unsigned numbers (vs. 2's comp.) (7) Atomic test&set pair; R[rt] = 1 if pair atomic, 0 if not atomic	

BASIC INSTRUCTION FORMATS

R	opcode	rs	rt	rd	shamt	funct	
	31	26 25	21 20	16 15	11 10	6 5	0
I	opcode	rs	rt			immediate	
	31	26 25	21 20	16 15			0
J	opcode			address			
	31	26 25					0

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ARITHMETIC CORE INSTRUCTION SET

OPCODE / FMT / FT	/ FUNCT (Hex)
Branch On FP True	bclt FI if(FPcond)PC=PC+4+BranchAddr (4)
Branch On FP False	bclf FI if(!FPcond)PC=PC+4+BranchAddr(4)
Divide	div R Lo=R[rs]/R[rt]; Hi=R[rs]%R[rt] 0/-/-/1a
Divide Unsigned	divu R Lo=R[rs]/R[rt]; Hi=R[rs]%R[rt] (6) 0/-/-/1b
FP Add Single	add.s FR F[fd] = F[fs] + F[ft] 11/10/-/0
FP Add	add.d FR {F(fd),F(fd+1)} = {F(fs),F(fs+1)} + {F(ft),F(ft+1)} 11/11/-/0
Double	c.x.s* FR FPcond = {F(fs) op F(ft)} ? 1 : 0 11/10/-/y
FP Compare Single	c.x.d* FR FPcond = {{F(fs),F(fs+1)}} op {{F(ft),F(ft+1)}} ? 1 : 0 * (x is eq, lt, or le) (op is ==, <, or <=) (y is 32, 3c, or 3e)
FP Divide Single	div.s FR F[fd] = F[fs] / F[ft] 11/10/-/3
FP Divide	div.d FR {F(fd),F(fd+1)} = {F(fs),F(fs+1)} / {F(ft),F(ft+1)} 11/11/-/3
FP Multiply Single	mul.s FR F[fd] = F[fs] * F[ft] 11/10/-/2
FP Multiply	mul.d FR {F(fd),F(fd+1)} = {F(fs),F(fs+1)} * {F(ft),F(ft+1)} 11/11/-/2
FP Subtract Single	sub.s FR F[fd]=F[fs] - F[ft] 11/10/-/1
FP Subtract	sub.d FR {F(fd),F(fd+1)} = {F(fs),F(fs+1)} - {F(ft),F(ft+1)} 11/11/-/1
Double	load FP Single lwc1 I F[rt]=M[R[rs]+SignExtImm] (2) 31/-/-/--
Load FP	load FP ldc1 I F[rt]=M[R[rs]+SignExtImm]; F[rt+1]=M[R[rs]+SignExtImm+4] (2) 35/-/-/--
Double	move mfc0 R R[Rd] = Hi 0 / -/-/10
Move From Hi	mflo R R[Rd] = Lo 0 / -/-/12
Move From Lo	
Move From Control	mfc0 R R[Rd] = CR[rs] 10 / 0/-/0
Multiply	mult R {Hi,Lo} = R[rs] * R[rt] 0 / -/-/18
Multiply Unsigned	multu R {Hi,Lo} = R[rs] * R[rt] (6) 0 / -/-/19
Shift Right Arith.	sra R R[Rd] = R[rt] >> shampt 0 / -/-/3
Store FP Single	swci I M[R[rs]]+SignExtImm = F[rt] (2) 39/-/-/--
Store FP	sdci I M[R[rs]]+SignExtImm = F[rt]; M[R[rs]+SignExtImm+4] = F[rt+1] (2) 3d/-/-/--
Double	

FLOATING-POINT INSTRUCTION FORMATS

FR	opcode	fmt	ft	fs	fd	funct	
	31	26 25	21 20	16 15	11 10	6 5	0
FI	opcode	fmt	ft		immediate		0
	31	26 25	21 20	16 15			

PSEUDOINSTRUCTION SET

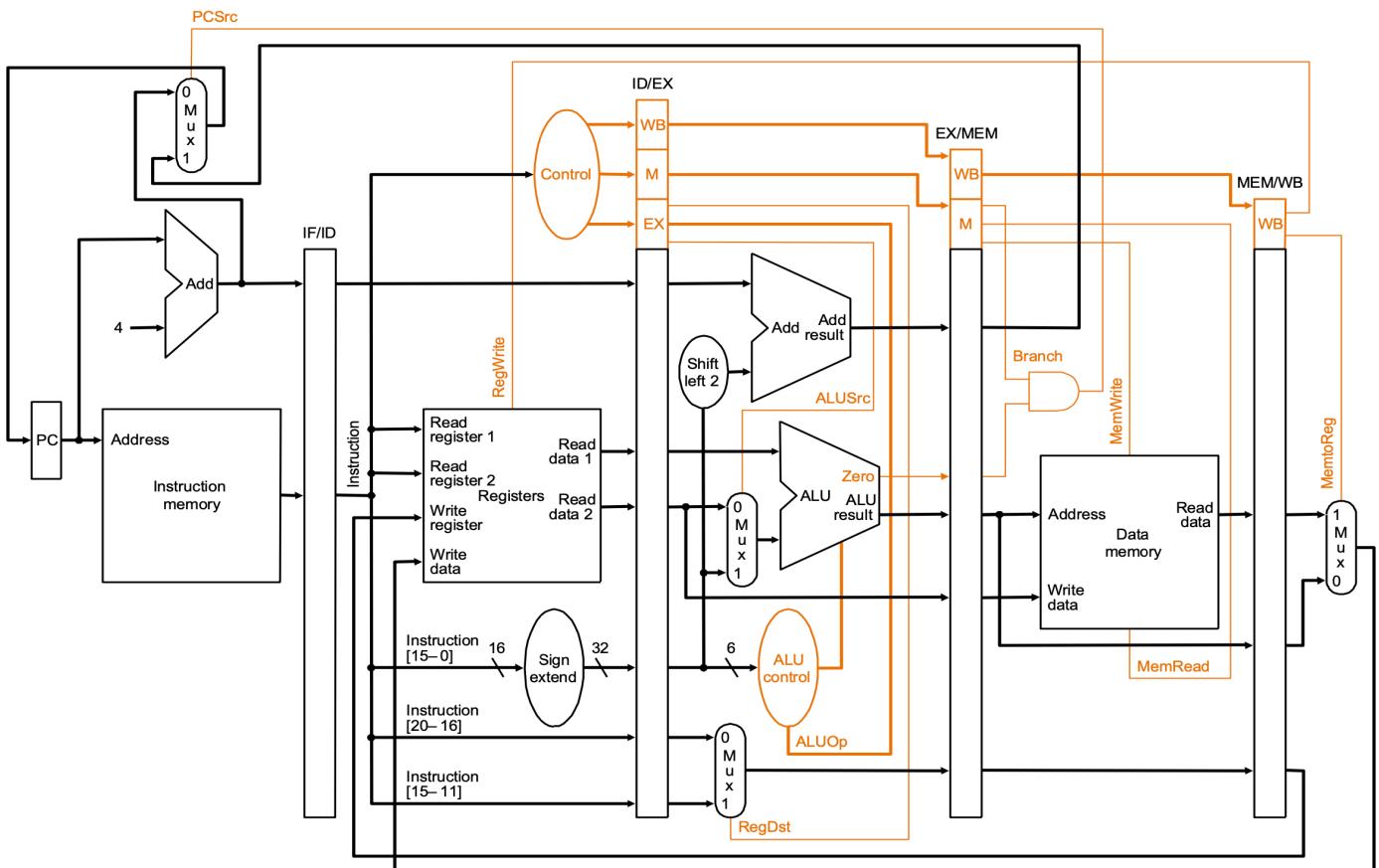
NAME	MNEMONIC	OPERATION
Branch Less Than	blt	if(R[rs]<R[rt]) PC = Label
Branch Greater Than	bgt	if(R[rs]>R[rt]) PC = Label
Branch Less Than or Equal	ble	if(R[rs]<=R[rt]) PC = Label
Branch Greater Than or Equal	bge	if(R[rs]>=R[rt]) PC = Label
Load Immediate	li	R[Rd] = immediate
Move	move	R[Rd] = R[rs]

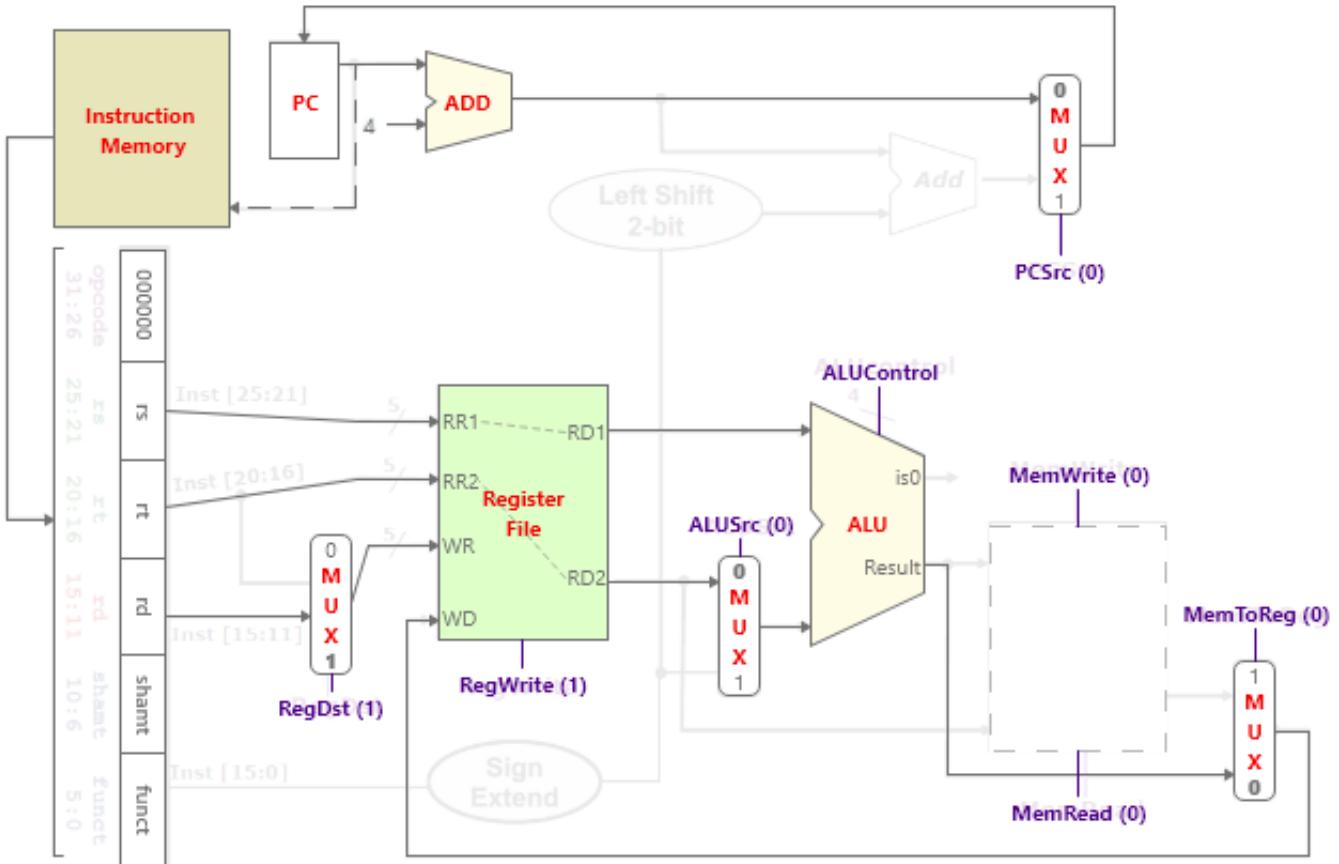
REGISTER NAME, NUMBER, USE, CALL CONVENTION

NAME	NUMBER	USE	PRESERVED ACROSS A CALL?
\$zero	0	The Constant Value 0	N.A.
\$at	1	Assembler Temporary	No
\$v0-\$v1	2-3	Values for Function Results and Expression Evaluation	No
\$a0-\$a3	4-7	Arguments	No
\$t0-\$t7	8-15	Temporaries	No
\$s0-\$s7	16-23	Saved Temporaries	Yes
\$t8-\$t9	24-25	Temporaries	No
\$k0-\$k1	26-27	Reserved for OS Kernel	No
\$gp	28	Global Pointer	Yes
\$sp	29	Stack Pointer	Yes
\$fp	30	Frame Pointer	Yes
\$ra	31	Return Address	Yes

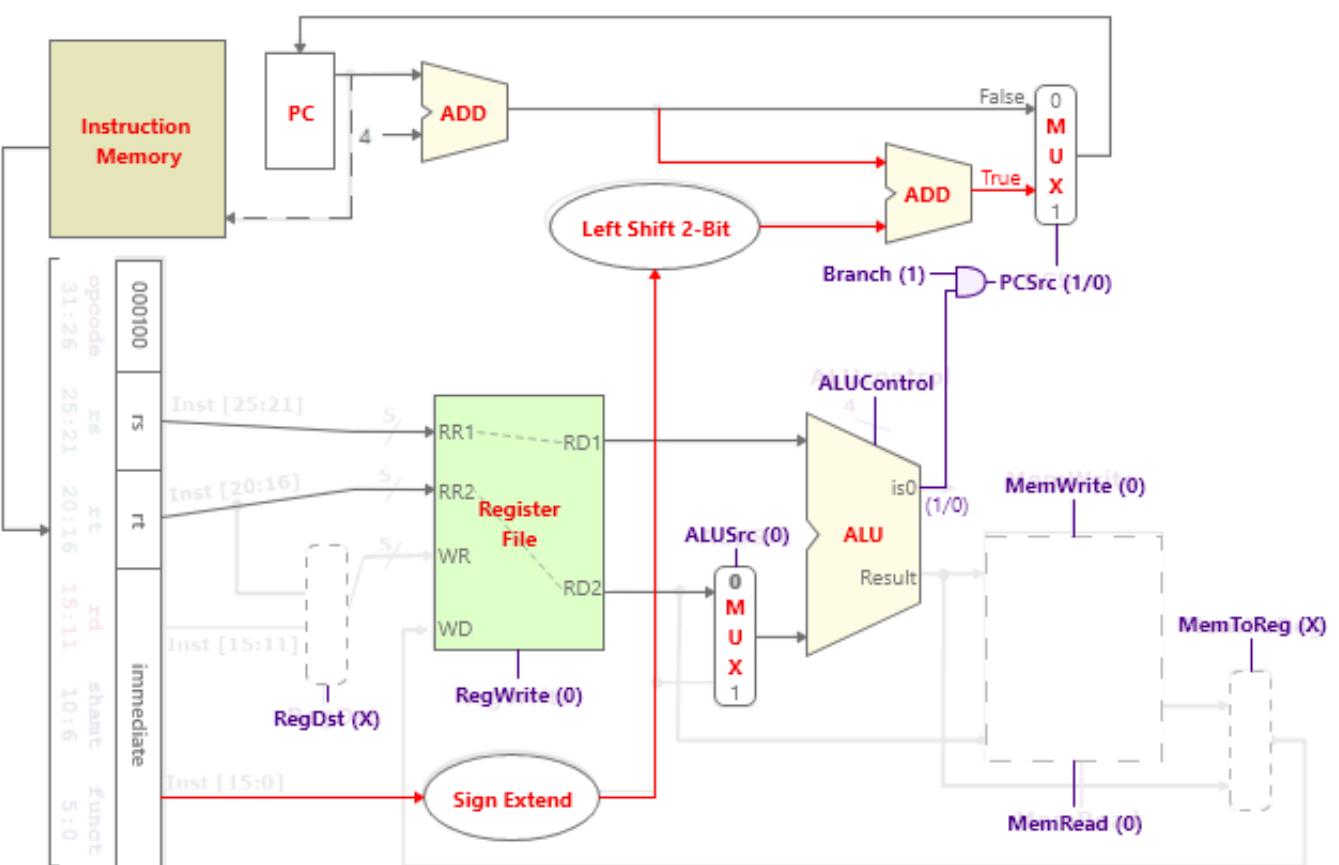
	EX Stage				MEM Stage			WB Stage	
	RegDst	ALUSrc	ALUOp		Mem Read	Mem Write	Branch	MemTo Reg	Reg Write
			op1	op0					
R-type	1	0	1	0	0	0	0	0	1
lw	0	1	0	0	1	0	0	1	1
sw	X	1	0	0	0	1	0	X	0
beq	X	0	0	1	0	0	1	X	0

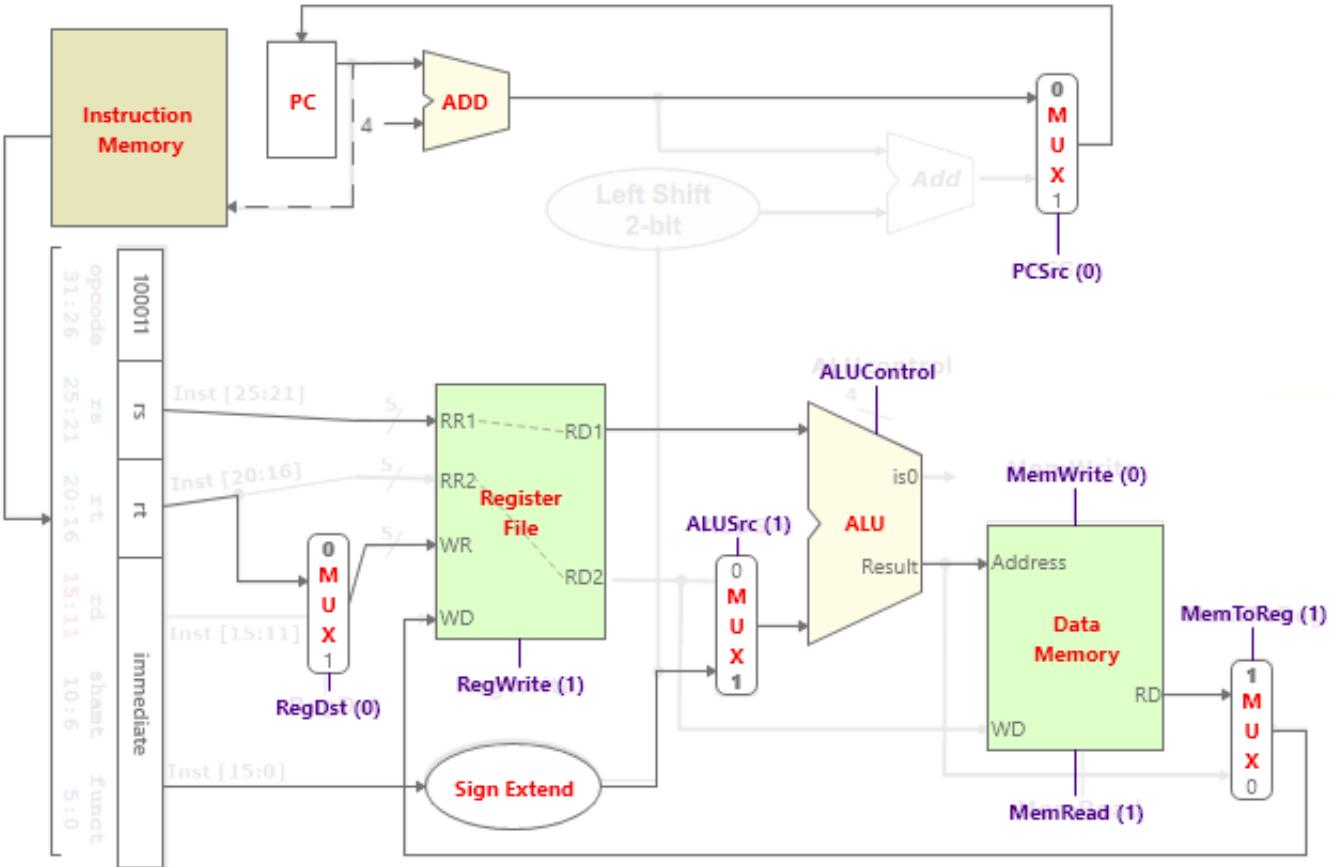
	Opcode (Op[5:0] == Inst[31:26])						Value in Hexadecimal
	Op5	Op4	Op3	Op2	Op1	Op0	
R-type	0	0	0	0	0	0	0
lw	1	0	0	0	1	1	23
sw	1	0	1	0	1	1	2B
beq	0	0	0	1	0	0	4



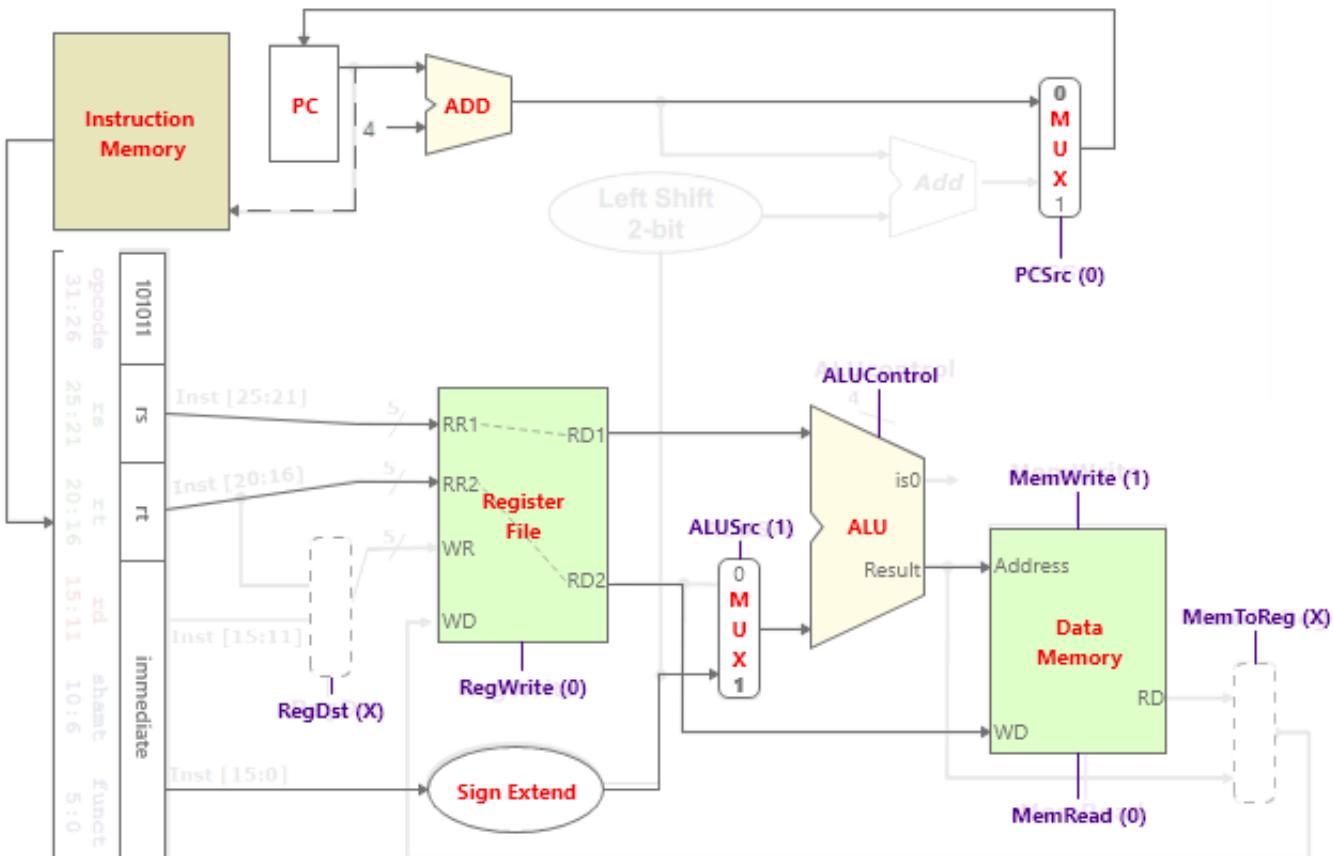


Add





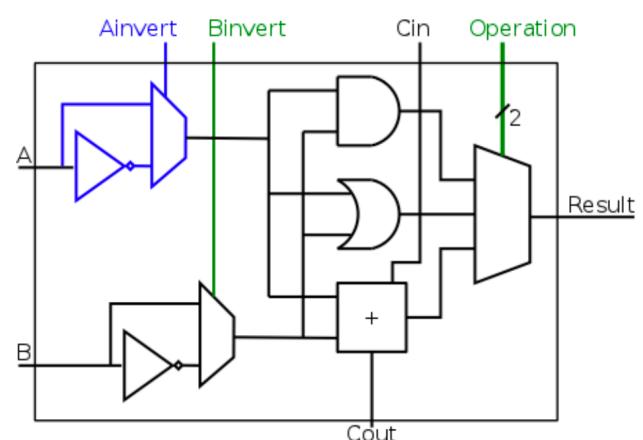
Load Word



Store Word

Opcode	ALUop	Instruction Operation	Funct field	ALU action	ALU control
lw	00	load word	xxxxxx	add	0010
sw	00	store word	xxxxxx	add	0010
beq	01	branch equal	xxxxxx	subtract	0110
R-type	10	add	10 0000	add	0010
R-type	10	subtract	10 0010	subtract	0110
R-type	10	AND	10 0100	AND	0000
R-type	10	OR	10 0101	OR	0001
R-type	10	set on less than	10 1010	set on less than	0111

ALUcontrol			Function
Ainvert	Binvert	Operation	
0	0	00	AND
0	0	01	OR
0	0	10	add
0	1	10	subtract
0	1	11	slt
1	1	00	NOR



Dependency	Solution	Inst	Stall	Dependency	Solution	Inst	Stall
Data	None	add	2	Control	Early		1
Data	None	lw	2	Control	Early	add	2
Data	Fwd	add	0	Control	Early	lw	3
Data	Fwd	lw	1	Control	Predict	YES	0
Control	None	ALL	3	Control	Delay	?	0

Boolean Algebra

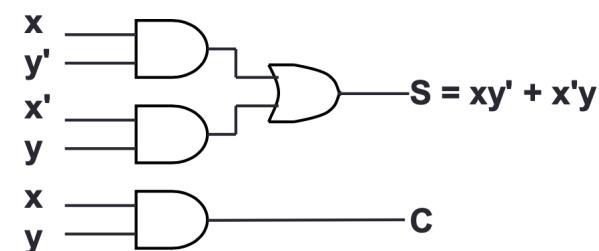
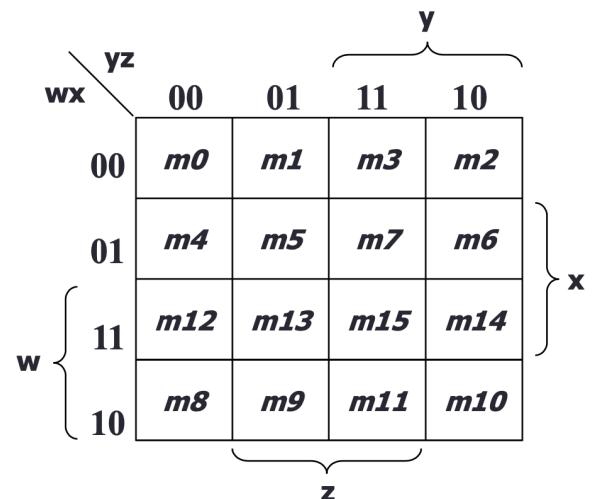
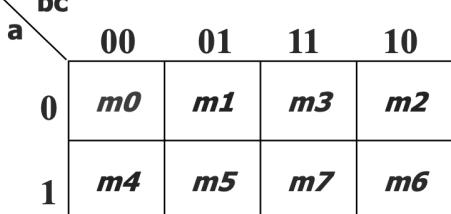
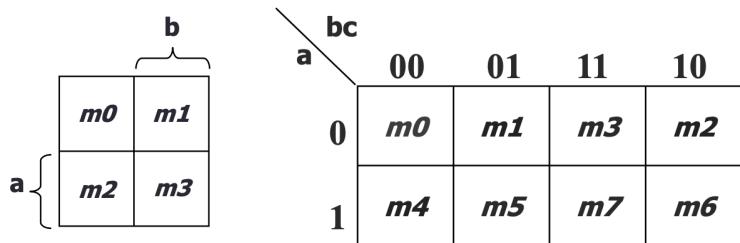
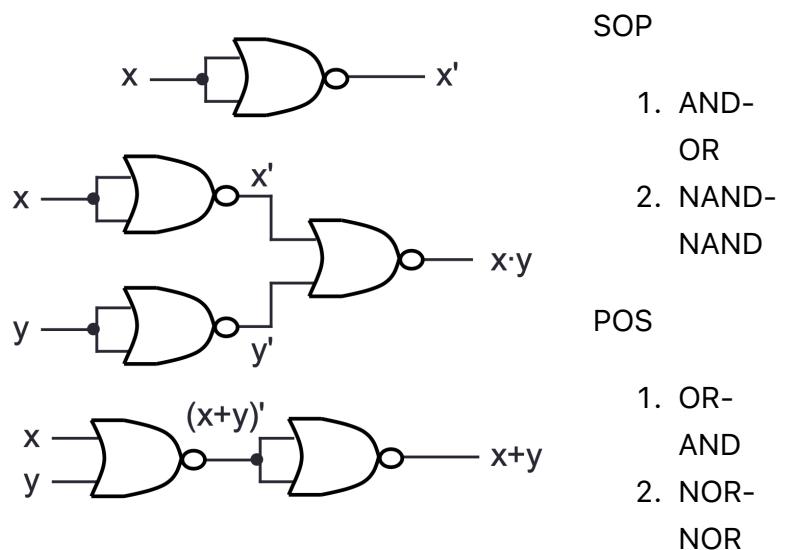
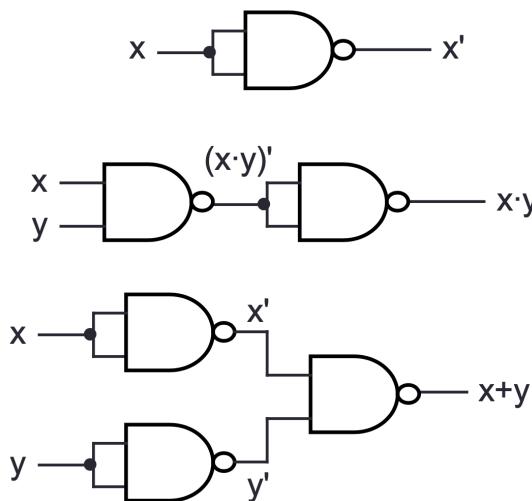
Identity laws	
$A + 0 = 0 + A = A$	$A \cdot 1 = 1 \cdot A = A$
Inverse/complement laws	
$A + A' = 1$	$A \cdot A' = 0$
Commutative laws	
$A + B = B + A$	$A \cdot B = B \cdot A$
Associative laws *	
$A + (B + C) = (A + B) + C$	$A \cdot (B \cdot C) = (A \cdot B) \cdot C$
Distributive laws	
$A \cdot (B + C) = (A \cdot B) + (A \cdot C)$	$A + (B \cdot C) = (A + B) \cdot (A + C)$

Idempotency	
$X + X = X$	$X \cdot X = X$
One element / Zero element	
$X + 1 = 1$	$X \cdot 0 = 0$
Involution	
$(X')' = X$	
Absorption 1	
$X + X \cdot Y = X$	$X \cdot (X + Y) = X$
Absorption 2	
$X + X' \cdot Y = X + Y$	$X \cdot (X' + Y) = X \cdot Y$
DeMorgans' (can be generalised to more than 2 variables)	
$(X + Y)' = X' \cdot Y'$	$(X \cdot Y)' = X' + Y'$
Consensus	
$X \cdot Y + X' \cdot Z + Y \cdot Z = X \cdot Y + X' \cdot Z$	$(X+Y) \cdot (X'+Z) \cdot (Y+Z) = (X+Y) \cdot (X'+Z)$

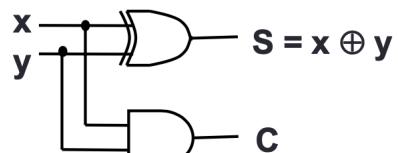
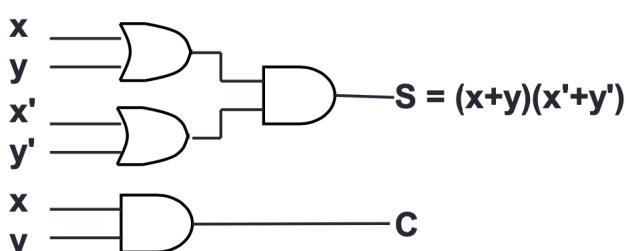
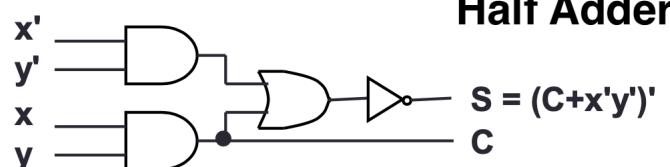
x	y	Minterms		Maxterms	
		Term	Notation	Term	Notation
0	0	$x' \cdot y'$	m0	$x+y$	M0
0	1	$x' \cdot y$	m1	$x+y'$	M1
1	0	$x \cdot y'$	m2	$x'+y$	M2
1	1	$x \cdot y$	m3	$x'+y'$	M3

Duality: If the AND/OR operators and 0/1 identity elements are interchanged, it remains valid
 $x+1 = 1 \rightarrow x \cdot 0 = 0$

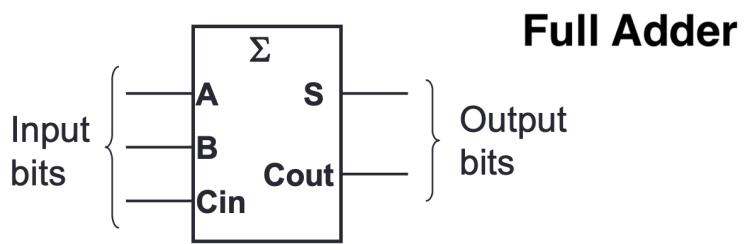
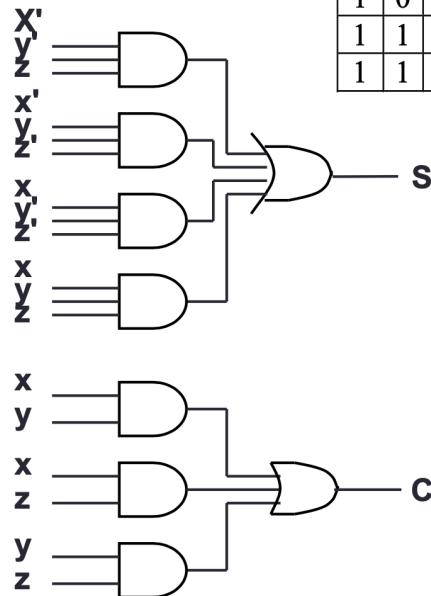
Logic Circuits



Half Adder

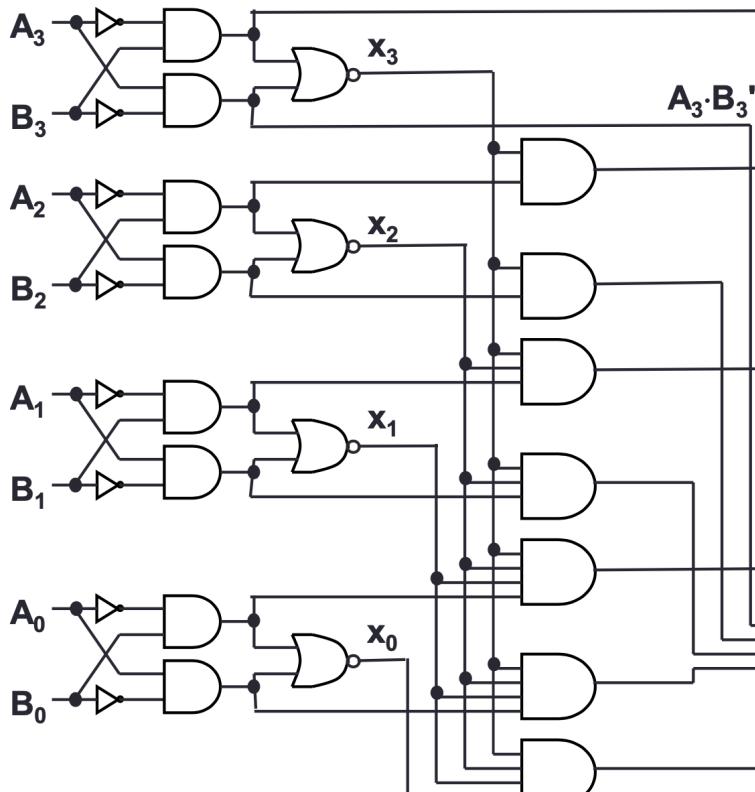
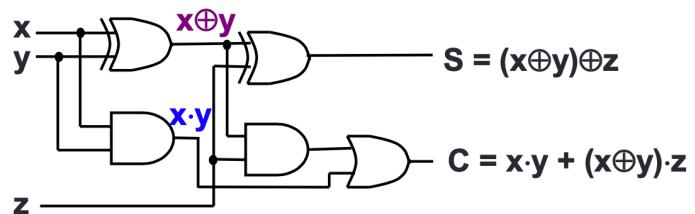


x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



	x	y	z	00	01	11	10
0	0	0	0	1			
1	1	1	1	1	1	1	1

$C = xy + xz + yz$ $S = x'y'z + x'y'z' + xy'z' + xyz$



Magnitude Comparator

$A_3 \cdot B_3'$

$$\begin{aligned} & A_3' \cdot B_3 + x_3 \cdot A_2' \cdot B_2 \\ & + x_3 \cdot x_2 \cdot A_1' \cdot B_1 \\ & + x_3 \cdot x_2 \cdot x_1 \cdot A_0' \cdot B_0 \end{aligned}$$

(A < B)

$$\begin{aligned} & A_3 \cdot B_3' + x_3 \cdot A_2 \cdot B_2' \\ & + x_3 \cdot x_2 \cdot A_1 \cdot B_1' \\ & + x_3 \cdot x_2 \cdot x_1 \cdot A_0 \cdot B_0' \end{aligned}$$

(A > B)

(A = B)

$$x_3 \cdot x_2 \cdot x_1 \cdot x_0$$

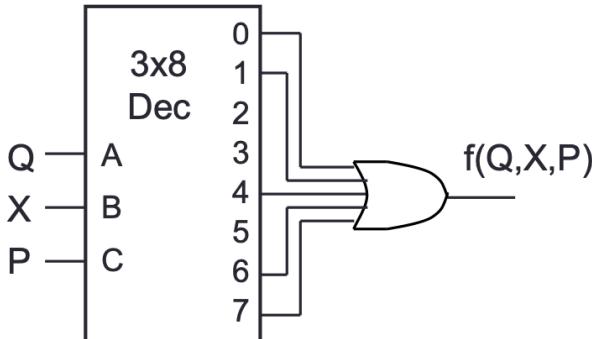
Let $A = A_3 A_2 A_1 A_0$, $B = B_3 B_2 B_1 B_0$; $x_i = A_i \cdot B_i + A_i' \cdot B_i'$

Functions using MSI

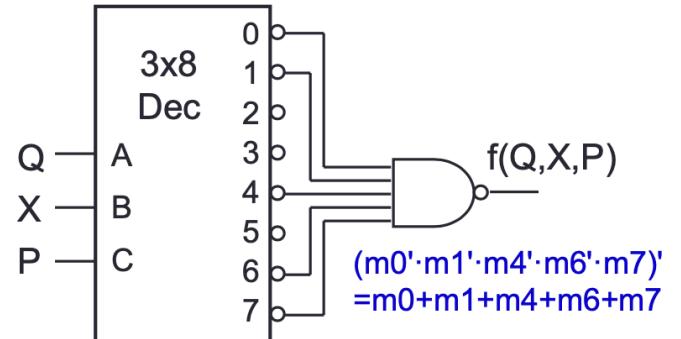
Demultiplexers are similar to a decoder (select) with enable (data)

Multiplexers are similar to a decoder (select) added with 2^n input lines (input)

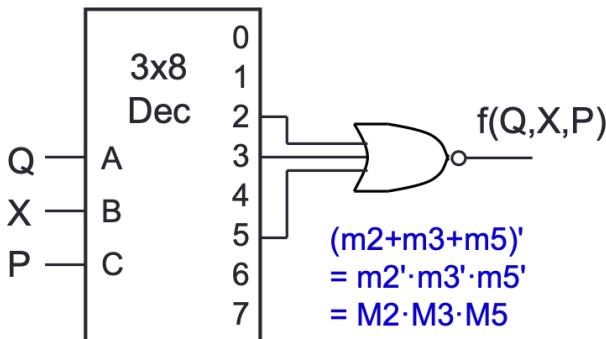
$$f(Q, X, P) = \sum m(0, 1, 4, 6, 7) = \prod M(2, 3, 5)$$



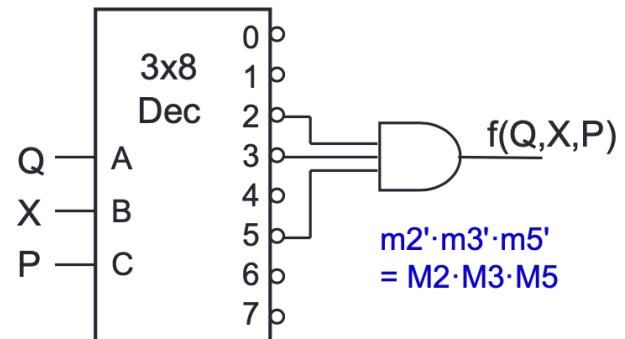
(a) Active-high decoder with OR gate.



(b) Active-low decoder with NAND gate.



(c) Active-high decoder with NOR gate.



(d) Active-low decoder with AND gate.

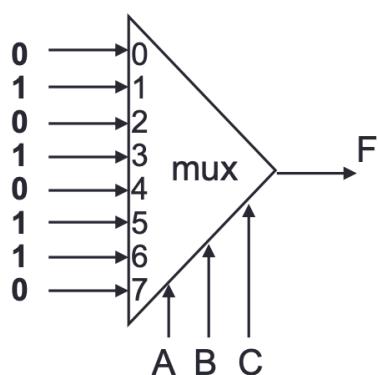
$$F(A, B, C) = \sum m(1, 3, 5, 6)$$

This method works because:

$$\begin{aligned} \text{Output} &= I_0 \cdot m_0 + I_1 \cdot m_1 + I_2 \cdot m_2 + I_3 \cdot m_3 \\ &\quad + I_4 \cdot m_4 + I_5 \cdot m_5 + I_6 \cdot m_6 + I_7 \cdot m_7 \end{aligned}$$

Supplying '1' to I_1, I_3, I_5, I_6 , and '0' to the rest:

$$\text{Output} = m_1 + m_3 + m_5 + m_6$$



Sequential Logic

J	K	$Q(t+1)$	Comments
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q(t)'$	Toggle

S	R	$Q(t+1)$	Comments
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	?	Unpredictable

D	$Q(t+1)$	
0	0	Reset
1	1	Set

Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

JK Flip-flop

T	$Q(t+1)$	
0	$Q(t)$	No change
1	$Q(t)'$	Toggle

Q	Q^+	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

SR Flip-flop

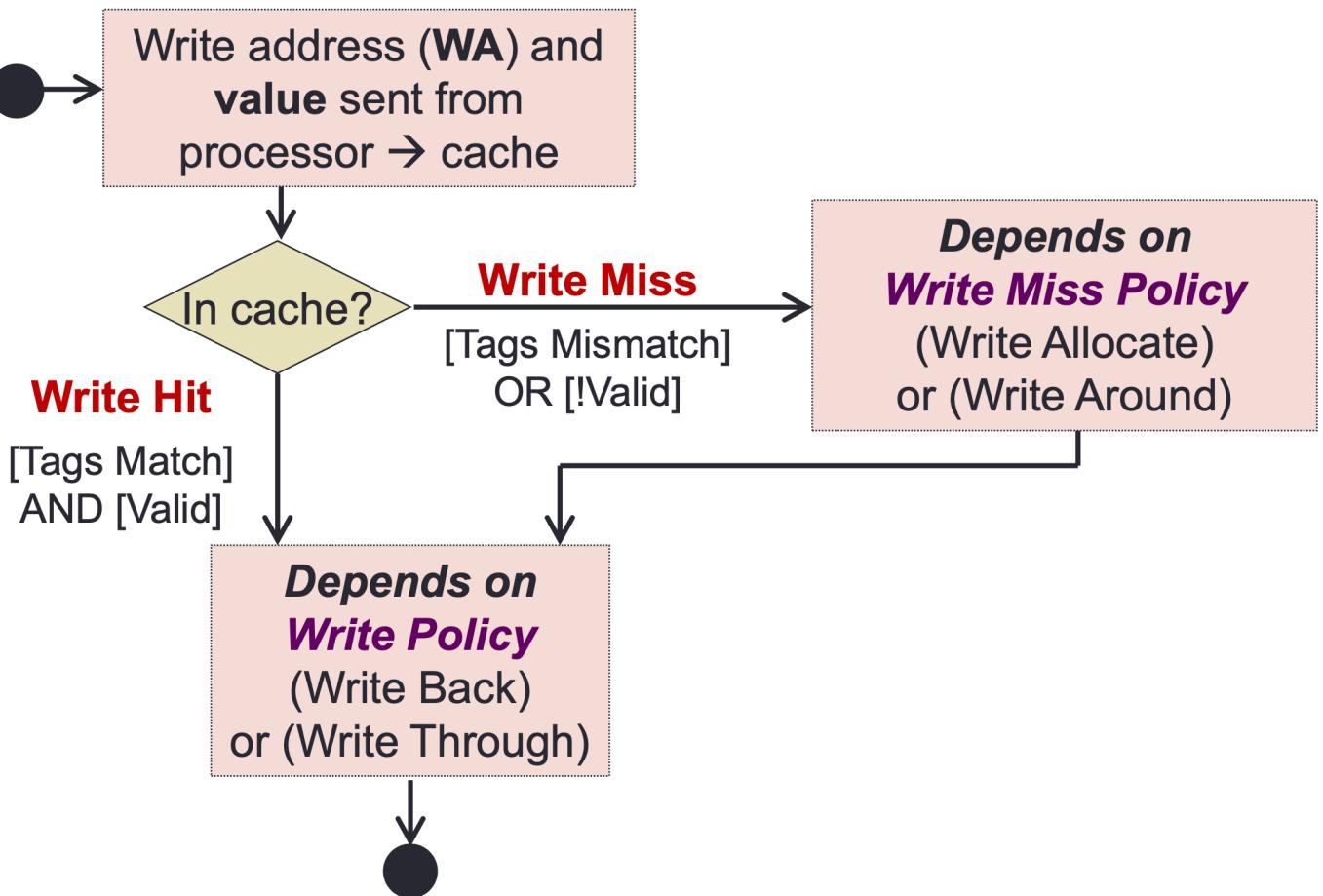
Q	Q^+	D
0	0	0
0	1	1
1	0	0
1	1	1

D Flip-flop

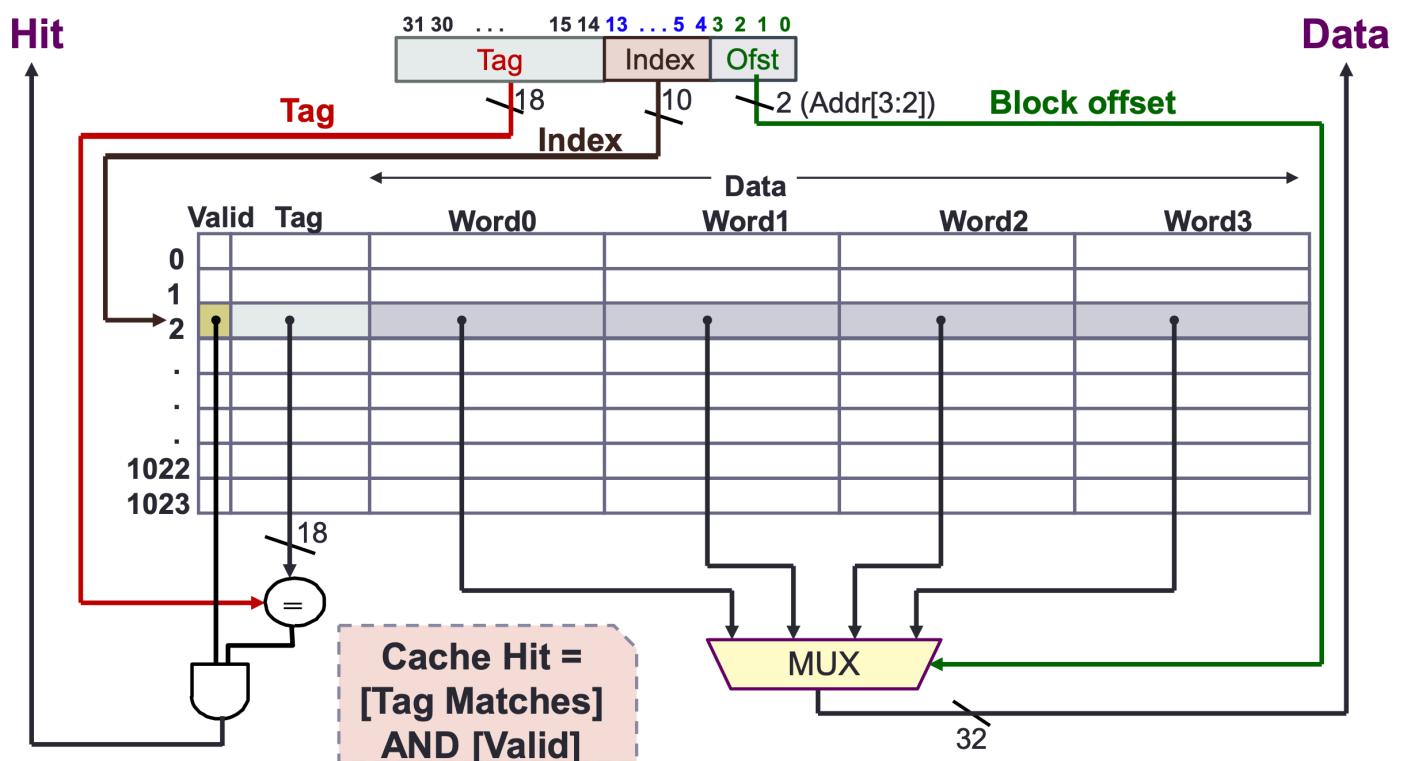
Q	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

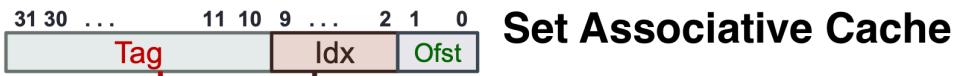
T Flip-flop

Cache

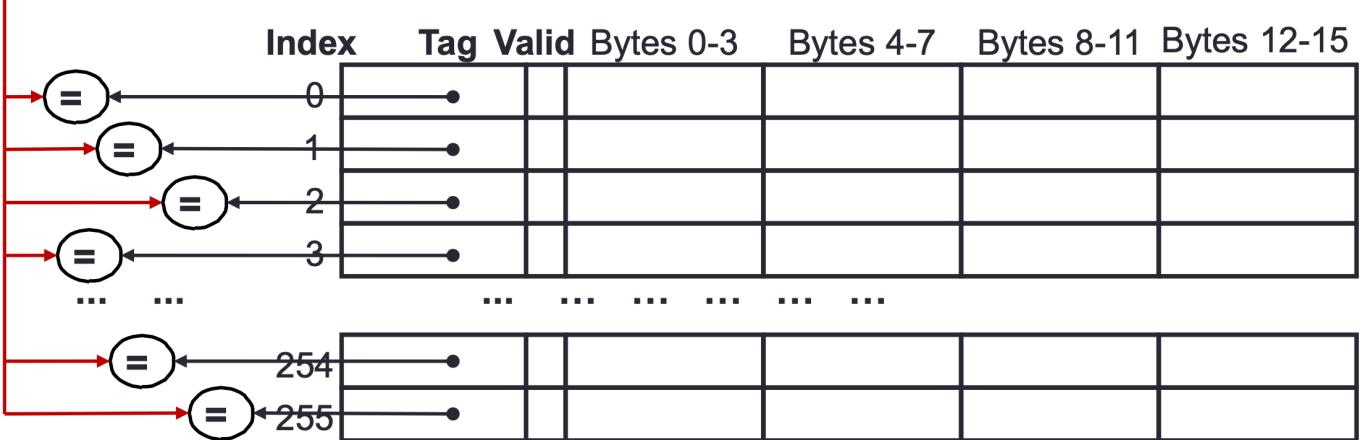


Direct Mapped Cache





Note the simultaneous "search" on all tags of a set.



Miss	Description	Replacement Policy
Compulsory	First access to a block	Least Recently Used
Conflict	Block has been replaced in cache	First In First Out
Capacity	Cache cannot contain all blocks	Random Replacement Least Frequently Used