# **Number Systems**

System	Value	-x	Negation	Addition	Overflow
Sign & Magnitude			Invert first bit		
1s Complement	+ve: same as 2s -ve: 2s + 1	2^n - x - 1	Invert all bits	Ignore MSB carry out	MSB carry in !=  MSB carry out  Result opposite  sign of A and B
2s Complement	if x[n-1]: -= 2^(n- 1) for i in [n-20]: if x[i]: += 2^i	2^n - x	Invert all bits + 1	If MSB carry out: +=1	Result opposite sign of A and B
Excess-n	x-n				
IEEE 754	(Sign) (1.Mantissa) x 2^Exponent		Invert first bit	1: Sign 8: Ex-127 Exp	 23: Mantissa

# MIPS

Operation	RR1	RR2	WR	WD	Opr1	Opr2	Address	Write Data
lw \$a, x(\$b)	\$b	\$a	<b>\$</b> a	Mem([\$b] +x)	[\$b]	Х	[\$b] + x	[\$a]
beq \$a,\$b, immd	\$a	\$b	\$b	?	[\$a]	[\$b]	[\$a] - [\$b]	[\$b]
sub \$a, \$b, \$c	\$b	\$c	\$a	[\$b] - [\$c]	[\$b]	[\$c]	[\$b] - [\$c]	[\$c]
addi \$a, \$b, immd	\$b	\$a	\$a	[\$b] + immd	[\$b]	immd	[\$b] + immd	[\$a]

# MIPS Reference Data



CORE INSTRUCTI	ON SE			OPCODE	
NAME, MNEMO	NIC	FOR- MAT			/ FUNCT (Hex)
Add	add	R	R[rd] = R[rs] + R[rt]	(1)	$0/20_{\text{hex}}$
Add Immediate	addi	I	R[rt] = R[rs] + SignExtImm	(1,2)	8 <sub>hex</sub>
Add Imm. Unsigned	addiu	1	R[rt] = R[rs] + SignExtImm	(2)	9 <sub>hex</sub>
Add Unsigned	addu	R	R[rd] = R[rs] + R[rt]		0 / 21 <sub>hex</sub>
And	and	R	R[rd] = R[rs] & R[rt]		0 / 24 <sub>hex</sub>
And Immediate	andi	I	R[rt] = R[rs] & ZeroExtImm	(3)	c <sub>hex</sub>
Branch On Equal	beq	I	if(R[rs]==R[rt]) PC=PC+4+BranchAddr	(4)	4 <sub>hex</sub>
Branch On Not Equa	bne	I	if(R[rs]!=R[rt]) PC=PC+4+BranchAddr	(4)	$5_{ m hex}$
Jump	j	J	PC=JumpAddr	(5)	2 <sub>hex</sub>
Jump And Link	jal	J	R[31]=PC+8;PC=JumpAddr	(5)	3 <sub>hex</sub>
Jump Register	jr	R	PC=R[rs]		$0/08_{hex}$
Load Byte Unsigned	lbu	I	R[rt]={24'b0,M[R[rs] +SignExtImm](7:0)}	(2)	24 <sub>hex</sub>
Load Halfword Unsigned	lhu	I	R[rt]={16'b0,M[R[rs] +SignExtImm](15:0)}	(2)	25 <sub>hex</sub>
Load Linked	11	I	R[rt] = M[R[rs] + SignExtImm]	(2,7)	$30_{\text{hex}}$
Load Upper Imm.	lui	I	$R[rt] = \{imm, 16'b0\}$		$f_{hex}$
Load Word	lw	Ι	R[rt] = M[R[rs] + SignExtImm]	(2)	nex
Nor	nor	R	$R[rd] = \sim (R[rs] \mid R[rt])$		0 / 27 <sub>hex</sub>
Or	or	R	R[rd] = R[rs]   R[rt]		0 / 25 <sub>hex</sub>
Or Immediate	ori	I	$R[rt] = R[rs] \mid ZeroExtImm$	(3)	
Set Less Than	slt	R	R[rd] = (R[rs] < R[rt]) ? 1 : 0		$0/2a_{hex}$
Set Less Than Imm.	slti	I	R[rt] = (R[rs] < SignExtImm)? 1	: 0(2)	$a_{hex}$
Set Less Than Imm. Unsigned	sltiu	I	R[rt] = (R[rs] < SignExtImm) $? 1:0$	(2,6)	b <sub>hex</sub>
Set Less Than Unsig		R	R[rd] = (R[rs] < R[rt]) ? 1 : 0	(6)	$0/2b_{\text{hex}}$
Shift Left Logical	sll	R	$R[rd] = R[rt] \ll shamt$		0 / 00 <sub>hex</sub>
Shift Right Logical	srl	R	R[rd] = R[rt] >> shamt		0 / 02 <sub>hex</sub>
Store Byte	sb	I	M[R[rs]+SignExtImm](7:0) = R[rt](7:0)	(2)	$28_{\text{hex}}$
Store Conditional	SC	I	M[R[rs]+SignExtImm] = R[rt]; R[rt] = (atomic) ? 1 : 0	(2,7)	38 <sub>hex</sub>
Store Halfword	sh	I	M[R[rs]+SignExtImm](15:0) = R[rt](15:0)	(2)	29 <sub>hex</sub>
Store Word	SW	I	M[R[rs]+SignExtImm] = R[rt]	(2)	
Subtract	sub	R	R[rd] = R[rs] - R[rt]	(1)	$0/22_{\text{hex}}$
Subtract Unsigned	subu	R	R[rd] = R[rs] - R[rt]		$0/23_{hex}$
<ul> <li>(1) May cause overflow exception</li> <li>(2) SignExtlmm = { 16{immediate[15]}, immediate }</li> <li>(3) ZeroExtlmm = { 16{1b'0}, immediate }</li> <li>(4) BranchAddr = { 14{immediate[15]}, immediate, 2'b0 }</li> <li>(5) JumpAddr = { PC+4[31:28], address, 2'b0 }</li> <li>(6) Operands considered unsigned numbers (vs. 2's comp.)</li> <li>(7) Atomic test&amp;set pair; R[rt] = 1 if pair atomic, 0 if not atom</li> </ul>				2'b0 }	

#### **BASIC INSTRUCTION FORMATS**

R	opcode	rs	rt	rd	shamt	funct
	31 26	25 21	20 16	15 1	1 10 6	5 0
1	opcode	rs	rt		immediate	
	31 26	25 21	20 16	15		0
J	opcode			address		
	31 26	25				

#### ARITHMETIC CORE INSTRUCTION SET

			•	/ FMT /FT
	1	FOR-	•	/ FUNCT
NAME, MNEMO	ONIC	MAT	OPERATION	(Hex)
Branch On FP True	bc1t	FI	if(FPcond)PC=PC+4+BranchAddr (4)	11/8/1/
Branch On FP False	bclf	FI	if(!FPcond)PC=PC+4+BranchAddr(4)	11/8/0/
Divide	div	R	Lo=R[rs]/R[rt]; Hi=R[rs]%R[rt]	0///1a
Divide Unsigned	divu	R	Lo=R[rs]/R[rt]; Hi=R[rs]%R[rt] (6)	0///1b
FPAdd Single	add.s	FR	F[fd] = F[fs] + F[ft]	11/10//0
FP Add	add.d	FR	${F[fd],F[fd+1]} = {F[fs],F[fs+1]} +$	11/11//0
Double	add.d	II	$\{F[ft],F[ft+1]\}$	11/11//0
FP Compare Single	c.x.s*	FR	FPcond = (F[fs] op F[ft])? 1:0	11/10//y
FP Compare	c.x.d*	FR	$FPcond = ({F[fs],F[fs+1]}) op$	11/11//y
Double			$\{F[ft],F[ft+1]\}\)?1:0$	11/11//
			==, <, or <=) ( y is 32, 3c, or 3e)	
FP Divide Single	div.s	FR	F[fd] = F[fs] / F[ft]	11/10//3
FP Divide	div.d	FR	${F[fd],F[fd+1]} = {F[fs],F[fs+1]} /$	11/11//3
Double			{F[ft],F[ft+1]}	
FP Multiply Single	mul.s	FR	F[fd] = F[fs] * F[ft]	11/10//2
FP Multiply	mul.d	FR	${F[fd],F[fd+1]} = {F[fs],F[fs+1]} *$	11/11//2
Double			{F[ft],F[ft+1]}	
FP Subtract Single	sub.s	FR	F[fd]=F[fs] - F[ft]	11/10//1
FP Subtract	sub.d	FR	${F[fd],F[fd+1]} = {F[fs],F[fs+1]} -$	11/11//1
Double	Jub.u	100	$\{F[ft],F[ft+l]\}$	
Load FP Single	lwcl	I	F[rt]=M[R[rs]+SignExtImm]  (2)	31//
Load FP	ldcl	I	F[rt]=M[R[rs]+SignExtImm]; (2)	35///
Double	1401		F[rt+1]=M[R[rs]+SignExtImm+4]	331 1 1
Move From Hi	mfhi	R	R[rd] = Hi	0 ///10
Move From Lo	mflo	R	R[rd] = Lo	0 ///12
Move From Control	mfc0	R	R[rd] = CR[rs]	10 /0//0
Multiply	mult	R	$\{Hi,Lo\} = R[rs] * R[rt]$	0///18
Multiply Unsigned	multu	R	$\{Hi,Lo\} = R[rs] * R[rt] $ (6)	0///19
Shift Right Arith.	sra	R	R[rd] = R[rt] >>> shamt	0///3
Store FP Single	swcl	I	M[R[rs]+SignExtImm] = F[rt] (2)	39//
Store FP	sdcl	1	M[R[rs]+SignExtImm] = F[rt]; (2)	3d///
Double	suci	1	M[R[rs]+SignExtImm+4] = F[rt+1]	Ju///

#### FLOATING-POINT INSTRUCTION FORMATS

FR	opcode	fmt	ft	fs	fd	funct
	31 26	25 2	1 20	16 15	11 10	5 5 0
FI	opcode	fmt	ft		immediat	te
	31 26	25 2	1 20	16 15		0

#### **PSEUDOINSTRUCTION SET**

NAME	MNEMONIC	OPERATION
Branch Less Than	blt	if(R[rs] < R[rt]) PC = Label
Branch Greater Than	bgt	if(R[rs]>R[rt]) PC = Label
Branch Less Than or Equal	ble	$if(R[rs] \le R[rt]) PC = Label$
Branch Greater Than or Equal	bge	$if(R[rs] \ge R[rt]) PC = Label$
Load Immediate	li	R[rd] = immediate
Move	move	R[rd] = R[rs]

#### REGISTER NAME, NUMBER, USE, CALL CONVENTION

NAME	NUMBER	USE	PRESERVEDACROSS
NAME	NUMBER	USE	A CALL?
\$zero	0	The Constant Value 0	N.A.
\$at	1	Assembler Temporary	No
\$v0-\$vl	2-3	Values for Function Results and Expression Evaluation	No
\$a0-\$a3	4-7	Arguments	No
\$t0-\$t7	8-15	Temporaries	No
\$s0-\$s7	16-23	Saved Temporaries	Yes
\$t8-\$t9	24-25	Temporaries	No
\$k0-\$k1	26-27	Reserved for OS Kernel	No
\$gp	28	Global Pointer	Yes
\$sp	29	Stack Pointer	Yes
\$fp	30	Frame Pointer	Yes
\$ra	31	Return Address	Yes

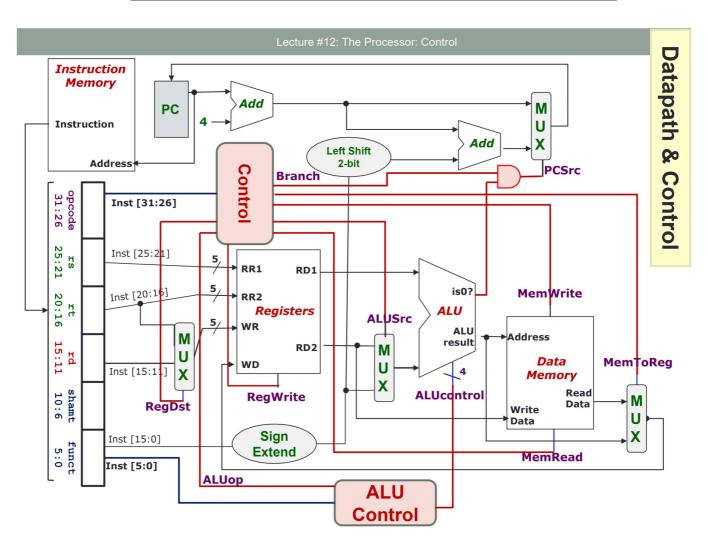
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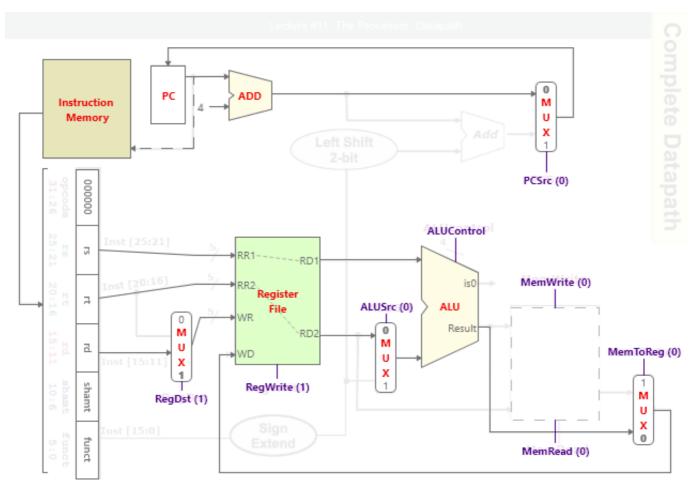
## **Control Design: Outputs**

	BogDat	ALUSrc	MemTo	Reg	Mem	Mem	Branch	ALU	Jop
	RegDst	ALUSIC	Reg	Write	Read	Write	Branch	op1	0qo
R-type	1	0	0	1	0	0	0	1	0
lw	0	1	1	1	1	0	0	0	0
sw	X	1	X	0	0	1	0	0	0
beq	X	0	X	0	0	0	1	0	1

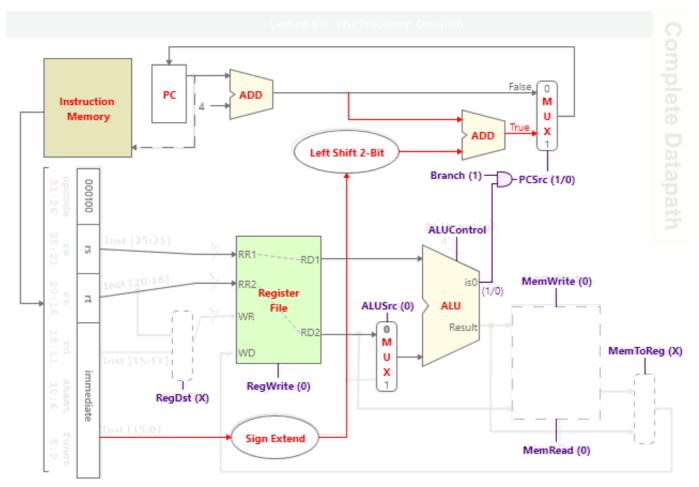
## **Control Design: Inputs**

		Opcode ( Op[5:0] == Inst[31:26] )							
	Op5	Op4	Op3	Op2	Op1	Op0	Value in Hexadecimal		
R-type	0	0	0	0	0	0	0		
lw	1	0	0	0	1	1	23		
sw	1	0	1	0	1	1	2B		
beq	0	0	0	1	0	0	4		

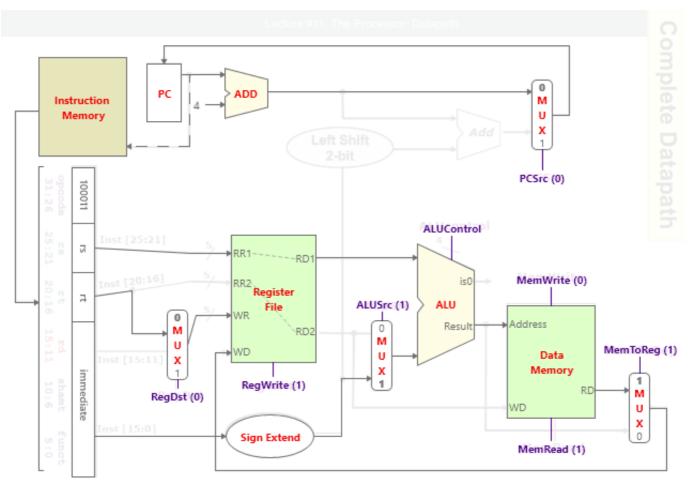




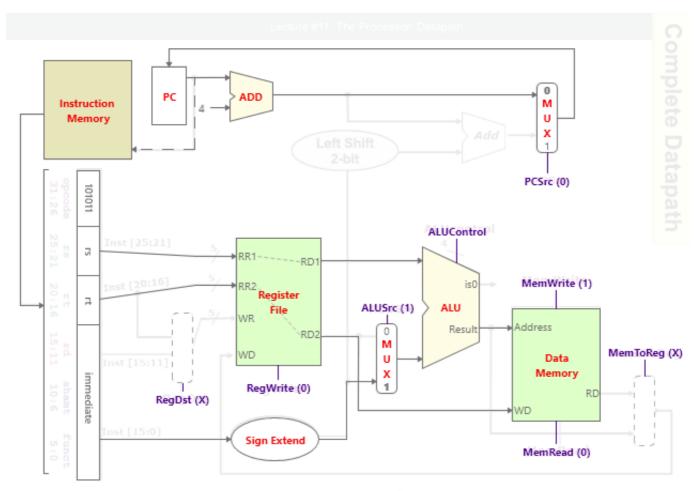
Add



BEQ



Load Word



Store Word

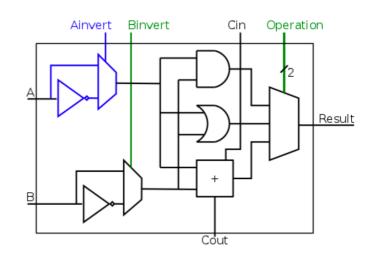
Opcode	ALUop	Instruction Operation	Funct field	ALU action	ALU control
lw	00	load word	XXXXXX	add	0010
sw	00	store word	XXXXXX	add	0010
beq	01	branch equal	XXXXXX	subtract	0110
R-type	10	add	10 0000	add	0010
R-type	10	subtract	10 0010	subtract	0110
R-type	10	AND	10 0100	AND	0000
R-type	10	OR	10 0101	OR	0001
R-type	10	set on less than	10 1010	set on less than	0111

Instruction Type	ALUop
lw / sw	00
beq	01
R-type	10

Function	ALUcontrol
AND	0000
OR	0001
add	0010
subtract	0110
slt	0111
NOR	1100

Generation of 2-bit **ALUop** signal will be discussed later

ALUcontrol			Formation
Ainvert	Binvert	Operation	Function
0	0	00	AND
0	0	01	OR
0	0	10	add
0	1	10	subtract
0	1	11	slt
1	1	00	NOR



## Links

Hexadecimal to Float Hexadecimal-Binary-Decimal XOR

Bitwise Calculator
Instructions to Hexadecimal