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Zedboard - Create a PlanAhead Project with Embedded Processor

EDIT: Git repo of this project can be found here: https://github.com/zynqgeek/zed_helloworld - enjoy!

To take advantage of any aspect of Zynq's configurable FPGA fabric we are going to need to learn how to use PlanAhead, and specifically how to create a new PlanAhead project with an embedded processor within it.

Giving credit where credit is due. I used the document in this example project from zedboard.org as my reference when doing this post:

<http://zedboard.org/node/95> - Thanks to the author!

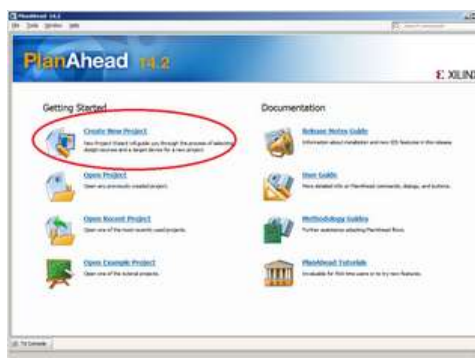
First, make sure you have the tools downloaded and licensed. You can read a how-to post [here](#).

The first we are going to launch is PlanAhead. Go ahead and open up PlanAhead from the state menu. Note: I am using version 14.2 of the tools.

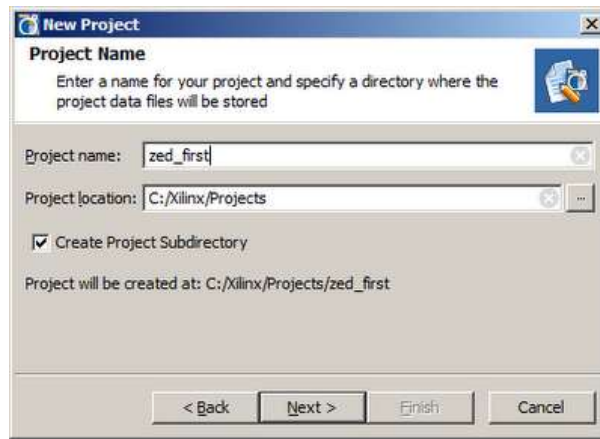


Note: If you are not on a x64 based machine, you should not be using the x64 version of the tools. Launch the PlanAhead(32-bit) version.

Once PlanAhead starts we want to click "Create New Project".



A wizard will pop up with some information. Click Next to get to the screen where you will name your project and decide where it will live.

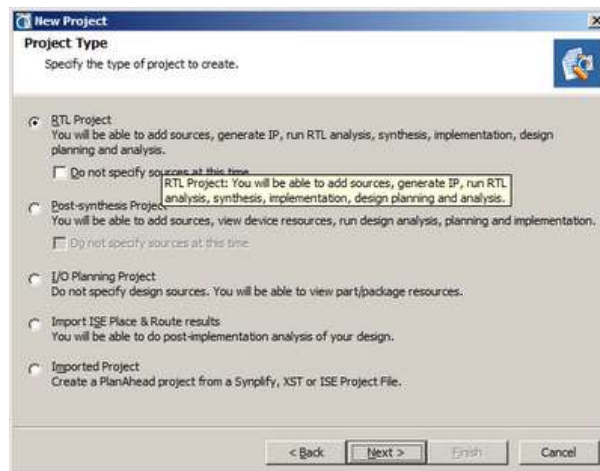


You need to remember two rules about naming projects, and placing them on your computer:

Directory length can not exceed 255 characters

No spaces are allowed in directory or file names

Don't break those two rules, and you can put your files anywhere you want :D.

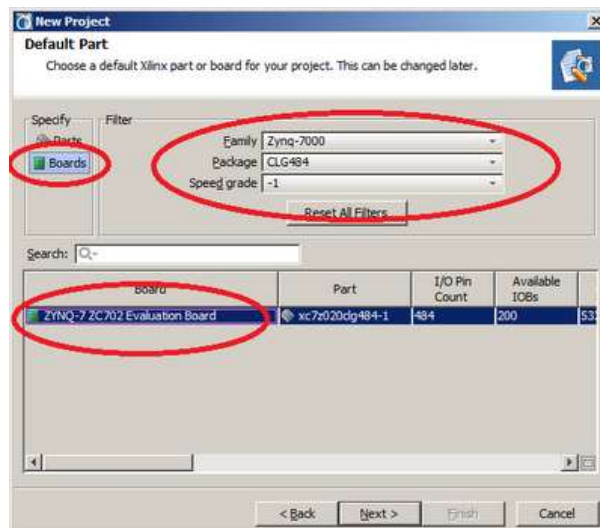


On the next screen we are presented with various different types of projects. In this case we are going to be writing picking a RTL project. More on what all these mean in a future blog post :D

On the next three screens we have the ability to add source files, existing IP (intellectual property blocks), and/or constraint files we may have. We have no need to do any of these things so just keep clicking next until you get to the Part Selection page. On the left side you will see two selectable options "Parts" and "Boards".

Now, Avnet hasn't released their board definition files for the Xilinx tools yet. They will include them in future releases of the tools though, don't worry. Today, though, we need to kind of hack something together using the Xilinx ZC702 board as our base configuration which we will then change. Not too bad, I promise.

Click "Boards" on the left hand side.



Change the three pull down options to these:

Family: Zynq-7000

Package: CLG484

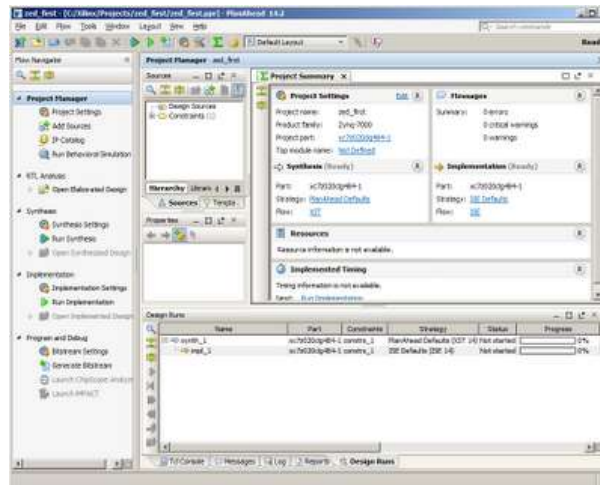
Speed grade: -1

In the list at the bottom of the window you will see the "Zynq-7 ZC702 Evaluation Board" as an option. Select it and hit Next.

Note: when this changes, I will stop back here and update the blog.

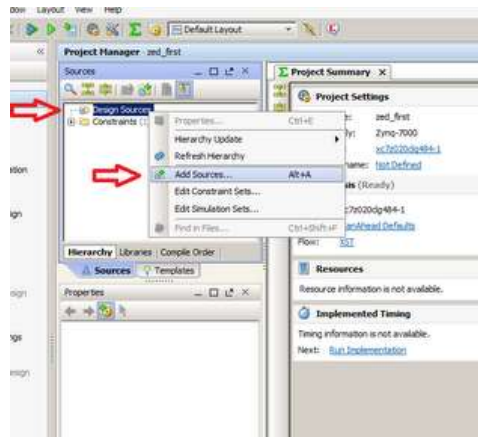
On the last page there is a brief summary of what you have selected throughout the wizard. Review it and click Finish.

PlanAhead will take a moment to create your project, and then display the default view. It should look something like this:



Now that we have PlanAhead launched and our project created, we will need to add our embedded processor to the design.

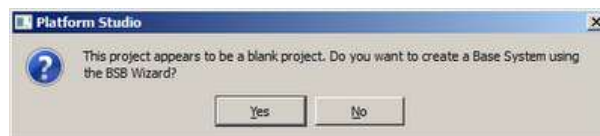
In the Sources Window Pane find the "Design Sources" folder and right mouse click on it. In that menu select "Add Sources ...".



A window with several options on it will pop up. One of the options in the list is "Add or Create Embedded Sources". This option will allow us to add the ARM subsystem to our design. Select this option and click next.

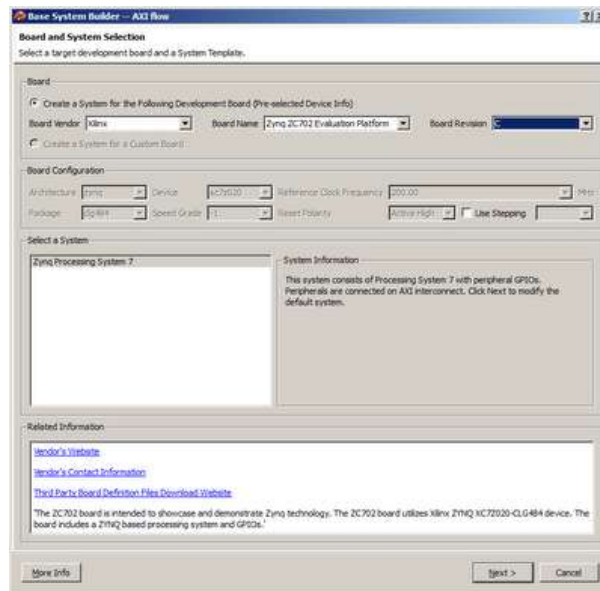
A window with two buttons below a listview will show up. The two buttons are "Add Sub-Design ..." and "Create Sub-Design". Since we do not have one created yet, we will click "Create Sub-Design". A small window will pop up asking what you would like to call your sub-system. I called mine "proc_module". That's it. Click Finish. A progress bar window will pop up and inform you that it is creating the Xilinx Platform Studio (XPS) project for your new sub system. XPS will then be launched (if you don't think it got launched, check your task bar - it might have launched in the background).

XPS will ask you this question:



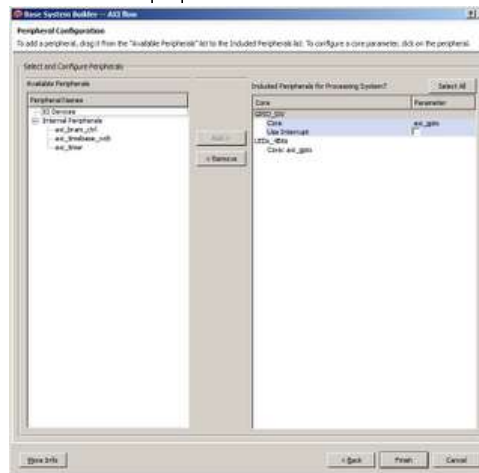
We want to use as many Wizards as possible for our first few designs until we become comfortable with the Xilinx tools, so click Yes.

A window will come up that is the beginning of the wizard. There is an option for an AXI based design or PLB. You will notice that the PLB option is grayed out. This is because the ARM sub system within Zynq uses the AXI standard to talk to it's peripherals, not the rather antiquated PLB standard. Select AXI (not that you have a choice) and click Next.



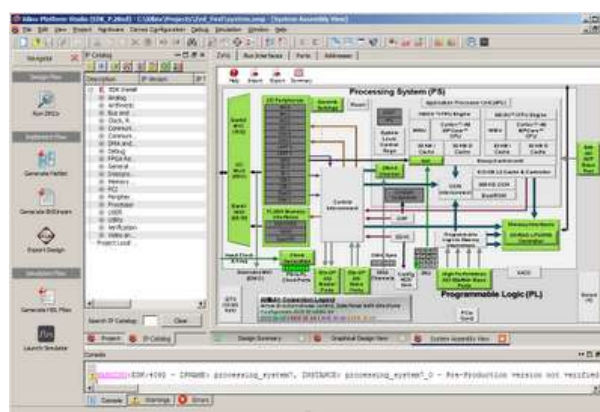
At the time of this post being written, Avnet's Zedboard isn't yet an option within the Board Selection portion of the wizard. What is available is the Xilinx ZC702 board. What we are going to do is pick this board, and then import the specific configuration for the Zedboard after the wizard is complete. Select the ZC702 board from the list, and click Next.

The next screen is where we will select what internal and external peripherals we want to use within our design.



In this particular case, we are going to just go with the defaults and move past this. This is mostly because these are the available peripherals for the ZC702 board, not the Zedboard. Click Finish.

The wizard will turn away on the configuration you have given it, and after a minute will return back to the XPS GUI, where the System Assembly View will be visible.



Ok, since we targeted the ZC702 board and not the Zedboard, we need to import the correct peripheral configuration file. This file can be downloaded here: http://zedboard.com/misc/files/zedboard_RevC_v1.xml

~~EDIT: An update has been posted to the Board Definition File.~~

http://zedboard.org/sites/default/files/documentations/zedboard_RevC_v2.xml

EDIT: bad link - updated. Thanks Jan for pointing it out!

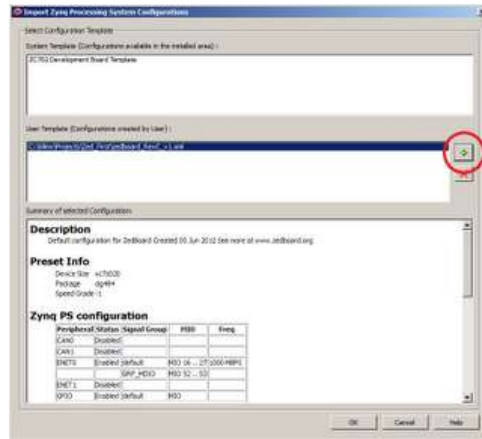
http://zedboard.org/sites/default/files/documentations/zedboard_RevC_v2_XML.zip

I have placed this file in the root directory of my project (same place as `system.xmp`). This file is an XML file (go ahead and open it up and take a look if you would like) which contains all of the information needed to configure the ARM sub-system of the Zynq device. Specifically in our case we will only have certain peripherals pulled out to the outside world, so we need to tell the device this.

Once you have downloaded the Board Definition File and saved it to your project directory, find the "Import" icon above the System Assembly View PS view.



A screen will pop up that is important to take a second to talk about. Once Xilinx start distributing the Board Support files with their software tools this window will have the Zedboard as a selectable item in the list of available boards (actually the process to get to this point will be completely different, but for now we will do it this way). Since we aren't there yet, we need to click the + sign on this window and browse to our .xml file.



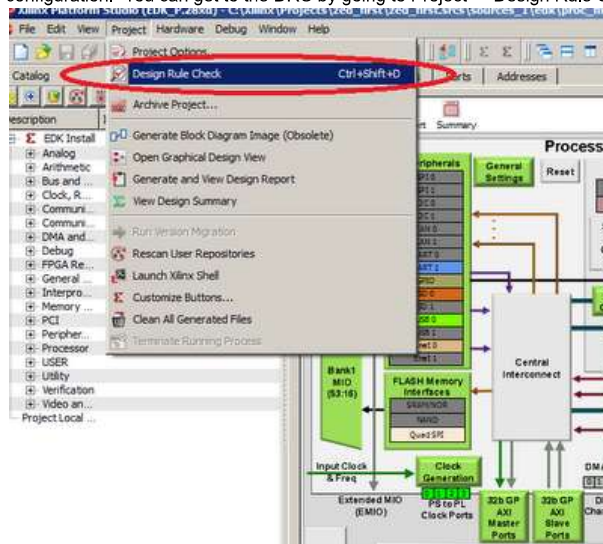
Once you have your file selected in the second window you can click OK. A message box will ask if you are sure you want to continue, if you are hit Yes.

EDK will load up the new configuration and after a few seconds it will show the updated System Assembly View. This configuration will set all of the various registers that are associated with the various parts of the ARM sub system, including peripherals with shared IO pins.

Note: I am going to a full blog post on what this view means. I have not yet, so poke around a bit and see what some of the different settings are.

Ok, take a deep breath. There is a lot going on here, and once you go through it a few times and start exploring what everything means you will feel better. Let's move on and get a simple Hello World example running.

First, let's make sure we've done everything correctly up to this point. We can do this by running a Design Rule Check. This will run a series of scripts that will tell us if we have any errors with our configuration. You can get to the DRC by going to Project -> Design Rule Check within XPS.

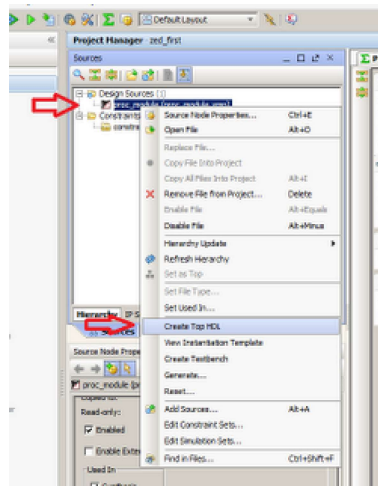


If there are no errors, then you've got it right up to this point, congratz! We can close XPS, we have done everything we need to here. Once XPS is closed, PlanAhead should be available to use again.

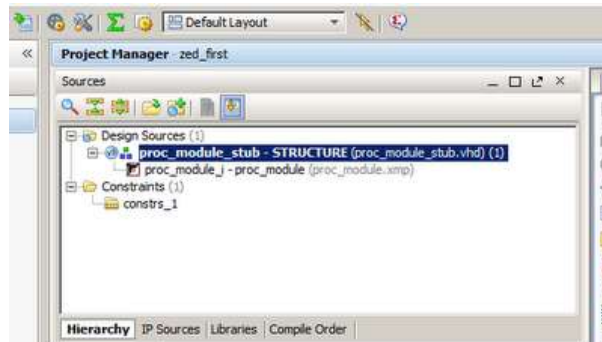
Now let me take a moment to let you all know that in the world of FPGA's there is a lot of Religion ... a LOT. There are "A" users, and "X" users (I'll let you figure that out on your own ..), and there are Verilog users and VHDL users. I happen to be an X and VHDL user - you know, because I only use the best ;D. I will be continuing my example using VHDL. If you choose to use Verilog go for it, you might be on your own with a few things though (But I am sure you will be able to get it!). As for you "A" users out there ... keep using your soft cores and co-processors, we'll be over here at the bleeding edge ;).

Note: To switch to/from Verilog or VHDL, click the "Project Settings" button under the "Project Manager" tree item on the left side of your screen (within the Flow Navigator). From the window that opens up you can choose Verilog or VHDL from the Target Language combo box.

Once you are done picking your preferred language you can right mouse click on your .xmp file. Mine was called proc_module.xmp. Select "Create Top HDL".



This will create a Human Readable file that is in VHDL that is the instantiation of the processor system. PlanAhead is creating this wrapper to instantiate the .xmp file that describes our processor system.



This file is really nice once you get into larger projects that might require you to add additional logic between your top level instantiation and your processor system. For now we will leave it unmodified.

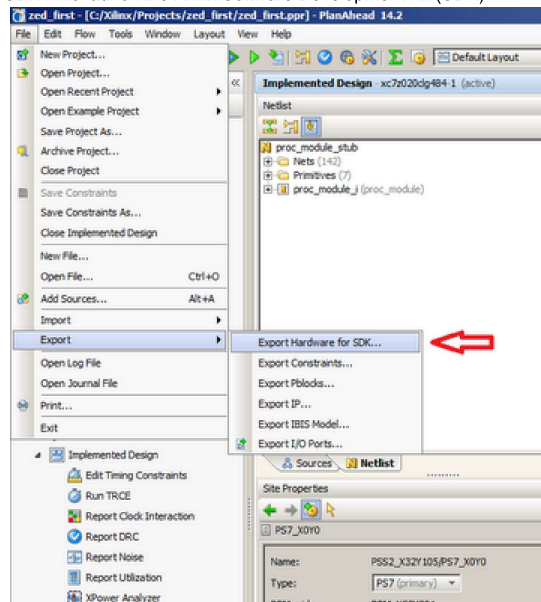
Well, that's ... we have our base system with just the processor sub system instantiated (that is that nothing from the Programmable Logic (PL) portion of the Zynq device is being used by custom code. Next, we need to create a bit file that will be used to program our Zed board.

On the left side in the Flow Navigator view click the "Generate Bitstream" option under Program and Debug. This is going to take a few minutes to run, as it is doing a lot of things. You may get a window that pops up that displays some warnings about unused pads. Click OK to close that window.

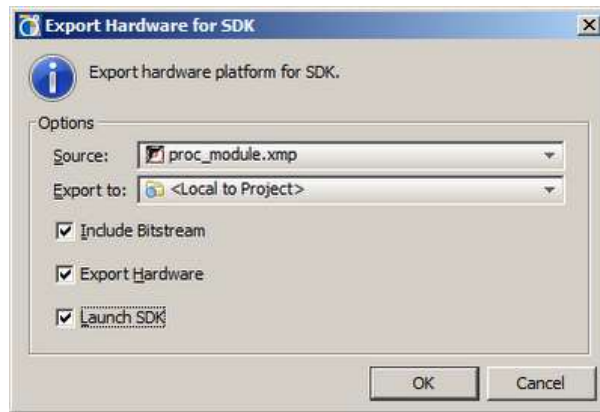
Once this is complete a small little window will pop up that asks what you would like to view now that the bit file is created. I like looking at the reports, but you can pick anything you would like. We are not quite ready to program our board, so don't load iMPACT quite yet.

Now that we have our full hardware system described, we can write some code for it! woohoo!

Go to File -> Export -> Export Hardware for SDK ... to launch the Xilinx Software Development Kit (SDK).



A little window will come up with some options. Make sure you click all three check boxes to Include the bitstream, export the hardware, and launch SDK. Click OK to launch SDK to start writing some code.



It will take a bit to export everything, but eventually SDK opens.

To continue getting the code written for the this project [go here](#).

You have created a PlanAhead project with an embedded ARM processor in it! That's so awesome!

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thanks!

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Avnet workaroud

Permalink Submitted by bartvolkaerts on Wed, 2012-11-07 08:59.

In the new Xilinx ISE (14.3) Avnet's board definition is implemented! The workaround (loading the xml - peripheral configuration file) is not necessary anymore.

Time to update the blog! ;-)

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