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Zynq-7000 SoC Product Selection Guide





Zynd®-7000 SoC Family

Single-Core				J	Cost-Optimized Devices	zed Devices				Mid-Ran	Mid-Range Devices	
Part Number XC720075 XC72012 Single-Co Processor Extensions L1 Cache On-Chip Memory External Memory Support ⁽²⁾ External Static Memory Support ⁽²⁾ DMA Channels Peripherals		Device Name	Z-7007S	Z-7012S	Z-7014S	Z-7010		Z-7020	Z-7030	Z-7035	Z-7045	Z-7100
Processor Core Processor Core ARM® Cortex**-A9 Up to 766N L1 Cache Con-Chip Memory External Memory Support(2) External Static Memory Support(2) Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only) 7 Series PL Equivalent Logic Cells Look-Up Tables (LUTs) Look-Up Tables (LUTs) Look-Up Tables (LUTs) Analog Mixed Signal (AMS) / XADC(2) Security(3) Security(3) Figh 14,400 Figh 2.5Mb (# 36Kb Block RAM) BOSP Slices Commercial Speed Grades Extended -12.		Part Number	XC7Z007S	XC7Z012S	XC7Z014S	XC7Z010	XC7Z015	XC7Z020	XC7Z030	XC7Z035	XC7Z045	XC7Z100
Processor Core District Context				Single-Core		חם	Jal-Core AR	Σ		Dual-C	Dual-Core ARM	
Processor Extensions 11 Cache 12 Cache On-Chip Memory External Memory Support ⁽²⁾ External Static Memory Support ⁽²⁾ External Static Memory Support ⁽²⁾ Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only) 7 Series PL Equivalent Artix®-7 Logic Cells 23K 55K Look-Up Tables (LUTs) 14,400 7 Series PL Equivalent Artix®-7 Artix-7 Logic Cells 23K 55K Look-Up Tables (LUTs) 14,400 7 Series PL Equivalent Artix®-7 Artix-7 Logic Cells 23K 55K Commercial Security ⁽³⁾ Analog Mixed Signal (AMS) / XADC ⁽²⁾ Security ⁽³⁾ Commercial 1.2.2 Speed Grades Extended -12		Processor Core		ırtex™-A9 N	1PCore™	Con	tex-A9 MPC	ore		Cortex-A	Cortex-A9 MPCore	
L1 Cache L2 Cache On-Chip Memory External Memory Support ⁽²⁾ External Static Memory Support ⁽²⁾ Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only) 7 Series PL Equivalent Look-Up Tables (LUTs) Look-Up Tables (LUTs) Total Blocks) (# 36kb Blocks) PCI Express® Analog Mixed Signal (AMS) / XADC ⁽²⁾ Security ⁽³⁾ Commercial Commercial Speed Grades Extended 1.2.2 Commercial -12			Ŋ	p to 766MH	z	'n	р to 866МҺ	Z		Up to	Up to $1GHz^{(1)}$	
L1 Cache L2 Cache On-Chip Memory External Memory Support ⁽²⁾ External Static Memory Support ⁽²⁾ External Static Memory Support ⁽²⁾ Peripherals Peripherals Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only) 7 Series PL Equivalent Artix®-7 Artix-7 Cook-Up Tables (LUTs) Look-Up Tables (LUTs) Look-Up Tables (LUTs) Total Block RAM Hip-Flops BOSP Slices Analog Mixed Signal (AMS) / XADC ⁽²⁾ Security ⁽³⁾ Commercial Commercial Speed Grades Extended -12	(Sc	Processor Extensions		Z	EON™ SIMI) Engine an	d Single/Do	uble Precisi	on Floating Pc	int Unit per pi	rocessor	
L2 Cache On-Chip Memory External Memory Support ⁽²⁾ External Static Memory Support ⁽²⁾ DMA Channels Peripherals Peripherals Security ⁽³⁾ Security ⁽³⁾ Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only) 7 Series PL Equivalent Artix®-7 Artix-7 Look-Up Tables (LUTs) Look-Up Tables (LUTs) Look-Up Tables (LUTs) Analog Mixed Signal (AMS) / XADC ⁽²⁾ Security ⁽³⁾ Commercial Speed Grades Extended -12	<u>վ</u>) և	L1 Cache				32K	B Instructio	n, 32KB Dat	a per processi	or		
External Memory Support ⁽²⁾ External Static Memory Support ⁽²⁾ DMA Channels Peripherals Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only) 7 Series PL Equivalent Artix®-7 Artix-7 Look-Up Tables (LUTs) 14,400 34,400 Flip-Flops 28,800 68,800 Total Block RAM 1.8Mb 2.5Mb (# 36Kb Blocks) DSP Slices 66 120 PCI Express® — Gen2 x4 Analog Mixed Signal (AMS) / XADC ⁽²⁾ Security ⁽³⁾ Commercial Speed Grades Extended -12	uəţ	L2 Cache						512KB				
External Memory Support ⁽²⁾ External Static Memory Support ⁽²⁾ Peripherals Peripherals Peripherals Peripherals Security ⁽³⁾ Security ⁽³⁾ Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only) 7 Series PL Equivalent Artix®-7 Artix-7 Logic Cells 23K 55K Look-Up Tables (LUTs) 14,400 8,800 Flip-Flops 18,800 68,800 Flip-Flops 18,800 68,800 Fotal Block RAM 1.8Mb 2.5Mb (# 36Kb Blocks)	s/s	On-Chip Memory						256KB				
External Static Memory Support ⁽²⁾ DMA Channels Peripherals Peripherals Security ⁽³⁾ Processing System to Programmable Logic Interface Ports (Primary Interface & Interrupts Only) 7 Series PL Equivalent Logic Cells 23K 55K Look-Up Tables (LUTs) 14,400 78,800 88,800 Flip-Flops 78,800 68,800 72) DSP Slices 66 120 PCI Express® — Gen2 x4 Analog Mixed Signal (AMS) / XADC ⁽²⁾ Security ⁽³⁾ Security ⁽³⁾ Security ⁽³⁾ Speed Grades Extended 11-2	g Bu	External Memory Support ⁽²					DDR3, DI	DR3L, DDR2,	, LPDDR2			
Peripherals Peripherals Peripherals Security ⁽³⁾ Processing System to Programmable Logic Interface Ports (Primary Interface & Interrupts Only) 7 Series PL Equivalent Artix®-7 Artix-7 Logic Cells 23K 55K Look-Up Tables (LUTs) 14,400 34,400 Flip-Flops 28,800 68,800 Flip-Flops (Bocks) (72) DSP Slices Analog Mixed Signal (AMS) / XADC ⁽²⁾ Security ⁽³⁾ Security ⁽³⁾ Speed Grades Extended -12	ijss	External Static Memory Support ⁽²					2x Qua	d-SPI, NAN	D, NOR			
Peripherals Peripherals w/ built-in DMA ⁽²⁾ Security ⁽³⁾ Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only) 7 Series PL Equivalent Artix®-7 Artix-7 Logic Cells 23K 55K Look-Up Tables (LUTs) 14,400 34,400 Flip-Flops 28,800 68,800 Flip-Flops 28,800 68,800 PCI Express® — Gen2 x4 Analog Mixed Signal (AMS) / XADC ⁽²⁾ Security ⁽³⁾ Security ⁽³⁾ Speed Grades Extended -12	9 00	DMA Channels					8 (4	dedicated to	o PL)			
Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only) 7 Series PL Equivalent Artix®-7 Artix-7 Logic Cells 23K 55K Look-Up Tables (LUTs) 14,400 34,400 Flip-Flops 28,800 68,800 Flip-Flops 28,800 68,800 PCI Express® — Gen2 x4 Analog Mixed Signal (AMS) / XADC ⁽²⁾ Security ⁽³⁾ Speed Grades Extended -12	ЛЧ	Peripherals				2x UAR	T, 2x CAN 2	.0B, 2x I2C,	2x SPI, 4x 32b	GPIO		
Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only) 7 Series PL Equivalent Logic Cells 23K 55K Look-Up Tables (LUTs) 14,400 34,400 Flip-Flops 28,800 68,800 Total Block RAM 1.8Mb 2.5Mb (# 36Kb Blocks) (50) (72) DSP Slices 66 120 PCI Express® — Gen2 x4 Analog Mixed Signal (AMS) / XADC ⁽²⁾ Speed Grades Extended -2 Industrial -12		Peripherals w/ built-in DMA ⁽²			2	x USB 2.0 ((OTG), 2x Tri	-mode Gigal	bit Ethernet, 2	OIGS/GS X		
Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only) 7 Series PL Equivalent Logic Cells 23K 55K Look-Up Tables (LUTs) 14,400 74,400 75K 119-Flops 18,800 72,800 73,800 74,800 74,800 75		Security ⁽³			AES	RSA A and SHA 25	outhentication (1997)	on of First Sion and Autl	tage Boot Loa hentication fo	der, r Secure Boot		
Processing system to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only) 7 Series PL Equivalent Artix®-7 Artix-7 Logic Cells 23K 55K Look-Up Tables (LUTs) 14,400 34,400 Flip-Flops 28,800 68,800 Total Block RAM 1.8Mb 2.5Mb (# 36Kb Blocks) (50) (72) DSP Slices 66 120 PCI Express® — Gen2 x4 Analog Mixed Signal (AMS) / XADC ⁽²⁾ Security ⁽³⁾ Commercial Commercial -12						. •	2x AXI 32b N	Master, 2x A	XI 32b Slave			
(Primary Interfaces & Interrupts Only) 7 Series PL Equivalent Artix®-7 Artix-7 Look-Up Tables (LUTs) 14,400 34,400 Flip-Flops 28,800 68,800 Total Block RAM 1.8Mb 2.5Mb (# 36Kb Blocks) (50) (72) DSP Slices 66 120 PCI Express® — Gen2 x4 Analog Mixed Signal (AMS) / XADC(2) Security(3) -1 Commercial -1 -1 Speed Grades Extended -2 Industrial -12		Processing system to Programmable Logic Interface Ports					4x AXI	64b/32b M	emory			
7 Series PL Equivalent		(Primary Interfaces & Interrupts Only)						AXI 64b ACF	0 (
Speed Grades Commercial C							1.	ייי ב וווכווחסר				
Logic Cells 23K 55K Look-Up Tables (LUTs) 14,400 34,400 Flip-Flops 28,800 68,800 Total Block RAM 1.8Mb 2.5Mb (# 36Kb Blocks) (50) (72) DSP Slices 66 120 PCI Express®		7 Series PL Equivalent		Artix-7	Artix-7	Artix-7	Artix-7	Artix-7	Kintex®-7	Kintex-7	Kintex-7	Kintex-7
Look-Up Tables (LUTs)		Logic Cells		55K	65K	28K	74K	85K	125K	275K	350K	444K
Flip-Flops	(7.	Look-Up Tables (LUTs)		34,400	40,600	17,600	46,200	53,200	78,600	171,900	218,600	277,400
Total Block RAM 1.8Mb 2.5Mb	d) 3	Flip-Flops		68,800	81,200	35,200	92,400	106,400	157,200	343,800	437,200	554,800
(# 36kb Blocks) (50) (72) DSP Slices 66 120 PCI Express® — Gen2 x4 Analog Mixed Signal (AMS) / XADC ⁽²⁾ Security ⁽³⁾ Commercial -1 Speed Grades Extended -2 Industrial -12	igo	Total Block RAIV		2.5Mb	3.8Mb	2.1Mb	3.3Mb	4.9Mb	9.3Mb	17.6Mb	19.2Mb	26.5Mb
Analog Mixed Signal (AMS) / XADC ⁽²⁾ Speed Grades DSP Slices 66 120 PCI Express® — Gen2 x4 Security ⁽³⁾ Commercial -1 Industrial -12	рη ә	(# 36Kb Blocks)	(20)	(72)	(107)	(09)	(62)	(140)	(265)	(200)	(545)	(755)
PCI Express® — Gen2 x4 Analog Mixed Signal (AMS) / XADC ⁽²⁾ Security ⁽³⁾ Commercial -1 Speed Grades Extended -2	IQE	DSP Slices		120	170	80	160	220	400	006	006	2,020
Analog Mixed Signal (AMS) / XADC ⁽²⁾ Security ⁽³⁾ Commercial -1 Speed Grades Extended -2	ะเนเ	PCI Express [®]		Gen2 x4	ı	ı	Gen2 x4	1	Gen2 x4	Gen2 x8	Gen2 x8	Gen2 x8
Security ⁽³⁾ Commercial -1 Speed Grades Extended -2 Industrial -12	ue.	Analog Mixed Signal (AMS) / XADC ⁽²				2x 12 bit,	MSPS ADCs	with up to	17 Differentia	l Inputs		
Speed Grades Extended -2. Industrial -12	IBO.	Security ⁽³		AE	:S & SHA 25	6b Decrypt	ion & Authe	entication fo	r Secure Prog	rammable Log	gic Config	
Extended -2 Industrial -12	٦d	Commercia					-1			-1		-1
-12				-2			-2,-3			-2,-3		-2
= /=		Industria		-1, -2			-1, -2, -1L			-1, -2, -2L		-1, -2, -2L

1. 1 GHz processor frequency is available only for -3 speed grades in Z-7035, and Z-7045 devices. See DS190, Zynq-7000 SoC Overview for details.
2. Z-7007S and Z-7010 in CLG225 have restrictions on PS peripherals, memory interfaces, and I/Os. Please refer to UGS85, Zynq-7000 SoC Technical Reference Manual for more details.
3. Security block is shared by the Processing System and the Programmable Logic.



HR I/O, HP I/O, PS I/O, and Transceivers (GTP or GTX) Zynq®-7000 SoC Family

ackage otprint ⁽¹⁾	ice Name								COLLEGE POLICE		
ackage stprint ⁽¹⁾		Device Name Z-7007S	Z-7012S	Z-7014S	Z-7010	Z-7015	Z-7020	Z-7030	Z-7035	Z-7045	Z-7100
	Dimensions (mm)		А	HR I/O, HP I/O PS I/O ⁽²⁾ , GTP Transceivers	HP I/O Fransceivers				HR I/O, HP I/O PS I/O ⁽²⁾ , GTX Transceivers	HP I/O Transceivers	
CLG400 1	13x13	54, 0 84 ⁽³⁾ , 0			54, 0 84 ⁽³⁾ , 0						
	17×17	100, 0 128, 0		125, 0 128, 0	100, 0 128, 0		125, 0 128, 0				
CLG484 1	19x19			200, 0 128, 0			200, 0 128, 0				
CLG485 ⁽⁴⁾	19×19		150, 0 128, 4			150, 0 128, 4					
SBG485 ⁽⁴⁾ 1	19x19							50, 100 128, 4			
FBG484 2	23x23							100, 63 128, 4			
FBG676 ⁽¹⁾ 2	27x27							100, 150 128, 4	100, 150 128, 8	100, 150 128, 8	
FFG676 ⁽¹⁾ 2	27x27							100, 150 128, 4	100, 150 128, 8	100, 150 128, 8	
FFG900 3	31x31								212, 150 128, 16	212, 150 128, 16	212, 150 128, 16
FFG1156 3	35x35										250, 150 128, 16



Devices in the same package are footprint compatible. FBG676 and FFG676 are also footprint compatible.
 PS I/O count does not include dedicated DDR calibration pins.
 PS DDR and PS MIO pin count is limited by package size. See <u>DS190</u>, *Zynq-7000 SoC Overview* for details.

^{4.} CLG485 and SBG485 are pin-to-pin compatible. See product data sheets and user guides for more details.

See DS190, Zynq-7000 SoC Overview for package details.

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13mm-35mm

PCB Footprint Dimensions (mm)	13x13	17x17	19x19	19x19	23x23	27x27	27x27	31x31	35x35
Unique Footprint	CLG225	CLG400	CLG484	CLG485	FBG484	FBG676	FFG676	FFG900	FFG1156
Z-7007-Z	54, 84, 0	100, 128, 0							
Z-7012S				150, 128, 4					
Z-7014S		125, 128, 0	200, 128, 0						
Z-7010	54, 84, 0	100, 128, 0							
Z-7015				150, 128, 4					
Z-7020		125, 128, 0	200, 128, 0						
0/1	0/136 0/1								

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	128, 16	128, 16	212, 150, 128, 16 250, 150, 128, 16
	212, 150,	212, 150,	212, 150,
100, 150, 128, 4	100, 150, 128, 8 100, 150, 128, 8 212, 150, 128, 16	100, 150, 128, 8 100, 150, 128, 8 212, 150, 128, 16	
100, 150, 128, 4	100, 150, 128, 8	100, 150, 128, 8	
50, 100, 128, 4 100, 63, 128, 4 100, 150, 128, 4 100, 150, 128, 4			
50, 100, 128, 4			
Z-7030	Z-7035	Z-7045	Z-7100

The footprint compatibility range is indicated by shading per column.

Important: Verify all data in this document with the device data sheets found at www.xilinx.com © Copyright 2014–2019 Xilinx





Zynq®-7000 Family Speed Grades

Device Name⁽¹⁾

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2-70075 2-70145 2-70145 2-7010 2-7020 2-7030 2-7035 2-7045 2-7000
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Notes:

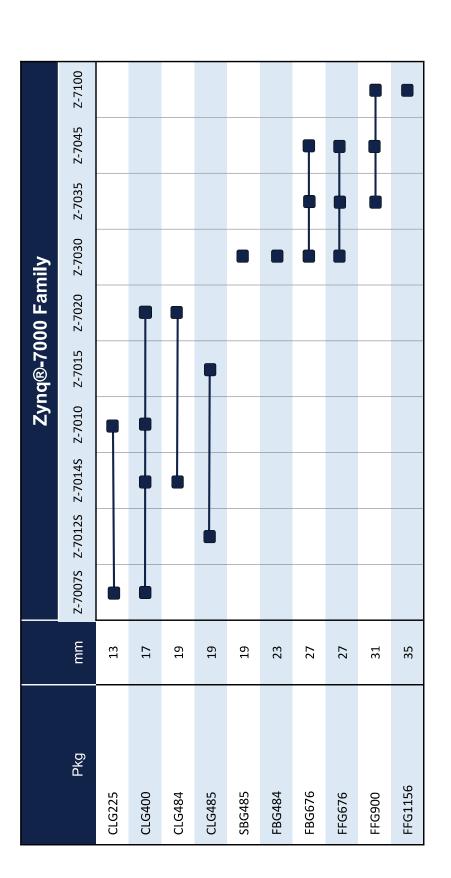
1. For full part number details, see the Ordering Information section in DS190, Zyng®-7000 SoC Overview.

Available

Not offered

C = Commercial (Tj = 0°C to +85°C) E = Extended (Tj = 0°C to +100°C) I = Industrial (Tj = -40°C to +100°C)

Zynd®-7000 Family Device Migration Table

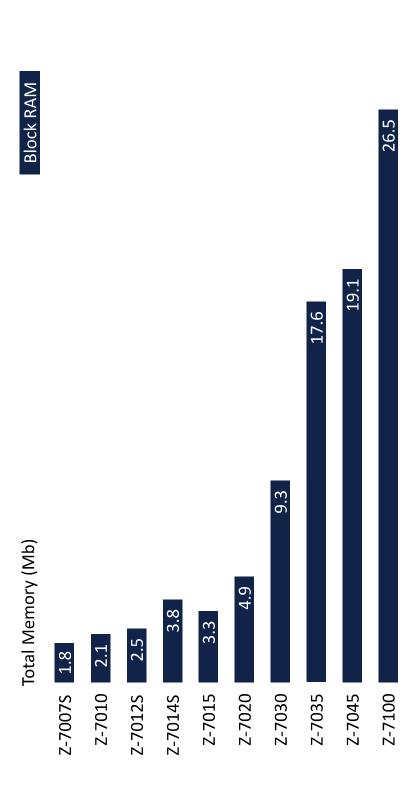




Memory



The Zyng®-7000 family has block RAM (dual-port, programmable, built-in optional error correction).



Transceiver Count and Bandwidth



The serial transceivers in the Zynq-7000 family include the proven on-chip circuits required to provide optimal signal integrity in real-world environments, at data rates up to 6.25Gb/s (GTP) and 12.5Gb/s (GTX).

Total Transceiver Count and Bandwidth

GTX	
GTP	

GTX = 12.5Gb/s

Z-7007S 0

Z-7010 0

Z-7012S

25Gb/s

Z-7014S 0

Z-7015

4 25Gb/s

Z-7020 0

Z-7030

50Gb/s

Z-7035

Z-7045

Z-7100

200Gb/s 16

200Gb/s

16

200Gb/s

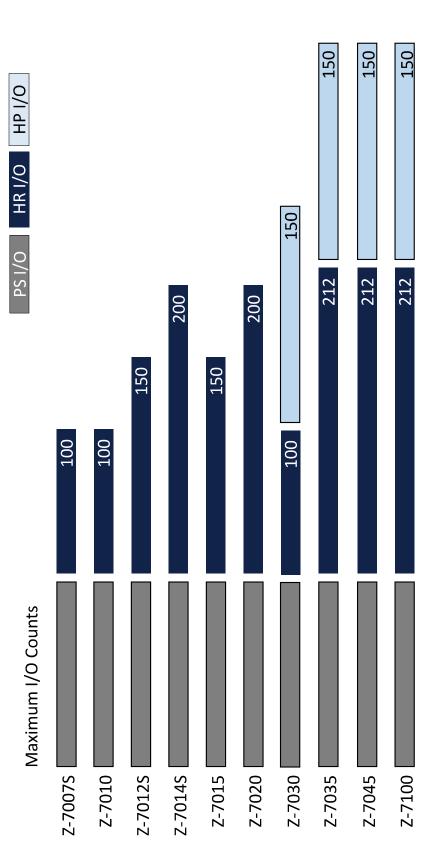
16

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

I/O Count



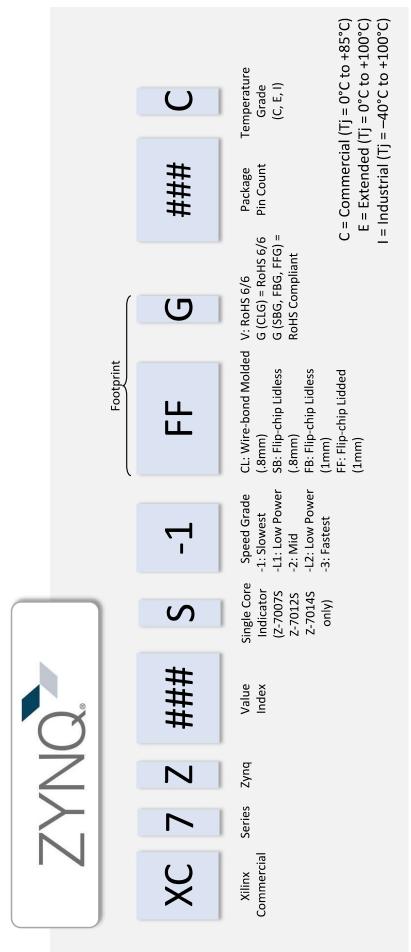
multi-use I/O (MIO), which support 1.8V to 3.3V standards. The HR I/Os are reduced-feature I/Os, providing voltage The I/Os are classified as PS I/O, high-range (HR) I/O, and high-performance (HP) I/O. The PS I/Os are composed of support from 1.2V to 3.3V. The HP I/Os are optimized for highest performance operation, from 1.2V to 1.8V.



1. The PS I/O count is composed of 54 I/Os (excluding DDR interface), which are used to communicate to external components, referred to as multiplexed I/O (MIO).

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

Zynq®-7000 Family Device Ordering Information



Refer to DS190, Zyng-7000 SoC Overview for additional information.



References

DS190, Zynq®-7000 SoC Overview

DS187, Zynq-7000 SoC (Z-7007S, Z-7012S, Z-7014S, Z-7010, Z-7015, and Z-7020): DC and AC Switching Characteristics

DS191, Zynq-7000 SoC (Z-7030, Z-7035, Z-7045, and Z-7100):DC and AC Switching Characteristics

DS176, Zynq-7000 SoC and 7 Series Devices Memory Interface Solutions (v4.0)

UG585, Zynq-7000 SoC Technical Reference Manual

UG865, Zynq-7000 SoC Packaging and Pinout Product Specification

UG471, 7 Series FPGAs SelectIO™ Resources User Guide

UG472, 7 Series FPGAs Clocking Resources User Guide

UG473, 7 Series FPGAs Memory Resources User Guide

UG474, 7 Series FPGAs Configurable Logic Block User Guide

UG479, 7 Series FPGAs DSP48E1 Slice User Guide

UG480, 7 Series FPGAs and Zynq-7000 SoC XADC Dual 12-Bit 1 MSPS ADC User Guide

UG482, 7 Series FPGAs GTP Transceivers User Guide

UG821, Zynq-7000 SoC Software Developers Guide

UG933, Zynq-7000 SoC PCB Design Guide

For a complete list of available documentation, go to: http://www.xilinx.com/products/silicon-devices/soc/zyng-7000.html#documentation

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

XMP097 (v1.3.2)

