

1. Description

1.1. Project

Project Name	Universal_board_F407VET6
Board Name	custom
Generated with:	STM32CubeMX 6.10.0
Date	04/22/2024

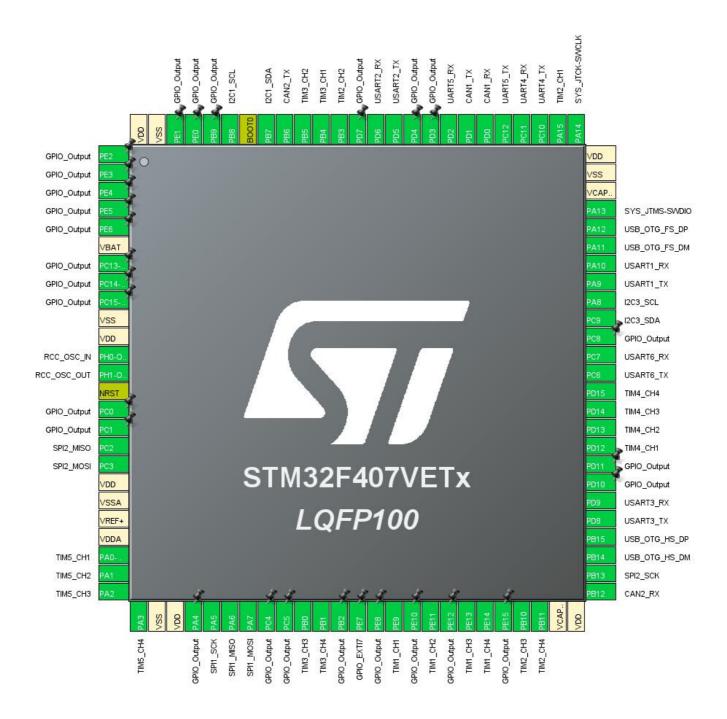
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F407/417
MCU name	STM32F407VETx
MCU Package	LQFP100
MCU Pin number	100

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



3. Pins Configuration

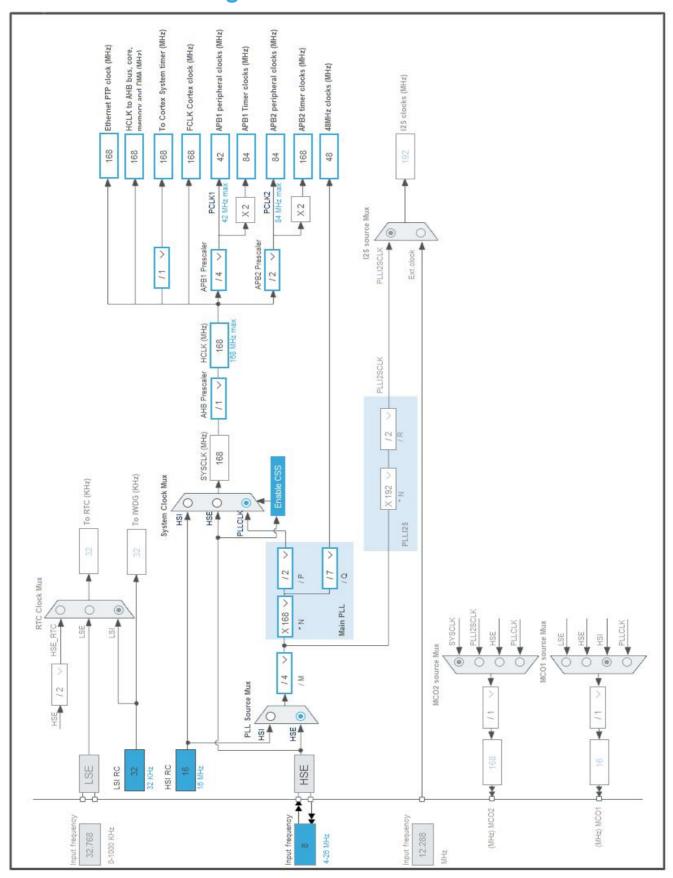
Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP100	(function after		Function(s)	
EQT 100	reset)		r unodon(o)	
1	PE2 *	I/O	GPIO_Output	
2	PE3 *	I/O	GPIO_Output	
3	PE4 *	I/O	GPIO_Output	
4	PE5 *	I/O	GPIO_Output	
5	PE6 *	I/O	GPIO_Output	
6	VBAT	Power	J. 10_0 a.p.a.	
7	PC13-ANTI_TAMP *	I/O	GPIO_Output	
8	PC14-OSC32_IN *	I/O	GPIO_Output	
9	PC15-OSC32_OUT *	I/O	GPIO_Output	
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
15	PC0 *	I/O	GPIO_Output	
16	PC1 *	I/O	GPIO_Output	
17	PC2	I/O	SPI2_MISO	
18	PC3	I/O	SPI2_MOSI	
19	VDD	Power		
20	VSSA	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0-WKUP	I/O	TIM5_CH1	
24	PA1	I/O	TIM5_CH2	
25	PA2	I/O	TIM5_CH3	
26	PA3	I/O	TIM5_CH4	
27	VSS	Power		
28	VDD	Power		
29	PA4 *	I/O	GPIO_Output	
30	PA5	I/O	SPI1_SCK	
31	PA6	I/O	SPI1_MISO	
32	PA7	I/O	SPI1_MOSI	
33	PC4 *	I/O	GPIO_Output	
34	PC5 *	I/O	GPIO_Output	
35	PB0	I/O	TIM3_CH3	
36	PB1	I/O	TIM3_CH4	

Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP100	(function after		Function(s)	
	reset)		()	
37	PB2 *	I/O	GPIO_Output	
38	PE7	I/O	GPIO_EXTI7	
39	PE8 *	I/O	GPIO_Output	
40	PE9	I/O	TIM1_CH1	
41	PE10 *	I/O	GPIO_Output	
42	PE11	I/O	TIM1_CH2	
43	PE12 *	I/O	GPIO_Output	
44	PE13	I/O	TIM1_CH3	
45	PE14	I/O	TIM1_CH4	
46	PE15 *	I/O	GPIO_Output	
47	PB10	I/O	TIM2_CH3	
48	PB11	I/O	TIM2_CH4	
49	VCAP_1	Power		
50	VDD	Power		
51	PB12	I/O	CAN2_RX	
52	PB13	I/O	SPI2_SCK	
53	PB14	I/O	USB_OTG_HS_DM	
54	PB15	I/O	USB_OTG_HS_DP	
55	PD8	I/O	USART3_TX	
56	PD9	I/O	USART3_RX	
57	PD10 *	I/O	GPIO_Output	
58	PD11 *	I/O	GPIO_Output	
59	PD12	I/O	TIM4_CH1	
60	PD13	I/O	TIM4_CH2	
61	PD14	I/O	TIM4_CH3	
62	PD15	I/O	TIM4_CH4	
63	PC6	I/O	USART6_TX	
64	PC7	I/O	USART6_RX	
65	PC8 *	I/O	GPIO_Output	
66	PC9	I/O	I2C3_SDA	
67	PA8	I/O	I2C3_SCL	
68	PA9	I/O	USART1_TX	
69	PA10	I/O	USART1_RX	
70	PA11	I/O	USB_OTG_FS_DM	
71	PA12	I/O	USB_OTG_FS_DP	
72	PA13	I/O	SYS_JTMS-SWDIO	
73	VCAP_2	Power		
74	VSS	Power		
75	VDD	Power		
-				1

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
76	PA14	I/O	SYS_JTCK-SWCLK	
77	PA15	I/O	TIM2_CH1	
78	PC10	I/O	UART4_TX	
79	PC11	I/O	UART4_RX	
80	PC12	I/O	UART5_TX	
81	PD0	I/O	CAN1_RX	
82	PD1	I/O	CAN1_TX	
83	PD2	I/O	UART5_RX	
84	PD3 *	I/O	GPIO_Output	
85	PD4 *	I/O	GPIO_Output	
86	PD5	I/O	USART2_TX	
87	PD6	I/O	USART2_RX	
88	PD7 *	I/O	GPIO_Output	
89	PB3	I/O	TIM2_CH2	
90	PB4	I/O	TIM3_CH1	
91	PB5	I/O	TIM3_CH2	
92	PB6	I/O	CAN2_TX	
93	PB7	I/O	I2C1_SDA	
94	BOOT0	Boot		
95	PB8	I/O	I2C1_SCL	
96	PB9 *	I/O	GPIO_Output	
97	PE0 *	I/O	GPIO_Output	
98	PE1 *	I/O	GPIO_Output	
99	VSS	Power		
100	VDD	Power		

^{*} The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	Universal_board_F407VET6
Project Folder	C:\Users\tangsang\Desktop\GY95_tac_F4
Toolchain / IDE	MDK-ARM V5.32
Firmware Package Name and Version	STM32Cube FW_F4 V1.28.0
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_CAN1_Init	CAN1
5	MX_CAN2_Init	CAN2
6	MX_I2C1_Init	I2C1
7	MX_I2C3_Init	I2C3
8	MX_SPI1_Init	SPI1
9	MX_SPI2_Init	SPI2
10	MX_TIM1_Init	TIM1
11	MX_TIM2_Init	TIM2

Rank	Function Name	Peripheral Instance Name
12	MX_TIM3_Init	TIM3
13	MX_TIM4_Init	TIM4
14	MX_TIM5_Init	TIM5
15	MX_UART4_Init	UART4
16	MX_UART5_Init	UART5
17	MX_USART1_UART_Init	USART1
18	MX_USART2_UART_Init	USART2
19	MX_USART3_UART_Init	USART3
20	MX_USART6_UART_Init	USART6
21	MX_USB_OTG_FS_PCD_Init	USB_OTG_FS
22	MX_USB_OTG_HS_PCD_Init	USB_OTG_HS

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F4
Line	STM32F407/417
MCU	STM32F407VETx
Datasheet	DS8626_Rev8

1.2. Parameter Selection

Temperature	25
Vdd	3.3

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

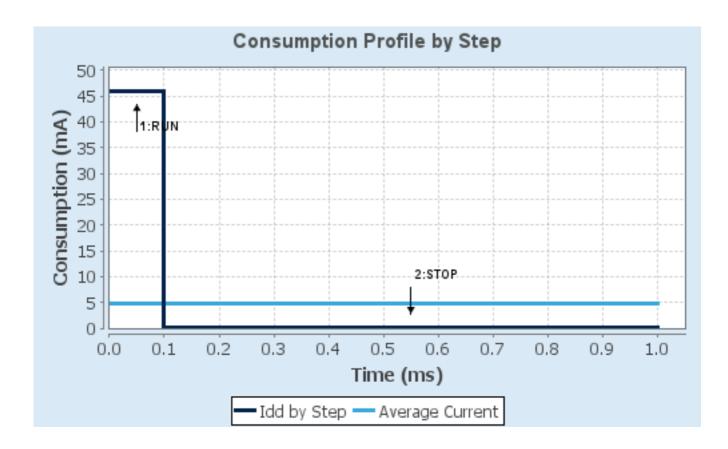
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	168 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	46 mA	280 μA
Duration	0.1 ms	0.9 ms
DMIPS	210.0	0.0
Ta Max	98.47	104.96
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	4.85 mA
Battery Life	29 days, 4 hours	Average DMIPS	210.0 DMIPS

1.6. Chart



2. Peripherals and Middlewares Configuration

2.1. CAN1

mode: Activated

2.1.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum) 3 *

Time Quantum 71.42857142857143 *

Time Quanta in Bit Segment 1 10 Times *

Time Quanta in Bit Segment 2 3 Times *

Time for one Bit 1000

Baud Rate 1000000 *

ReSynchronization Jump Width 1 Time

Basic Parameters:

Time Triggered Communication Mode

Automatic Bus-Off Management

Disable

Automatic Wake-Up Mode

Disable

Automatic Retransmission

Disable

Receive Fifo Locked Mode

Disable

Transmit Fifo Priority

Disable

Advanced Parameters:

Operating Mode Normal

2.2. CAN2

mode: Activated

2.2.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum) 3 *

Time Quantum 71.42857142857143 *

Time Quanta in Bit Segment 1 10 Times *

Time Quanta in Bit Segment 2 3 Times *

Time for one Bit 1000

Baud Rate 1000000 *

ReSynchronization Jump Width 1 Time

Basic Parameters:

Time Triggered Communication Mode

Automatic Bus-Off Management

Disable

Automatic Wake-Up Mode

Disable

Automatic Retransmission

Disable

Receive Fifo Locked Mode

Disable

Transmit Fifo Priority

Disable

Advanced Parameters:

Operating Mode Normal

2.3. I2C1 I2C: I2C

2.3.1. Parameter Settings:

Master Features:

I2C Speed Mode Fast Mode *

I2C Clock Speed (Hz) 400000

Fast Mode Duty Cycle Duty cycle Tlow/Thigh = 2

Slave Features:

Clock No Stretch Mode Disabled
Primary Address Length selection 7-bit
Dual Address Acknowledged Disabled
Primary slave address 0
General Call address detection Disabled

2.4. I2C3 I2C: I2C

2.4.1. Parameter Settings:

Master Features:

I2C Speed Mode Fast Mode *

I2C Clock Speed (Hz) 400000

Fast Mode Duty Cycle Duty cycle Tlow/Thigh = 2

Slave Features:

Clock No Stretch Mode Disabled
Primary Address Length selection 7-bit
Dual Address Acknowledged Disabled
Primary slave address 0

General Call address detection

Disabled

2.5. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

2.5.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Enabled
Data Cache Enabled

Flash Latency(WS) 5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value 16
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

2.6. SPI1

Mode: Full-Duplex Master

2.6.1. Parameter Settings:

Basic Parameters:

Frame Format Motorola

Data Size 8 Bits

First Bit MSB First

Clock Parameters:

Prescaler (for Baud Rate) 2

Baud Rate 42.0 MBits/s *

Clock Polarity (CPOL) Low
Clock Phase (CPHA) 1 Edge

Advanced Parameters:

CRC Calculation Disabled
NSS Signal Type Software

2.7. SPI2

Mode: Full-Duplex Master

2.7.1. Parameter Settings:

Basic Parameters:

Frame Format Motorola
Data Size 8 Bits
First Bit MSB First

Clock Parameters:

Prescaler (for Baud Rate) 2

Baud Rate 21.0 MBits/s *

Clock Polarity (CPOL) Low
Clock Phase (CPHA) 1 Edge

Advanced Parameters:

CRC Calculation Disabled
NSS Signal Type Software

2.8. SYS

Debug: Serial Wire

Timebase Source: TIM14

2.9. TIM1

Channel1: PWM Generation CH1 Channel2: PWM Generation CH2 Channel3: PWM Generation CH3 Channel4: PWM Generation CH4

2.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 168-1 *

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 2000-1 *
Internal Clock Division (CKD) No Division

Repetition Counter (RCR - 8 bits value) 0

auto-reload preload Enable *

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State Disable BRK Polarity High

Break And Dead Time management - Output Configuration:

Automatic Output State Disable
Off State Selection for Run Mode (OSSR) Disable
Off State Selection for Idle Mode (OSSI) Disable
Lock Configuration Off

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable
Fast Mode Disable
CH Polarity High
CH Idle State Reset

PWM Generation Channel 2:

Mode PWM mode 1

Pulse (16 bits value)0Output compare preloadEnableFast ModeDisableCH PolarityHighCH Idle StateReset

PWM Generation Channel 3:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

CH Idle State Reset

PWM Generation Channel 4:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable
Fast Mode Disable
CH Polarity High
CH Idle State Reset

2.10. TIM2

Channel1: PWM Generation CH1 Channel2: PWM Generation CH2 Channel3: PWM Generation CH3 Channel4: PWM Generation CH4

2.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 168-1 *

Counter Mode Up

Counter Period (AutoReload Register - 32 bits value) 2000-1 *

Internal Clock Division (CKD) No Division auto-reload preload Enable *

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)

Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (32 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

PWM Generation Channel 2:

Mode PWM mode 1

Pulse (32 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

PWM Generation Channel 3:

Mode PWM mode 1

Pulse (32 bits value) 0

Output compare preload Enable
Fast Mode Disable
CH Polarity High

PWM Generation Channel 4:

Mode PWM mode 1

Pulse (32 bits value) 0

Output compare preload Enable
Fast Mode Disable
CH Polarity High

2.11. TIM3

Channel1: PWM Generation CH1 Channel2: PWM Generation CH2 Channel3: PWM Generation CH3 Channel4: PWM Generation CH4

2.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 168-1 *
Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 2000-1 *

Internal Clock Division (CKD) No Division auto-reload preload Enable *

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)

Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

PWM Generation Channel 2:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

PWM Generation Channel 3:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

PWM Generation Channel 4:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable
Fast Mode Disable
CH Polarity High

2.12. TIM4

Channel1: PWM Generation CH1
Channel2: PWM Generation CH2
Channel3: PWM Generation CH3
Channel4: PWM Generation CH4

2.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 168-1 *

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 2000-1 *

Internal Clock Division (CKD) No Division auto-reload preload Enable *

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

PWM Generation Channel 2:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable
Fast Mode Disable
CH Polarity High

PWM Generation Channel 3:

Mode PWM mode 1

Pulse (16 bits value) 0
Output compare preload Enable
Fast Mode Disable
CH Polarity High

PWM Generation Channel 4:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

2.13. TIM5

Channel1: PWM Generation CH1
Channel2: PWM Generation CH2
Channel3: PWM Generation CH3
Channel4: PWM Generation CH4

2.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 168-1 *

Counter Mode Up

Counter Period (AutoReload Register - 32 bits value) 2000-1

Counter Period (AutoReload Register - 32 bits value) 2000-1 *
Internal Clock Division (CKD) No Division
auto-reload preload Enable *

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (32 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

PWM Generation Channel 2:

Mode PWM mode 1

Pulse (32 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

PWM Generation Channel 3:

Mode PWM mode 1

Pulse (32 bits value) 0

Output compare preload Enable
Fast Mode Disable
CH Polarity High

PWM Generation Channel 4:

Mode PWM mode 1

Pulse (32 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

2.14. UART4

Mode: Asynchronous

2.14.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples

2.15. UART5

Mode: Asynchronous

2.15.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples

2.16. USART1

Mode: Asynchronous

2.16.1. Parameter Settings:

Basic Parameters:

Baud Rate 100000 *

Word Length 9 Bits (including Parity) *

Parity Even *

Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples

2.17. USART2

Mode: Asynchronous

2.17.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples

2.18. USART3

Mode: Asynchronous

2.18.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples

2.19. USART6

Mode: Asynchronous

2.19.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples

2.20. USB_OTG_FS

Mode: Device_Only

2.20.1. Parameter Settings:

Speed Device Full Speed 12MBit/s

Low powerDisabledLink Power ManagementDisabledVBUS sensingDisabledSignal start of frameDisabled

2.21. USB_OTG_HS

Internal FS Phy: Device_Only

2.21.1. Parameter Settings:

Speed Device Full Speed 12MBit/s

Enable internal IP DMA Disabled
Physical interface Internal Phy
Low power Disabled
Link Power Management Disabled

Use dedicated end point 1 interrupt Disabled VBUS sensing Disabled Signal start of frame Disabled

* User modified value

3. System Configuration

3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
CAN1	PD0	CAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD1	CAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
CAN2	PB12	CAN2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB6	CAN2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
I2C1	PB7	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Very High	
	PB8	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Very High	
I2C3	PC9	I2C3_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Very High	
	PA8	I2C3_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Very High	
RCC	PH0- OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1- OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPI2	PC2	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC3	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB13	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SYS	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	
TIM1	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE11	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE13	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE14	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM2	PB10	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB11	TIM2_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA15	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB3	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM3	PB0	TIM3_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB1	TIM3_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB4	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB5	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD14	TIM4_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD15	TIM4_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM5	PA0-WKUP	TIM5_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	TIM5_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA2	TIM5_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA3	TIM5_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART4	PC10	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
UART5	PC12	UART5_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	UART5_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
USART2	PD5	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD6	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
USART6	PC6	USART6_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC7	USART6_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
USB_OTG_ FS	PA11	USB_OTG_FS_ DM	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA12	USB_OTG_FS_ DP	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
USB_OTG_ HS	PB14	USB_OTG_HS_ DM	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB15	USB_OTG_HS_ DP	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
GPIO	PE2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC13- ANTI_TAMP	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC14- OSC32_IN	GPIO_Output	Output Push Pull	Pull-up *	Low	
	PC15- OSC32_OU T	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE7	GPIO_EXTI7	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	
	PE8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

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IP	Pin	Signal	GPIO mode	GPIO pull/up pull	Max	User Label
				down	Speed	
	PD11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

3.2. DMA configuration

DMA request	Stream	Direction	Priority
USART1 RX	DMA2 Stream2	Peripheral To Memory	Low

USART1_RX: DMA2_Stream2 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: Enable *

Peripheral Data Width: Byte
Memory Data Width: Byte

3.3. NVIC configuration

3.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
CAN1 RX0 interrupts	true	0	0
TIM3 global interrupt	true	0	0
TIM4 global interrupt	true	0	0
USART1 global interrupt	true	0	0
USART2 global interrupt	true	0	0
USART3 global interrupt	true	0	0
TIM8 trigger and commutation interrupts and TIM14 global interrupt	true	15	0
TIM5 global interrupt	true	0	0
DMA2 stream2 global interrupt	true	0	0
USART6 global interrupt	true	0	0
PVD interrupt through EXTI line 16		unused	
Flash global interrupt		unused	
RCC global interrupt		unused	
CAN1 TX interrupts		unused	
CAN1 RX1 interrupt		unused	
CAN1 SCE interrupt		unused	
EXTI line[9:5] interrupts		unused	
TIM1 break interrupt and TIM9 global interrupt		unused	
TIM1 update interrupt and TIM10 global interrupt		unused	
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
SPI1 global interrupt	unused		
SPI2 global interrupt		unused	
UART4 global interrupt		unused	

Interrupt Table	Enable	Preenmption Priority	SubPriority
UART5 global interrupt		unused	
CAN2 TX interrupts		unused	
CAN2 RX0 interrupts		unused	
CAN2 RX1 interrupt		unused	
CAN2 SCE interrupt	unused		
USB On The Go FS global interrupt	unused		
I2C3 event interrupt		unused	
I2C3 error interrupt		unused	
USB On The Go HS End Point 1 Out global interrupt		unused	
USB On The Go HS End Point 1 In global interrupt		unused	
USB On The Go HS global interrupt	unused		
FPU global interrupt		unused	

3.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
CAN1 RX0 interrupts	false	true	true
TIM3 global interrupt	false	true	true
TIM4 global interrupt	false	true	true
USART1 global interrupt	false	true	true
USART2 global interrupt	false	true	true
USART3 global interrupt	false	true	true
TIM8 trigger and commutation interrupts and TIM14 global interrupt	false	true	true
TIM5 global interrupt	false	true	true
DMA2 stream2 global interrupt	false	true	true
USART6 global interrupt	false	true	true

* User modified value

4. System Views

4.1. Category view

4.1.1. Current

5. Software Pack Report

5.1. Software Pack selected

Vendor	Name	Version	Component
STMicroelectronic	X-CUBE-	1.1.0	Class : RTOS
s	AZRTOS-F4		Group : ThreadX
			SubGroup : Core
			Version : 6.1.10

6. Docs & Resources

Type Link

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417_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis model/stm32f405-415 407-

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System View https://www.st.com/resource/en/svd/stm32f4_svd.zip

Description

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