FPGA 开源工作室将通过五篇文章来给大家讲解 xilinx FPGA 使用 mig IP 对 DDR3 的读写控制，旨在让大家更快的学习和应用 DDR3。
本实验和工程基于 Digilent 的 Arty Artix-35T FPGA 开发板完成。
软件使用 Vivado 2018.1。

第一篇：DDR3 和 mig 的介绍

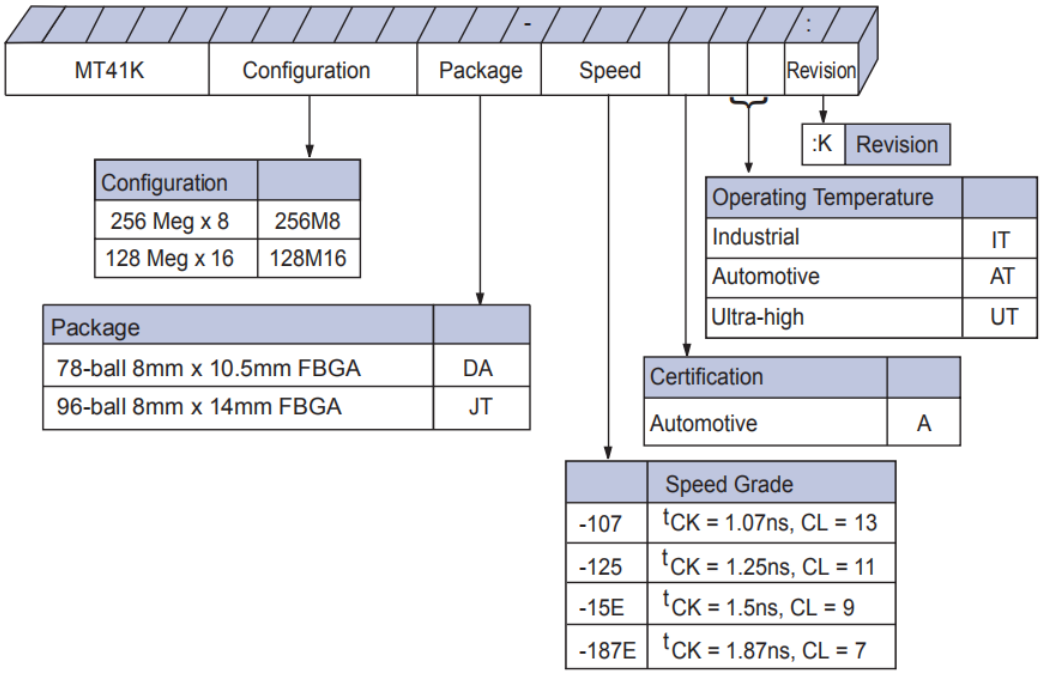
1 DDR3 介绍

以镁光的 MT41K128M16 为例来介绍 DDR3。

Parameter	256 Meg x 8	128 Meg x 16
Configuration	32 Meg x 8 x 8 banks	16 Meg x 16 x 8 banks
Refresh count	8K	8K
Row address	32K A[14:0]	16K A[13:0]
Bank address	8 BA[2:0]	8 BA[2:0]
Column address	1K A[9:0]	1K A[9:0]

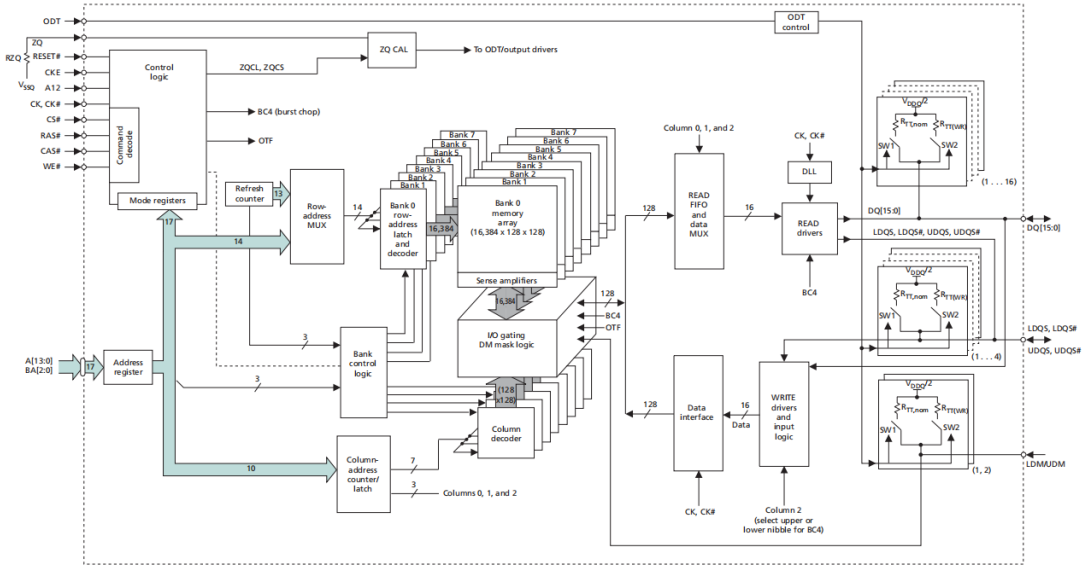
通过以上信息我们即可知道 DDR3 的内存容量，Row,Column 和 Bank 的地址位宽。开发板选用的 MT41K128M16 DDR3 的容量为 16Megx16x8banks=2048Mb=2Gb。

1.1 DDR3 命名



我们通过 Configuration,Package,Speed...等 DDR3 的命名可知道 DDR3 的容量，封装，速度等级等信息。

1.2 DDR3 的内部结构



1.3 接口

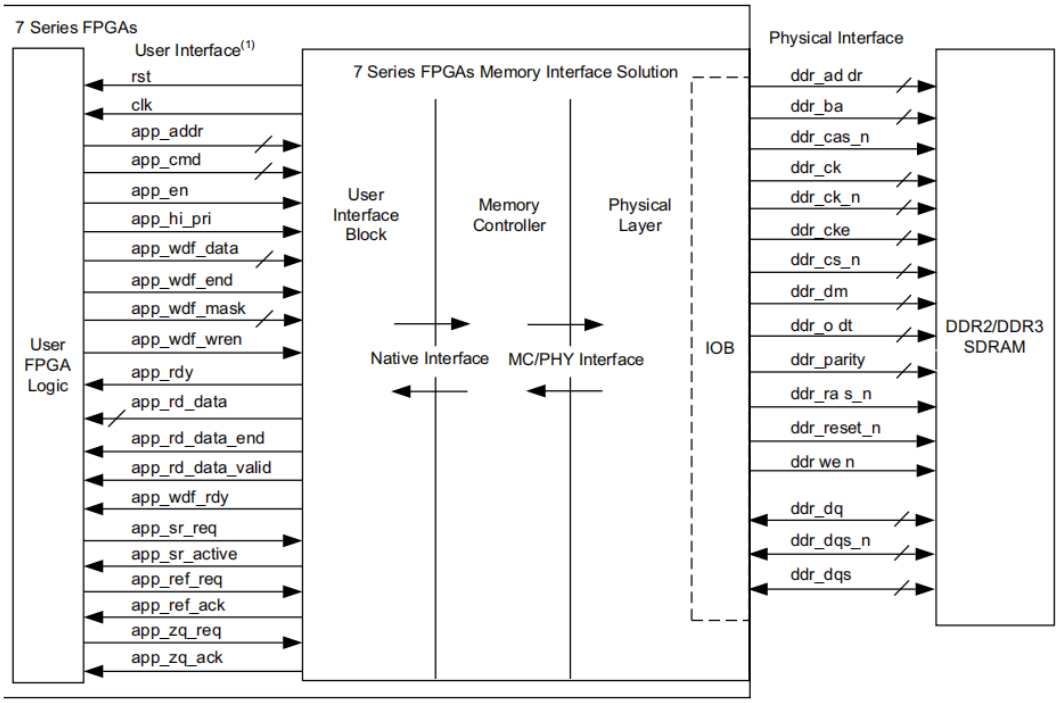
Symbol	Type	Description
A[14:13], A12/BC#, A11, A10/AP, A[9:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to V_{REFCA}. A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4 burst chop). See Truth Table - Command.
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to V_{REFCA}.
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
CKE	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE power-down and SELF REFRESH operations (all banks idle) or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to V_{REFCA}.

CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to V_{REFCA}.
DM	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with the input data during a write access. Although the DM ball is input-only, the DM loading is designed to match that of the DQ and DQS balls. DM is referenced to V_{REFDQ}. DM has an optional use as TDQS on the x8 device.
ODT	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[7:0], DQS, DQS#, and DM for the x8. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to V_{REFCA}.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to V_{REFCA}.
RESET#	Input	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × V_{DDQ} and DC LOW ≤ 0.2 × V_{DDQ}. RESET# assertion and deassertion are asynchronous.
DQ[7:0]	I/O	**Data input/output:** Bidirectional data bus for the x8 configuration. DQ[7:0] are referenced to V_{REFDQ}.

Symbol	Type	Description
DQS, DQS#	I/O	**Data strobe:** Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
TDQS, TDQS#	I/O	**Termination data strobe:** Applies to the x8 configuration only. When TDQS is enabled, DM is disabled, and the TDQS and TDQS# balls provide termination resistance.
V_{DD}	Supply	**Power supply:** 1.35V, 1.283–1.45V operational; compatible to 1.5V operation.
V_{DDQ}	Supply	**DQ power supply:** 1.35V, 1.283–1.45V operational; compatible with 1.5V operation.
V_{REFCA}	Supply	**Reference voltage for control, command, and address:** V_{REFCA} must be maintained at all times (including self refresh) for proper device operation.
V_{REFDQ}	Supply	**Reference voltage for data:** V_{REFDQ} must be maintained at all times (including self refresh) for proper device operation.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
ZQ	Reference	**External reference ball for output drive calibration:** This ball is tied to an external 240Ω resistor (R_{ZQ}), which is tied to V_{SSQ}.
NC	–	**No connect:** These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).
NF	–	**No function:** When configured as a x8 device, these balls are defined as TDQS#, DQ[7:4].

使用 xilinx mig IP 来控制 DDR3 的数据读写我们了解 DDR3 以上信息即可。

2 mig 介绍



如上图所示，mig(Memory Interface Solution) IP 由三部分组成 User Interface Block,Memory Controller 和 Physical Layer。IP 的一边是连接 DDR3 的接口（Physical Interface），另一边是用户逻辑控制接口（User FPGA Logic）。想要正确的控制 DDR3 的读写，我们需要正确的设置 mig IP 和正确的用户逻辑控制接口逻辑。

2.1 mig user interface

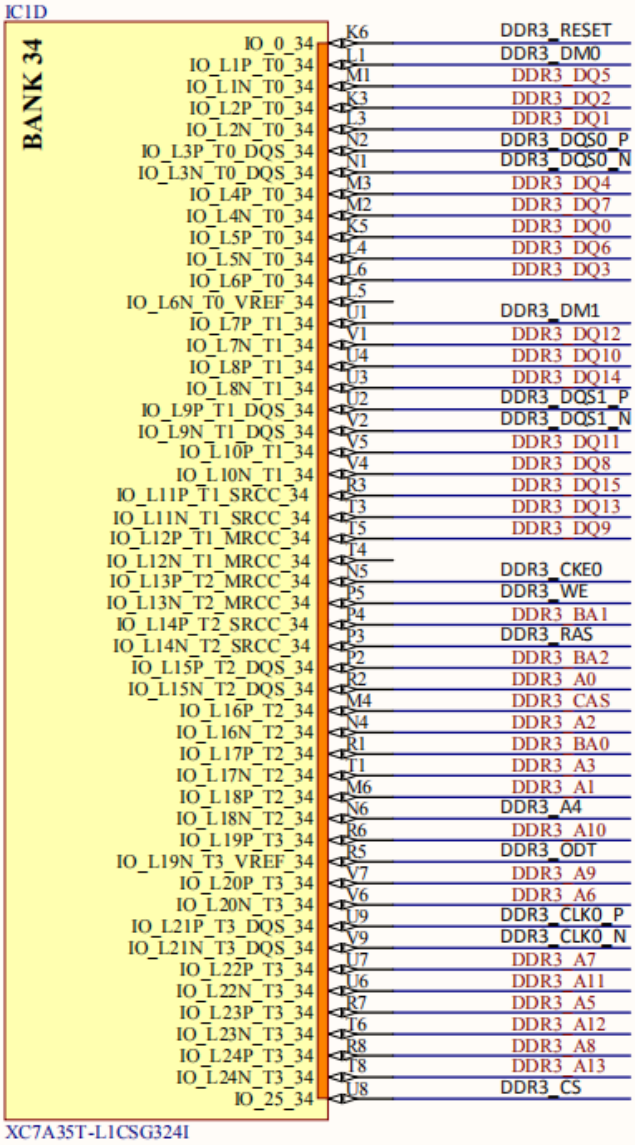
Signal	Direction	Description
app_addr[ADDR_WIDTH – 1:0]	Input	This input indicates the address for the current request.
app_cmd[2:0]	Input	This input selects the command for the current request.
app_en	Input	This is the active-High strobe for the app_addr[], app_cmd[2:0], app_sz, and app_hi_pri inputs.
app_rdy	Output	This output indicates that the UI is ready to accept commands. If the signal is deasserted when app_en is enabled, the current app_cmd and app_addr must be retried until app_rdy is asserted.
app_hi_pri	Input	This active-High input elevates the priority of the current request.
app_rd_data [APP_DATA_WIDTH – 1:0]	Output	This provides the output data from read commands.
app_rd_data_end	Output	This active-High output indicates that the current clock cycle is the last cycle of output data on app_rd_data[]. This is valid only when app_rd_data_valid is active-High.
app_rd_data_valid	Output	This active-High output indicates that app_rd_data[] is valid.
app_sz	Input	This input is reserved and should be tied to 0.
app_wdf_data [APP_DATA_WIDTH – 1:0]	Input	This provides the data for write commands.

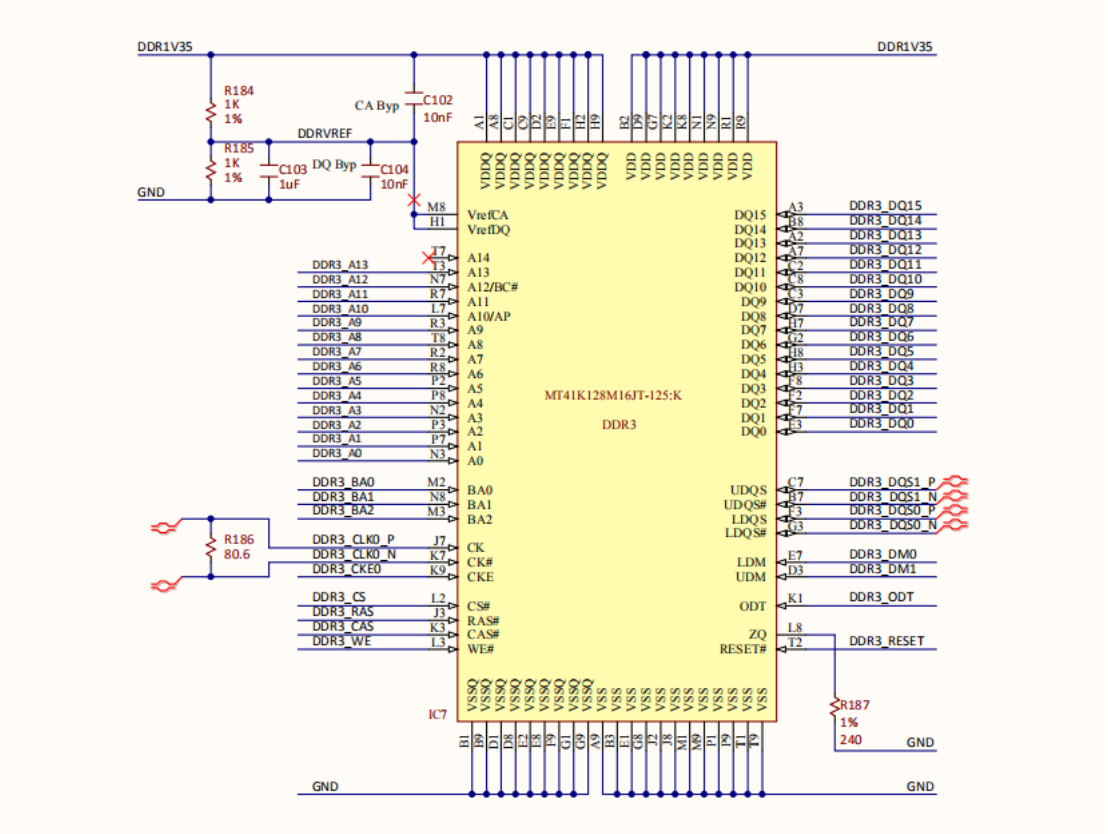
app_wdf_end	Input	This active-High input indicates that the current clock cycle is the last cycle of input data on app_wdf_data[].
app_wdf_mask [APP_MASK_WIDTH – 1:0]	Input	This provides the mask for app_wdf_data[].
app_wdf_rdy	Output	This output indicates that the write data FIFO is ready to receive data. Write data is accepted when app_wdf_rdy = 1'b1 and app_wdf_wren = 1'b1.
app_wdf_wren	Input	This is the active-High strobe for app_wdf_data[].
app_correct_en_i	Input	When asserted, this active-High signal corrects single bit data errors. This input is valid only when ECC is enabled in the GUI. In the example design, this signal is always tied to 1.
app_sr_req	Input	This input is reserved and should be tied to 0.
app_sr_active	Output	This output is reserved.

Signal	Direction	Description
app_ref_req	Input	This active-High input requests that a refresh command be issued to the DRAM.
app_ref_ack	Output	This active-High output indicates that the Memory Controller has sent the requested refresh command to the PHY interface.
app_zq_req	Input	This active-High input requests that a ZQ calibration command be issued to the DRAM.
app_zq_ack	Output	This active-High output indicates that the Memory Controller has sent the requested ZQ calibration command to the PHY interface.
ui_clk	Output	This UI clock must be a half or quarter of the DRAM clock.
init_calib_complete	Output	PHY asserts init_calib_complete when calibration is finished.
app_ecc_multiple_err[7:0](1)	Output	This signal is applicable when ECC is enabled and is valid along with app_rd_data_valid. The app_ecc_multiple_err[3:0] signal is non-zero if the read data from the external memory has two bit errors per beat of the read burst. The SECDED algorithm does not correct the corresponding read data and puts a non-zero value on this signal to notify the corrupted read data at the UI.
ui_clk_sync_rst	Output	This is the active-High UI reset.
app_ecc_single_err[7:0]	Output	This signal is applicable when ECC is enabled and is valid along with app_rd_data_vali. The app_ecc_single_err signal is non-zero if the read data from the external memory has a single bit error per beat of the read burst.

对于 mig 用户端接口含义我们将在《第三篇--mig IP 用户逻辑接口读写时序分析》中详细介绍。

3 DDR3 原理图和 FPGA 原理图


IC1D
BANK 34
IO_0_34
IO_L1P_T0_34
IO_L1N_T0_34
IO_L2P_T0_34
IO_L2N_T0_34
IO_L3P_T0_DQS_34
IO_L3N_T0_DQS_34
IO_L4P_T0_34
IO_L4N_T0_34
IO_L5P_T0_34
IO_L5N_T0_34
IO_L6P_T0_34
IO_L6N_T0_VREF_34
IO_L7P_T1_34
IO_L7N_T1_34
IO_L8P_T1_34
IO_L8N_T1_34
IO_L9P_T1_DQS_34
IO_L9N_T1_DQS_34
IO_L10P_T1_34
IO_L10N_T1_34
IO_L11P_T1_SRCC_34
IO_L11N_T1_SRCC_34
IO_L12P_T1_MRCC_34
IO_L12N_T1_MRCC_34
IO_L13P_T2_MRCC_34
IO_L13N_T2_MRCC_34
IO_L14P_T2_SRCC_34
IO_L14N_T2_SRCC_34
IO_L15P_T2_DQS_34
IO_L15N_T2_DQS_34
IO_L16P_T2_34
IO_L16N_T2_34
IO_L17P_T2_34
IO_L17N_T2_34
IO_L18P_T2_34
IO_L18N_T2_34
IO_L19P_T3_34
IO_L19N_T3_VREF_34
IO_L20P_T3_34
IO_L20N_T3_34
IO_L21P_T3_DQS_34
IO_L21N_T3_DQS_34
IO_L22P_T3_34
IO_L22N_T3_34
IO_L23P_T3_34
IO_L23N_T3_34
IO_L24P_T3_34
IO_L24N_T3_34
IO_25_34
K6 DDR3_RESET
L1 DDR3_DM0
M1 DDR3_DQ5
K3 DDR3_DQ2
L3 DDR3_DQ1
N2 DDR3_DQS0_P
N1 DDR3_DQS0_N
M3 DDR3_DQ4
M2 DDR3_DQ7
K5 DDR3_DQ0
L4 DDR3_DQ6
L6 DDR3_DQ3
L5
U1 DDR3_DM1
V1 DDR3_DQ12
U4 DDR3_DQ10
U3 DDR3_DQ14
U2 DDR3_DQS1_P
V2 DDR3_DQS1_N
V5 DDR3_DQ11
V4 DDR3_DQ8
R3 DDR3_DQ15
T3 DDR3_DQ13
T5 DDR3_DQ9
T4
N5 DDR3_CKE0
P5 DDR3_WE
P4 DDR3_BA1
P3 DDR3_RAS
P2 DDR3_BA2
R2 DDR3_A0
M4 DDR3_CAS
N4 DDR3_A2
R1 DDR3_BA0
T1 DDR3_A3
M6 DDR3_A1
N6 DDR3_A4
R6 DDR3_A10
R5 DDR3_ODT
V7 DDR3_A9
V6 DDR3_A6
U9 DDR3_CLK0_P
V9 DDR3_CLK0_N
U7 DDR3_A7
U6 DDR3_A11
R7 DDR3_A5
T6 DDR3_A12
R8 DDR3_A8
T8 DDR3_A13
U8 DDR3_CS
XC7A35T-L1CSG324I



通过 DDR3 的原理图我们可以知道 DDR3 的供电电压为 1.35V。DDR3 挂在 FPGA 的 34 bank 上。

FPGA 开源工作室为了大家更好的学习 FPGA 目前开通了知识星球（FPGA 自习学院）。FPGA 自习学院将不断更新和总结 FPGA 相关的学习资料，欢迎大家加入。