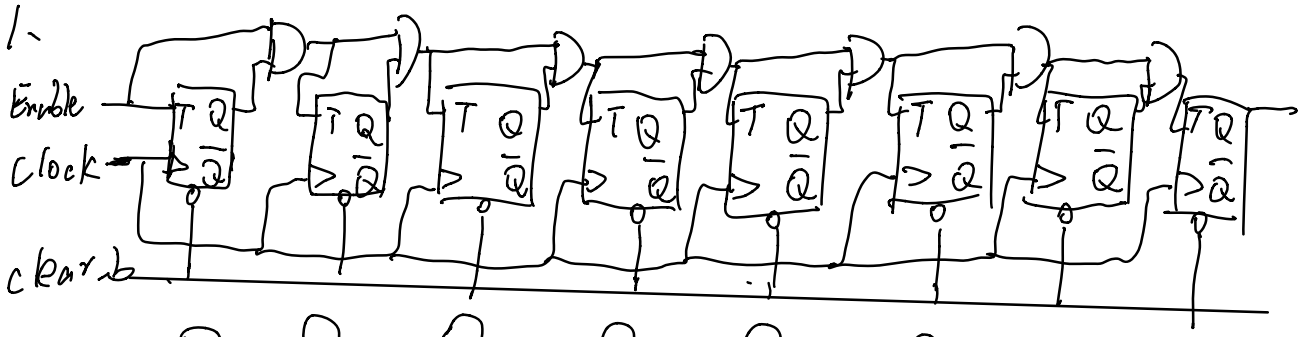
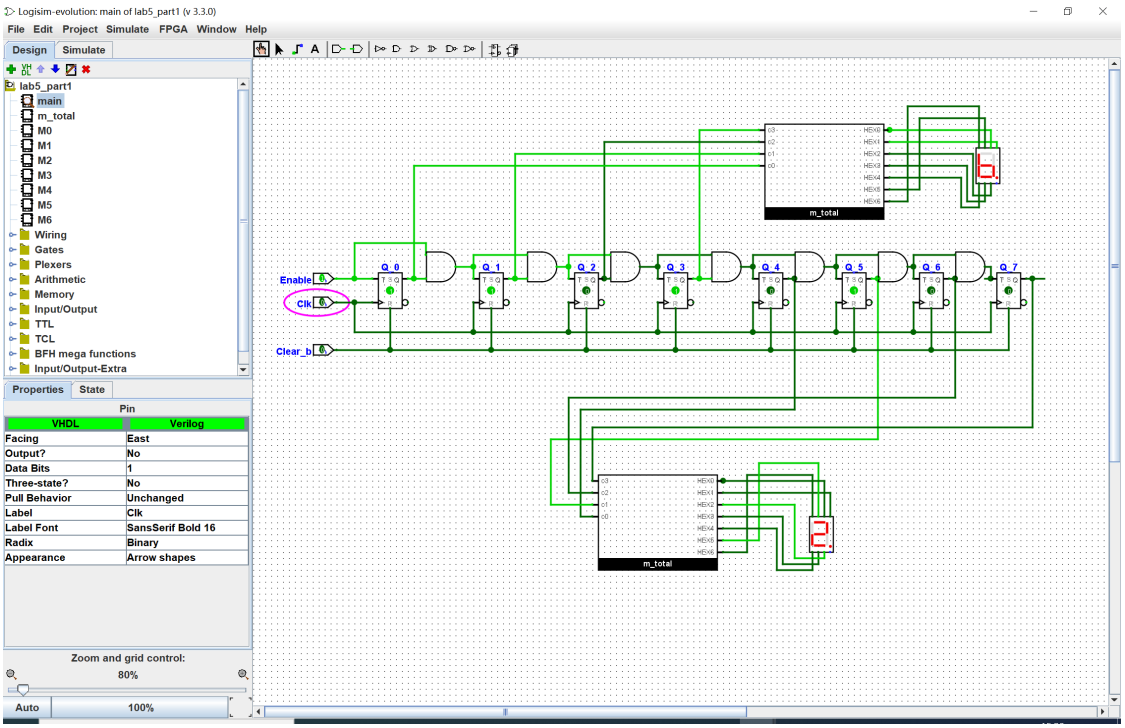
Part I

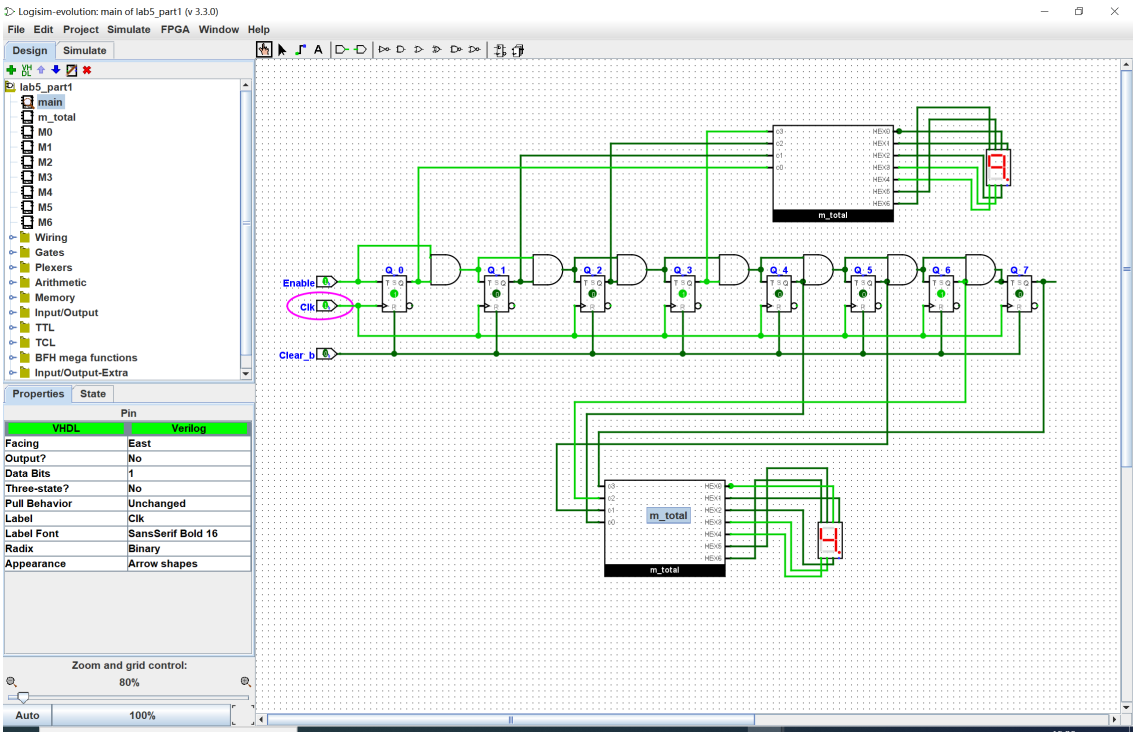
1.



2. Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7

4.



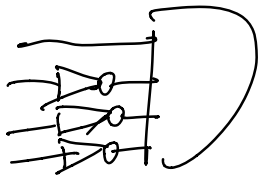

Logisim-evolution: main of lab5_part1 (v 3.3.0)
File Edit Project Simulate FPGA Window Help
Design Simulate
lab5_part1
main
m_total
M0
M1
M2
M3
M4
M5
M6
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
TTL
TCL
BFH mega functions
Input/Output-Extra
Properties State
Pin
VHDL Verilog
Facing East
Output? No
Data Bits 1
Three-state? No
Pull Behavior Unchanged
Label Clk
Label Font SansSerif Bold 16
Radix Binary
Appearance Arrow shapes
Zoom and grid control:
80%
Auto 100%
Enable
Clk
Clear_b
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
m_total
m_total
m_total

Part II:

1. Cause 1111+1 = 10000 − 5 bits
   which the counter has only 4bits,
   so maximum number is not necessary.

2. ① set maximum to be 9

   ② for the And gate

   so maximum would be 1001 → 

In the Wrap around state, next value would be zero.

3.

Wrap around

next value is { 0 – if incrementing
{ max – if decrementing

stay at value

The counters value remains at

the maximum – incrementing

0 – if decrementing

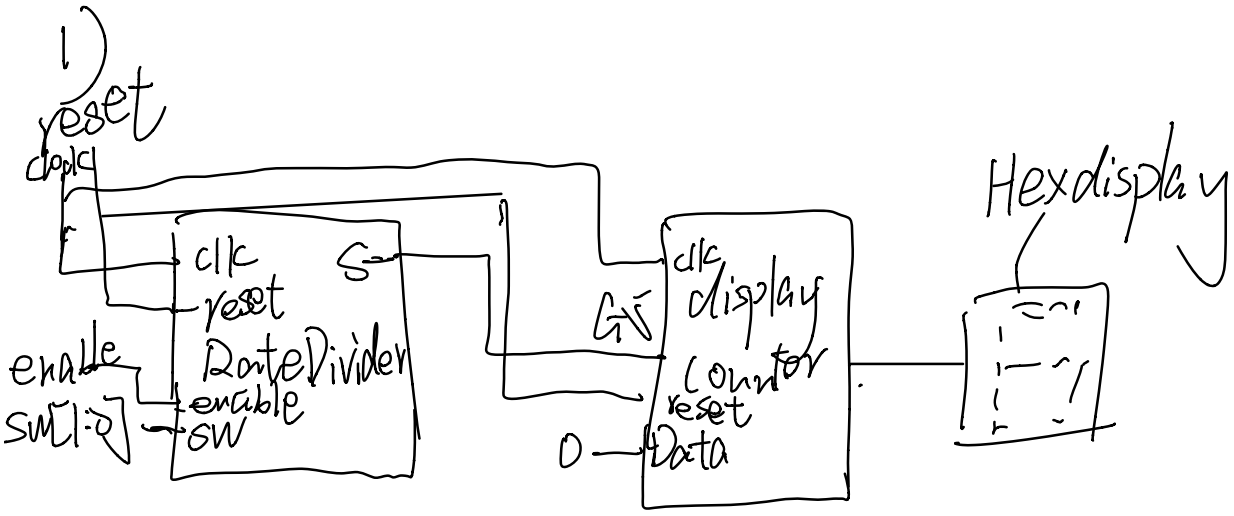
Continue counting

The counter continues incrementing decrementing. keeps the number of bits are as provided by the Data bits Attribute.

Load Next Value
The next value is loaded from the D input.

4. $\log_2(50{,}000{,}000) = 26$ bits

16 Hz – 3125000 – 22 bits
1 Hz – 50M – 26 bits
0.5 Hz – 100M – 27 bits
0.25 Hz – 200M – 28 bits



4) reset: SW 2

Control: SW_{1-0}

enable: SW_3

HEXDisplay: HEX0

Part III:

2a00
3800
2bc0
2ae0
2ee0
3a38
3aee
3ba8

S — 10,1010,0000,0000
T — 11,1000,0000,0000
U — 10,1011,1100,0000
V — 10,1010,1110,0000
W — 10,1110,1110,0000
X — 11,1010,1110,1000
Y — 11,1010,1110,1110
Z — 11,1011,1010,1000

14

1) bit-width: 14

2)