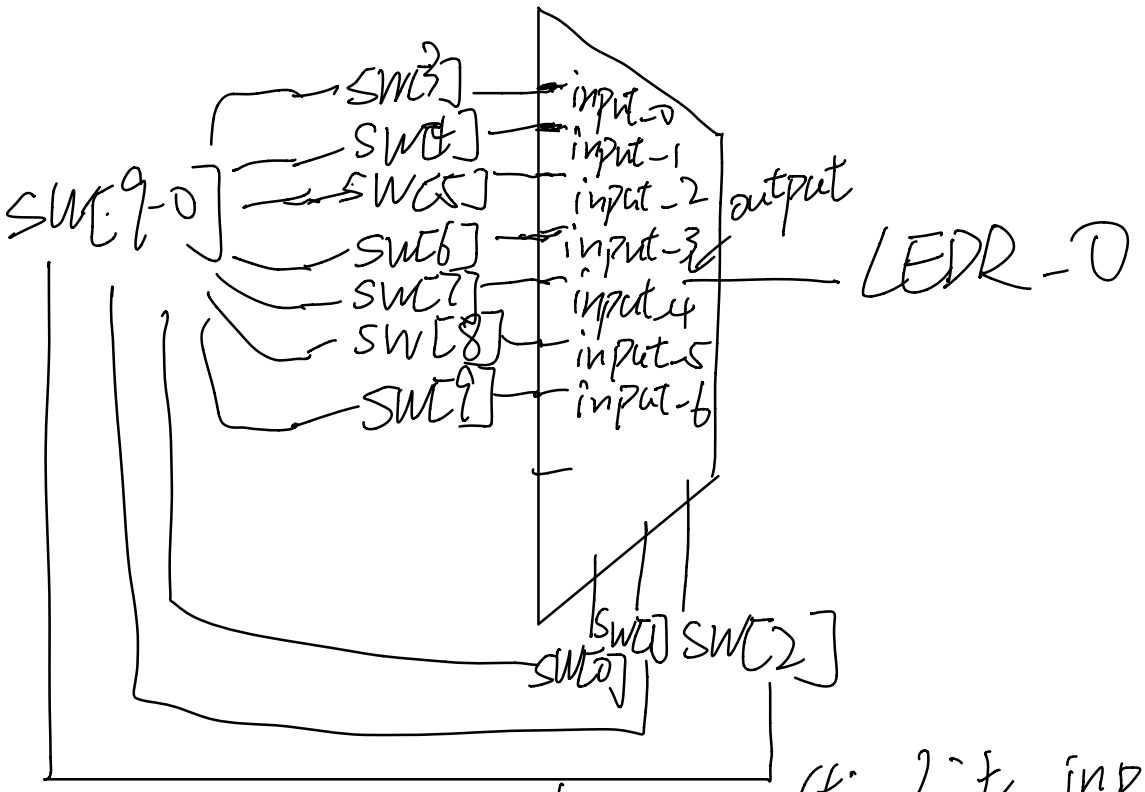
Part 1:

1. Draw schematic

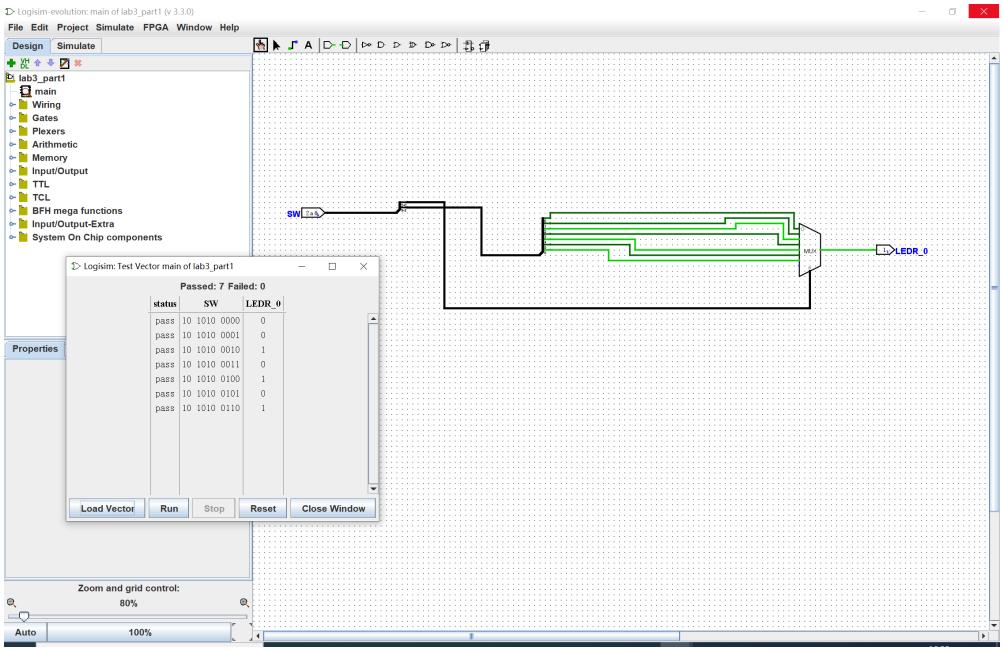


2. How big does the multi-bit input need to be to provide all the inputs to the 7-to-1 multiplexer?

There are 7 inputs to be selected, so in order to have enough bits for selector, we

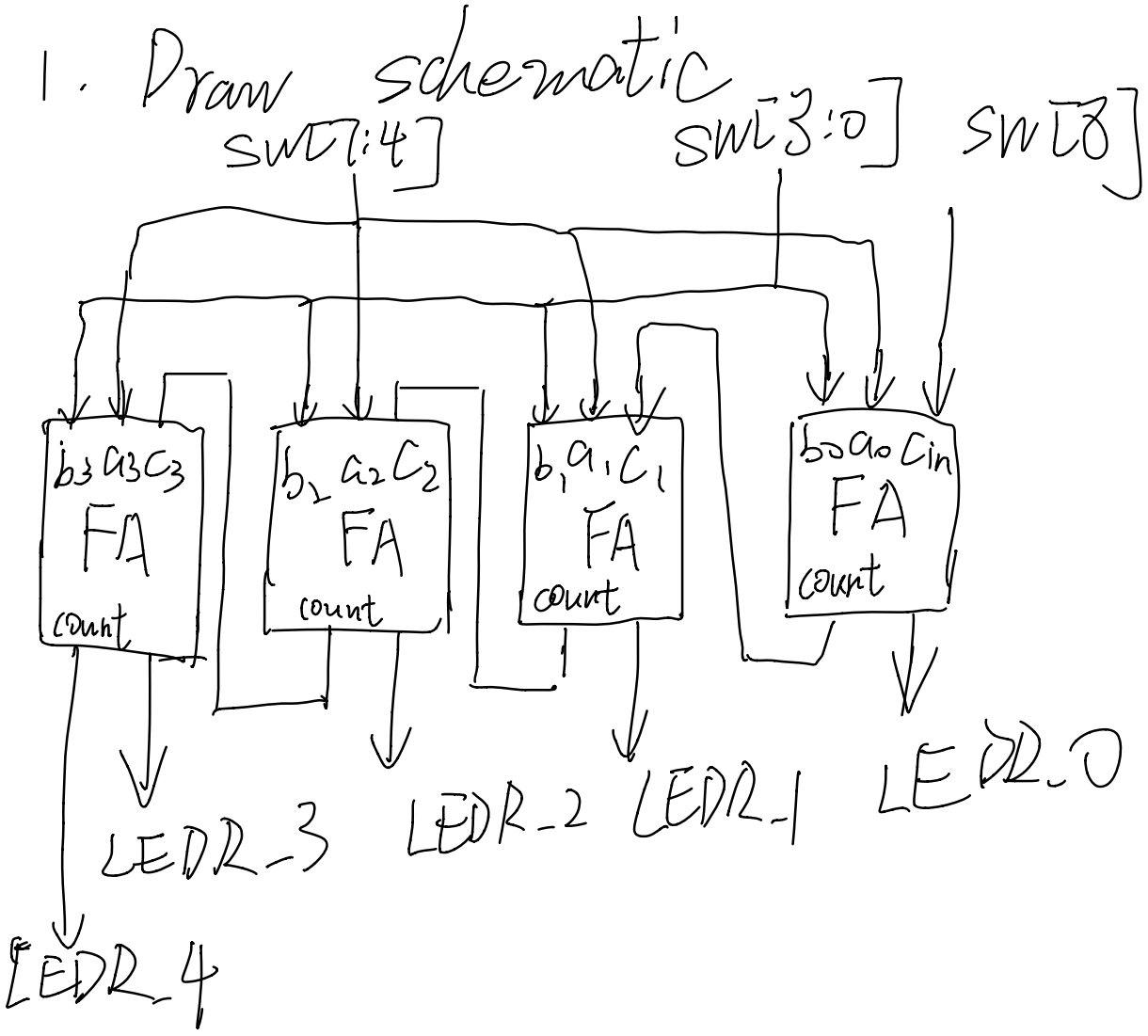
need 3 bits for selection, so totally 10 bits.

3.

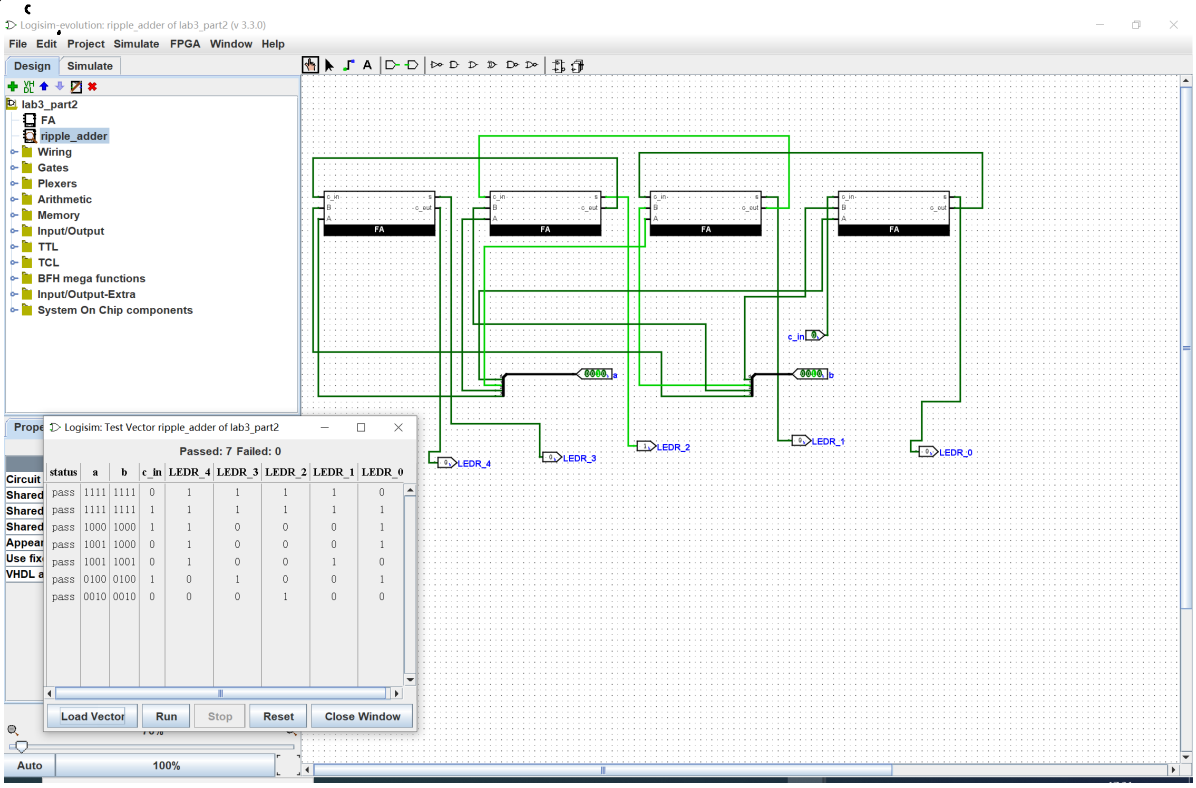


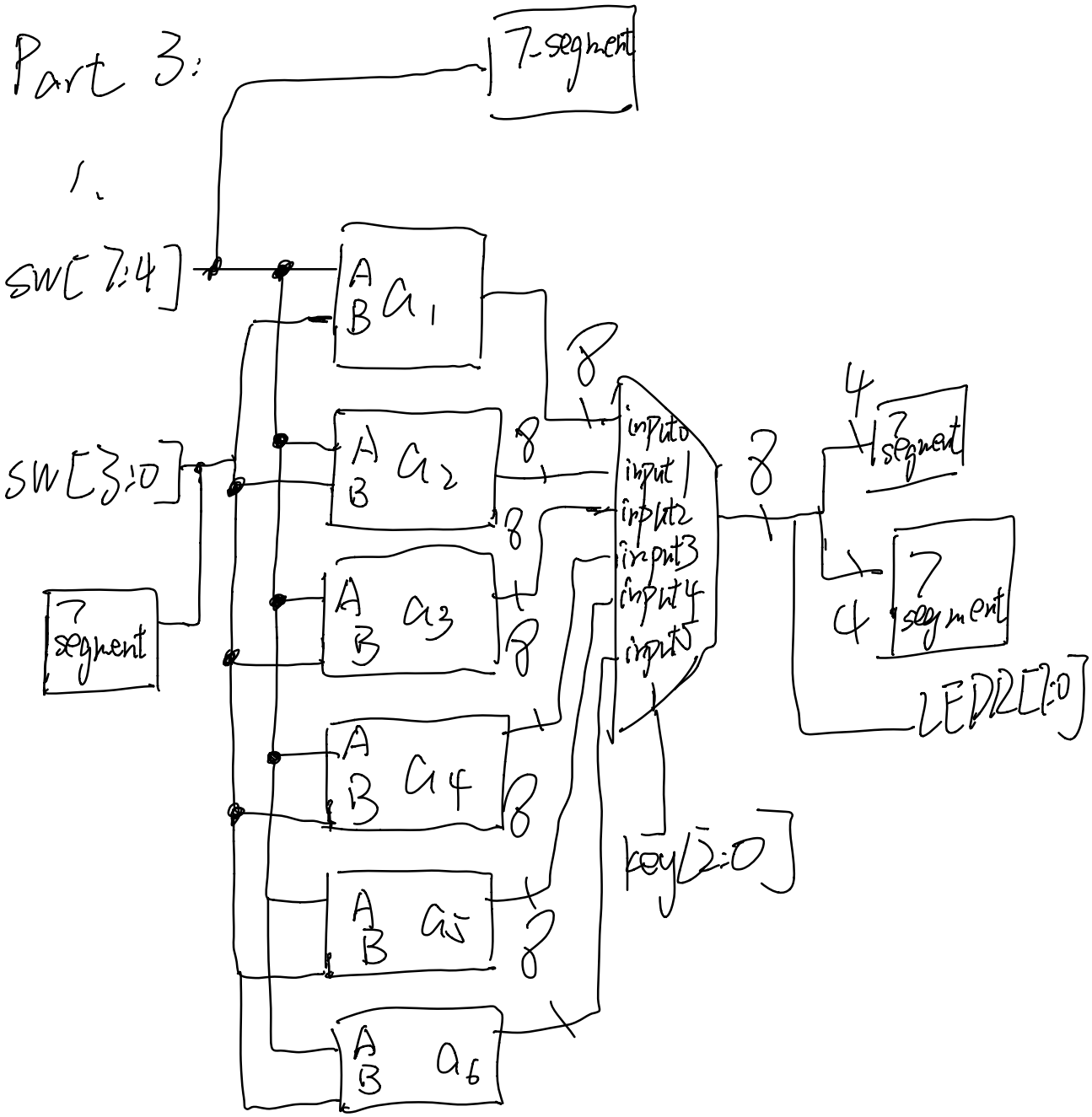
Part 2:

1. Draw schematic



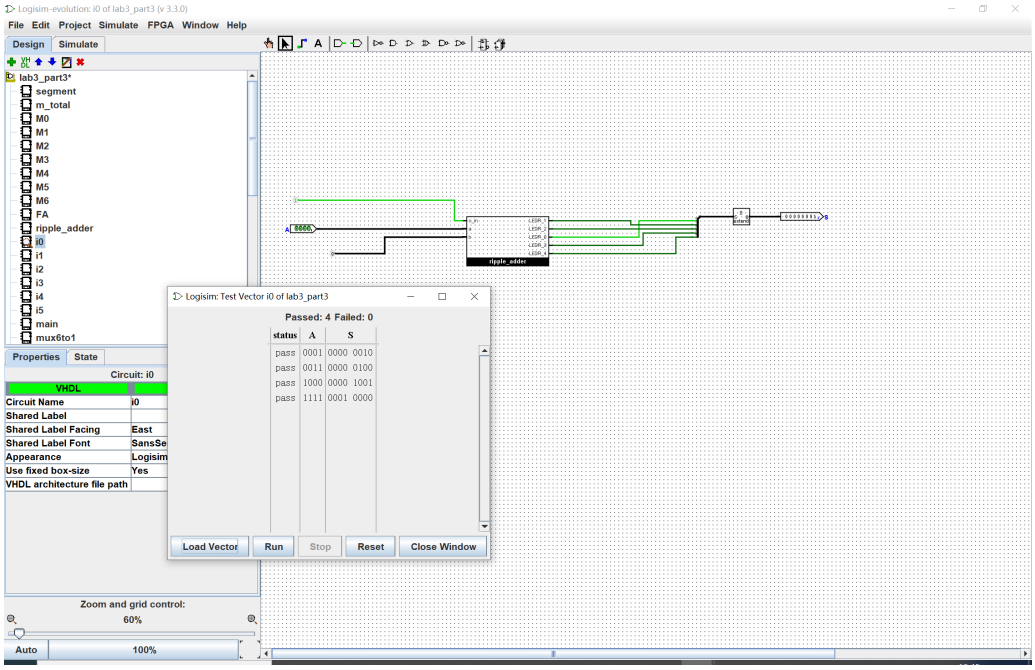
3. c


Logisim evolution: ripple_adder of lab3_part2 (v 3.3.0)
File Edit Project Simulate FPGA Window Help
Design Simulate
lab3_part2
FA
ripple_adder
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
TTL
TCL
BFH mega functions
Input/Output-Extra
System On Chip components
FA
c_in
a
b
LEDR_4
LEDR_3
LEDR_2
LEDR_1
LEDR_0
Logisim: Test Vector ripple_adder of lab3_part2
Passed: 7 Failed: 0
status a b c_in LEDR_4 LEDR_3 LEDR_2 LEDR_1 LEDR_0
pass 1111 1111 0 1 1 1 1 0
pass 1111 1111 1 1 1 1 1 1
pass 1000 1000 1 1 0 0 0 1
pass 1001 1000 0 1 0 0 0 1
pass 1001 1001 0 1 0 0 1 0
pass 0100 0100 1 0 1 0 0 1
pass 0010 0010 0 0 0 1 0 0
Load Vector
Run
Stop
Reset
Close Window
Auto
100%

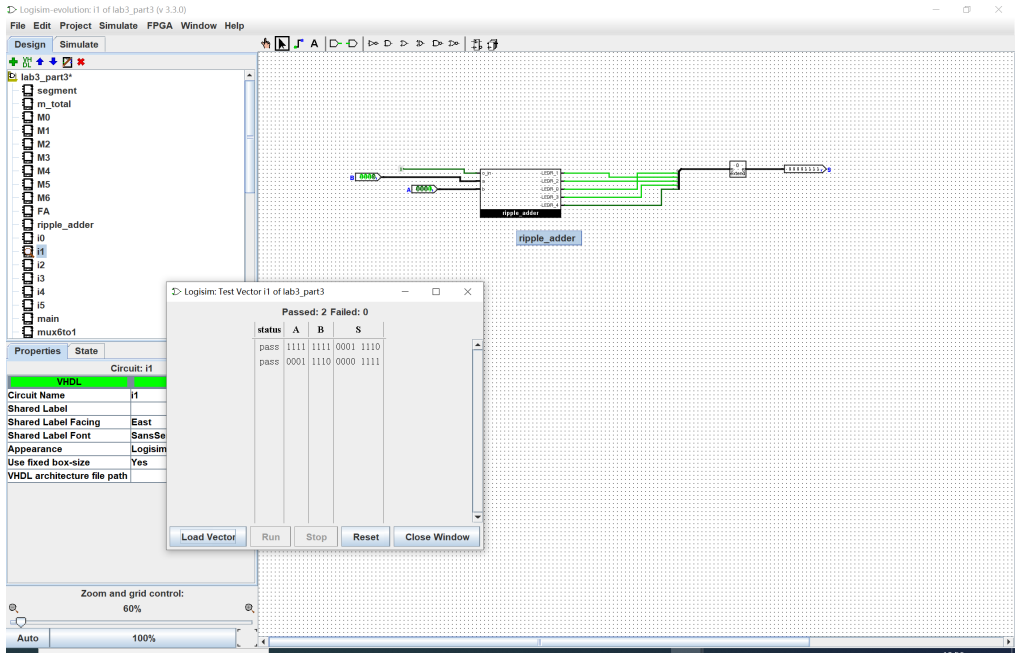

Part 3:
1.
7-segment
SW[7:4]
SW[3:0]
7 segment
A
B
A1
A2
A3
A4
A5
A6
8
input0
input1
input2
input3
input4
input5
4
7 segment
4
7 segment
LEDR[7:0]
key[2:0]

3.

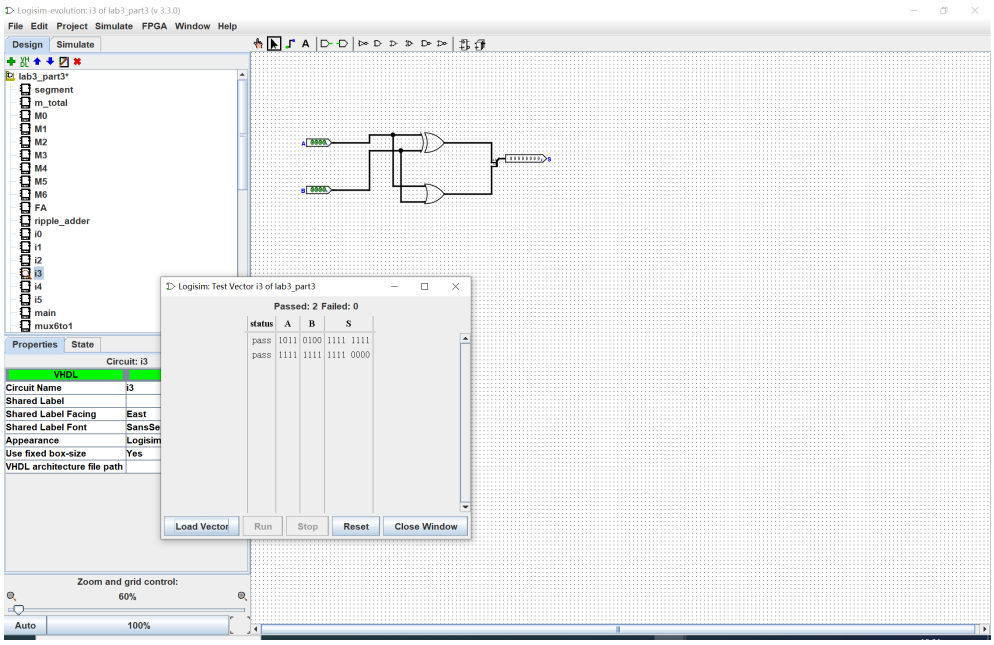
A_0:


Logisim-evolution: i0 of lab3_part3 (v 3.3.0)
File Edit Project Simulate FPGA Window Help
Design Simulate
lab3_part3*
segment
m_total
M0
M1
M2
M3
M4
M5
M6
FA
ripple_adder
i0
i1
i2
i3
i4
i5
main
mux6to1
Properties State
Circuit: i0
VHDL
Circuit Name i0
Shared Label
Shared Label Facing East
Shared Label Font SansSe
Appearance Logisim
Use fixed box-size Yes
VHDL architecture file path
Zoom and grid control:
60%
Auto 100%
Logisim: Test Vector i0 of lab3_part3
Passed: 4 Failed: 0
status A S
pass 0001 0000 0010
pass 0011 0000 0100
pass 1000 0000 1001
pass 1111 0001 0000
Load Vector Run Stop Reset Close Window
ripple_adder

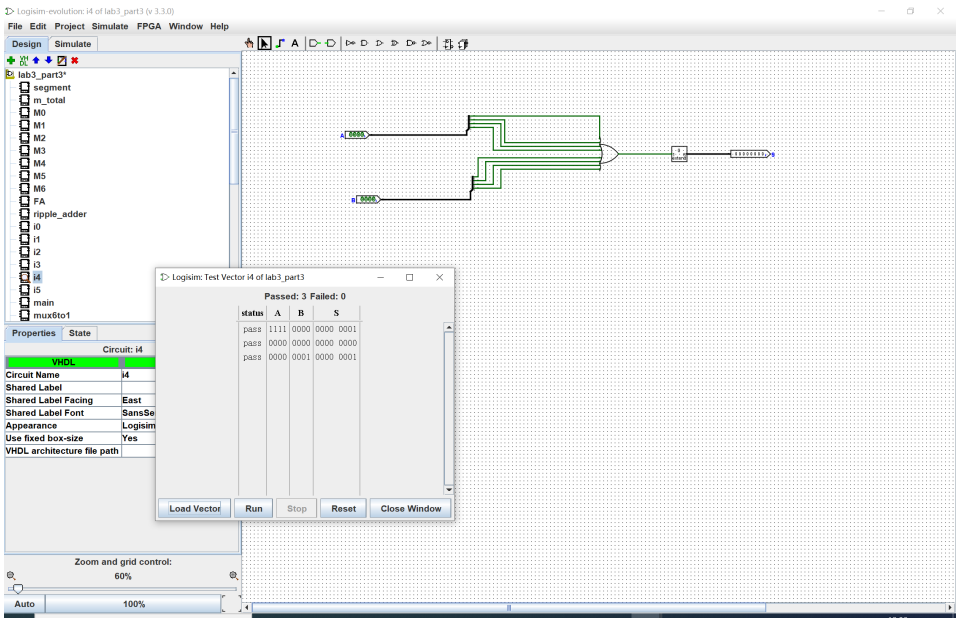
A_1, A_2:


Logisim-evolution: i1 of lab3_part3 (v 3.3.0)
File Edit Project Simulate FPGA Window Help
Design Simulate
lab3_part3*
segment
m_total
M0
M1
M2
M3
M4
M5
M6
FA
ripple_adder
i0
i1
i2
i3
i4
i5
main
mux6to1
Properties State
Circuit: i1
VHDL
Circuit Name i1
Shared Label
Shared Label Facing East
Shared Label Font SansSe
Appearance Logisim
Use fixed box-size Yes
VHDL architecture file path
Zoom and grid control:
60%
Auto 100%
Logisim: Test Vector i1 of lab3_part3
Passed: 2 Failed: 0
status A B S
pass 1111 1111 0001 1110
pass 0001 1110 0000 1111
Load Vector Run Stop Reset Close Window
ripple_adder

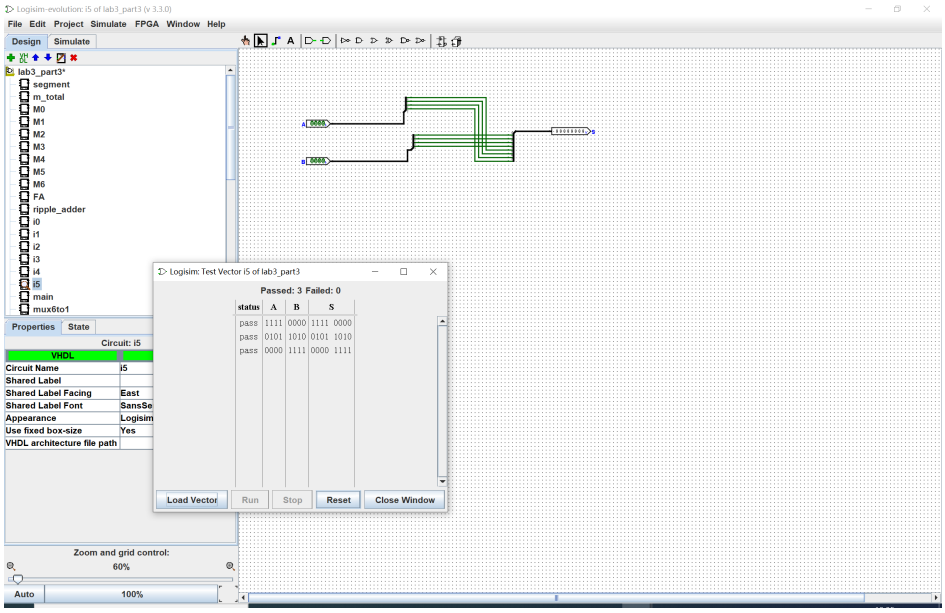
Q3 :


Logisim-evolution: i3 of lab3_part3 (v 3.3.0)
File Edit Project Simulate FPGA Window Help
Design Simulate
lab3_part3*
segment
m_total
M0
M1
M2
M3
M4
M5
M6
FA
ripple_adder
i0
i1
i2
i3
i4
i5
main
mux6to1
Properties State
Circuit: i3
VHDL
Circuit Name i3
Shared Label
Shared Label Facing East
Shared Label Font SansSe
Appearance Logisim
Use fixed box-size Yes
VHDL architecture file path
Zoom and grid control:
60%
Auto 100%
Logisim: Test Vector i3 of lab3_part3
Passed: 2 Failed: 0
status A B S
pass 1011 0100 1111 1111
pass 1111 1111 1111 0000
Load Vector Run Stop Reset Close Window

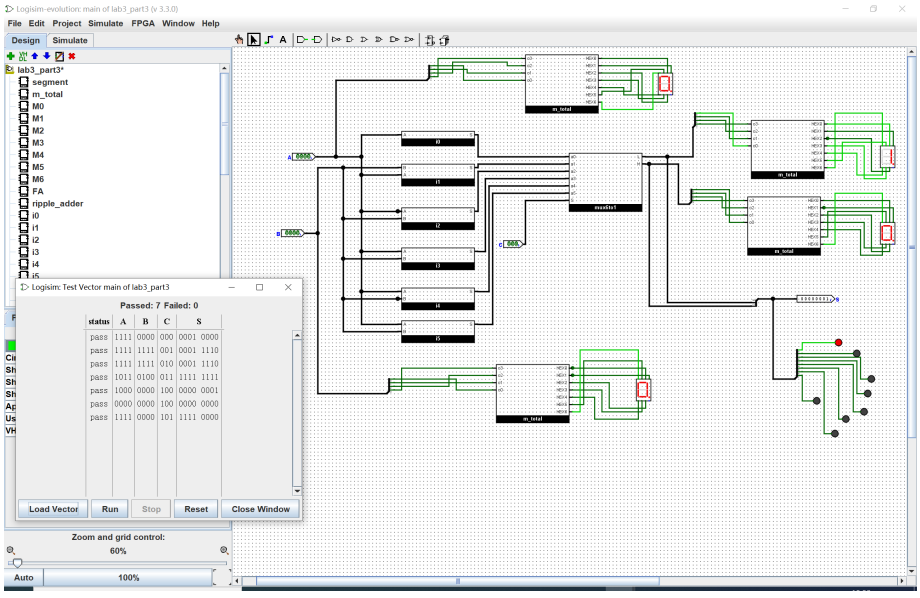
Q4 :


Logisim-evolution: i4 of lab3_part3 (v 3.3.0)
File Edit Project Simulate FPGA Window Help
Design Simulate
lab3_part3*
segment
m_total
M0
M1
M2
M3
M4
M5
M6
FA
ripple_adder
i0
i1
i2
i3
i4
i5
main
mux6to1
Properties State
Circuit: i4
VHDL
Circuit Name i4
Shared Label
Shared Label Facing East
Shared Label Font SansSe
Appearance Logisim
Use fixed box-size Yes
VHDL architecture file path
Zoom and grid control:
60%
Auto 100%
Logisim: Test Vector i4 of lab3_part3
Passed: 3 Failed: 0
status A B S
pass 1111 0000 0000 0001
pass 0000 0000 0000 0000
pass 0000 0001 0000 0001
Load Vector Run Stop Reset Close Window

i5:


Logisim-evolution: i5 of lab3_part3 (v 3.3.0)
File Edit Project Simulate FPGA Window Help
Design Simulate
lab3_part3*
segment
m_total
M0
M1
M2
M3
M4
M5
M6
FA
ripple_adder
i0
i1
i2
i3
i4
i5
main
mux6to1
Properties State
Circuit: i5
VHDL
Circuit Name i5
Shared Label
Shared Label Facing East
Shared Label Font SansSe
Appearance Logisim
Use fixed box-size Yes
VHDL architecture file path
Zoom and grid control:
60%
Auto 100%
Logisim: Test Vector i5 of lab3_part3
Passed: 3 Failed: 0
status A B S
pass 1111 0000 1111 0000
pass 0101 1010 0101 1010
pass 0000 1111 0000 1111
Load Vector Run Stop Reset Close Window

total:


Logisim-evolution: main of lab3_part3 (v 3.3.0)
File Edit Project Simulate FPGA Window Help
Design Simulate
lab3_part3*
segment
m_total
M0
M1
M2
M3
M4
M5
M6
FA
ripple_adder
i0
i1
i2
i3
i4
i5
Logisim: Test Vector main of lab3_part3
Passed: 7 Failed: 0
status A B C S
pass 1111 0000 000 0001 0000
pass 1111 1111 001 0001 1110
pass 1111 1111 010 0001 1110
pass 1011 0100 011 1111 1111
pass 1000 0000 100 0000 0001
pass 0000 0000 100 0000 0000
pass 1111 0000 101 1111 0000
Load Vector Run Stop Reset Close Window
Zoom and grid control:
60%
Auto 100%