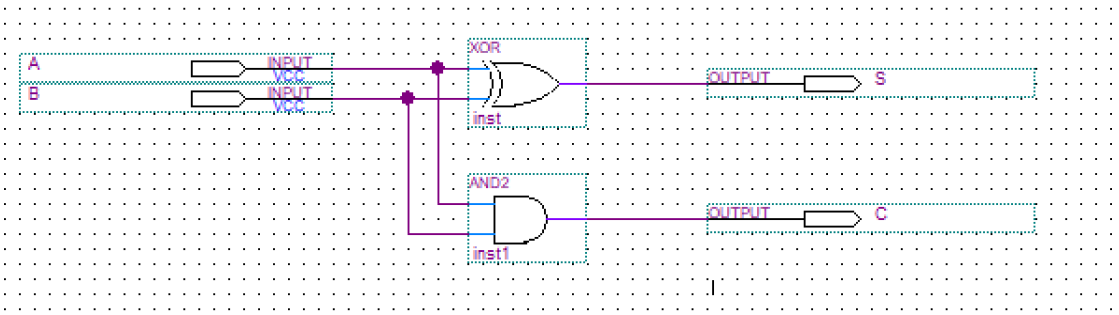
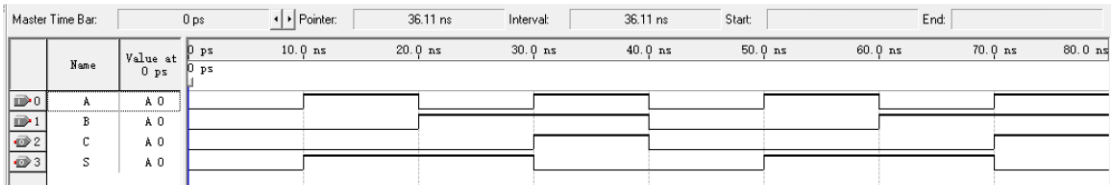
预习任务:

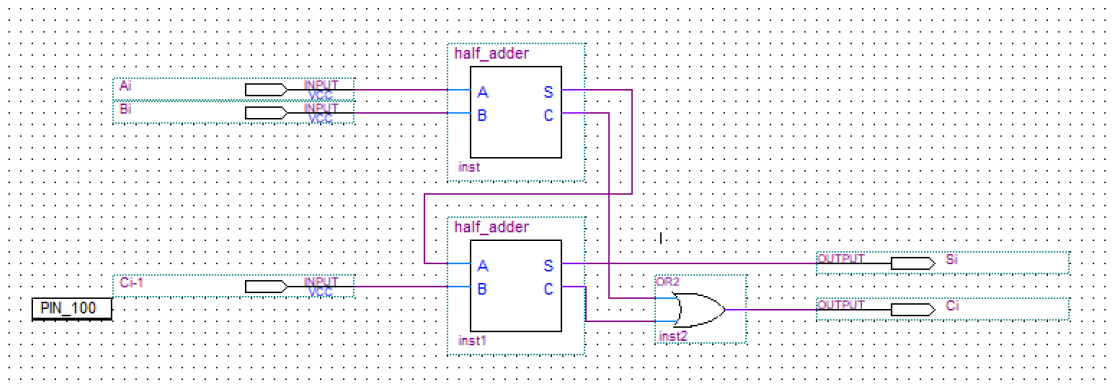
1，半加器



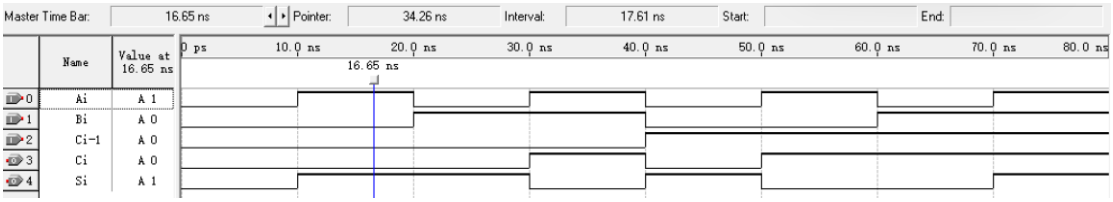
半加器仿真



2，全加器

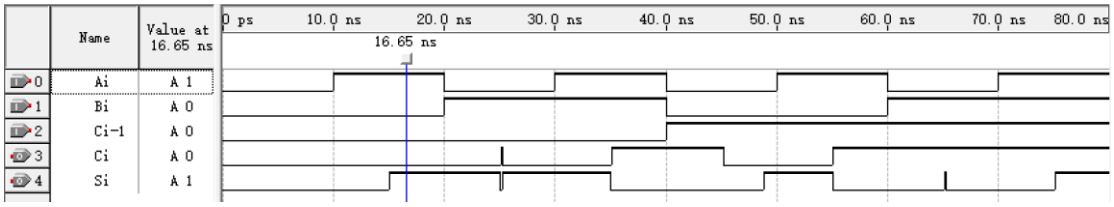


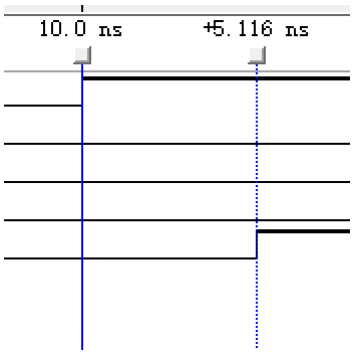
全加器仿真



半加器时序仿真

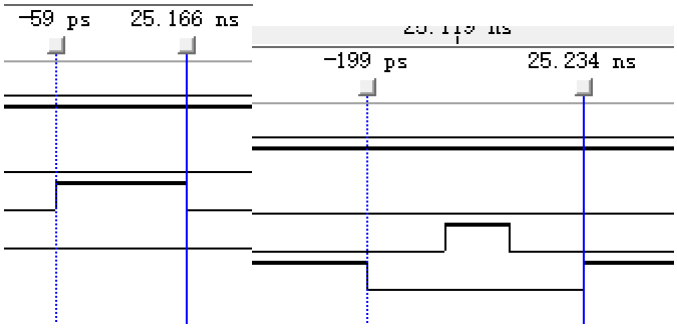
	Input Port	Output Port	RR	RF	FR	FF
1	Ai	Ci	5.095			5.166
2	Ai	Si	5.094	5.026	5.234	5.100
3	Bi	Ci	5.107			5.178
4	Bi	Si	5.107	5.035	5.234	5.114
5	Ci-1	Ci	8.870			9.011
6	Ci-1	Si	8.849	8.735	9.086	8.965



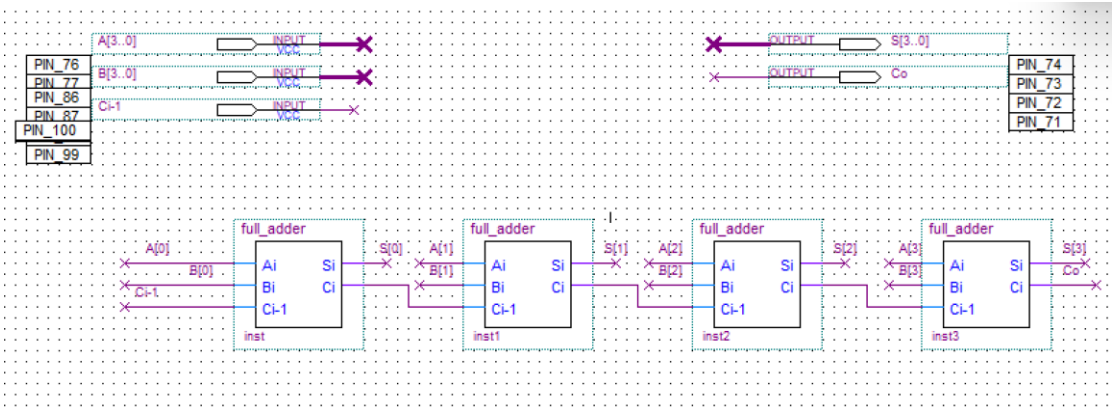


S 毛刺为 59ps

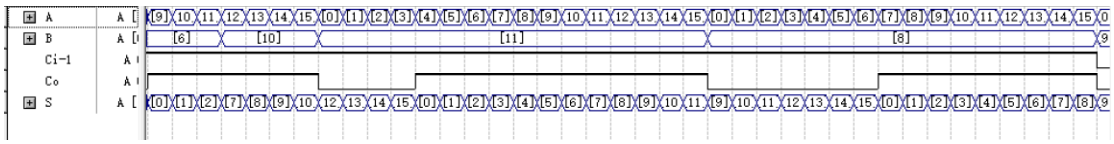
C 毛刺为 199ps



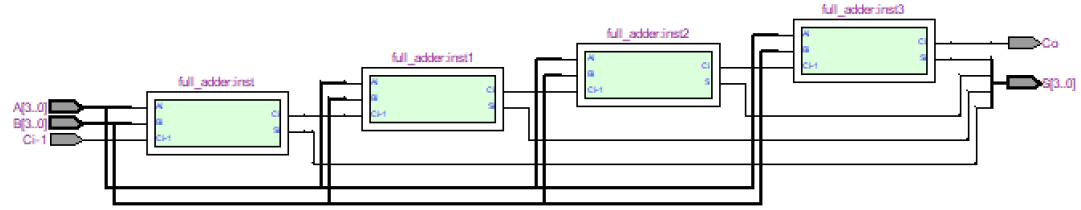
4 位行波加法器



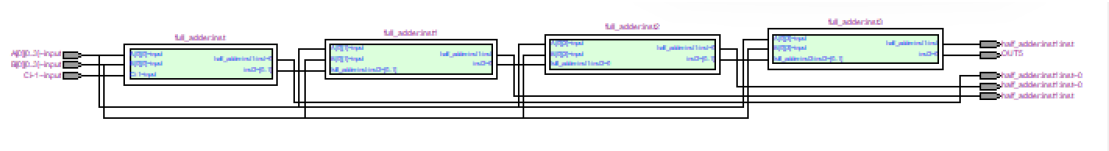
四位加法器仿真



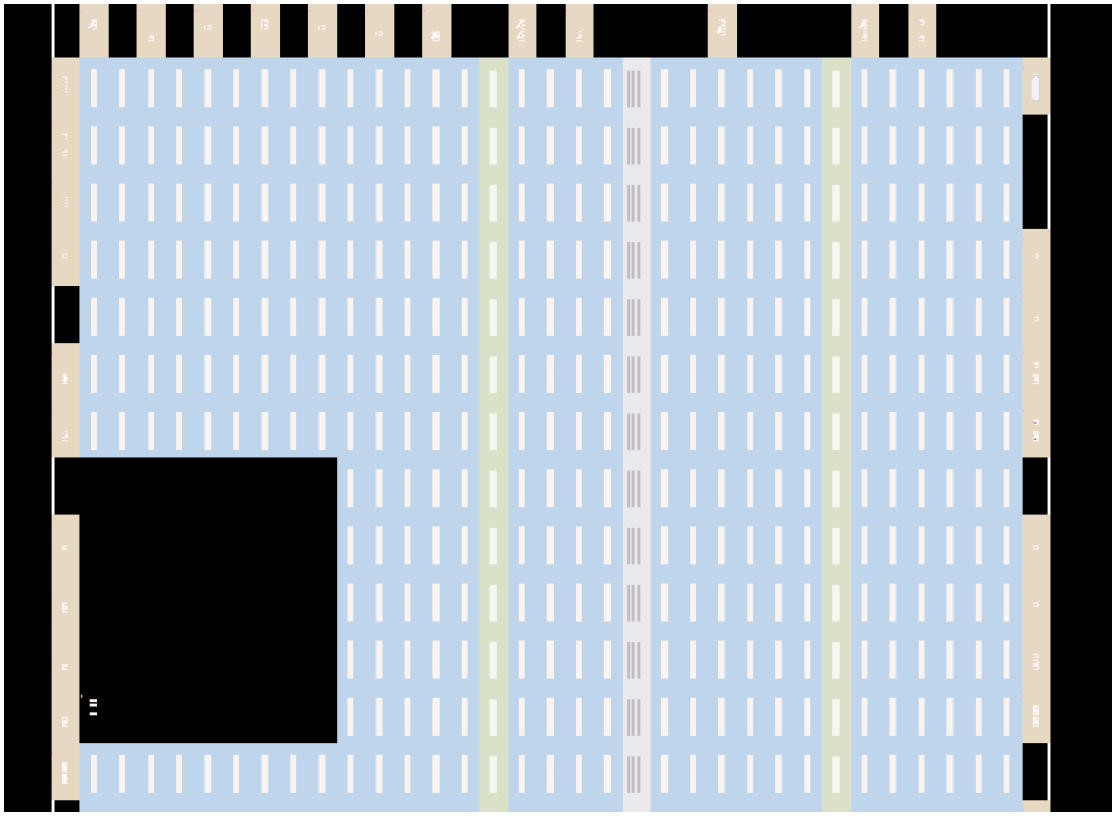
“RTL Viewer”查看电路综合结果



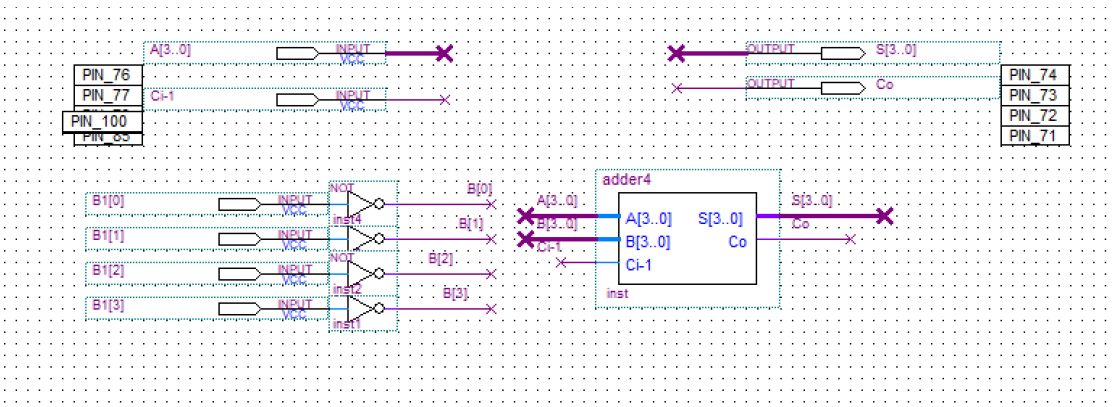
“Technology Map Viewer”查看电路 Map 结果



“Chip Planner”查看器件适配结果



全减器



全减器仿真