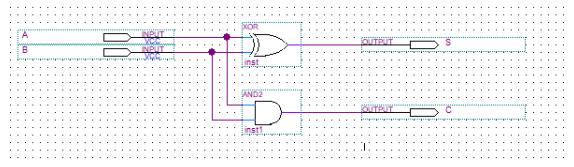
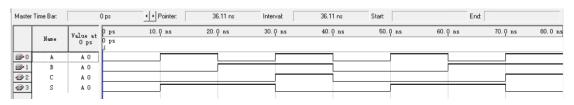
预习任务:

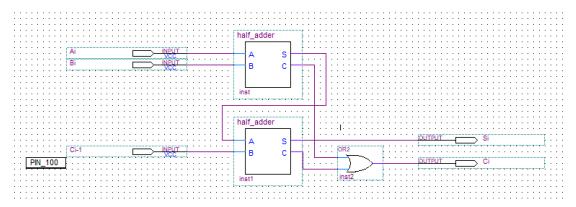
1、半加器



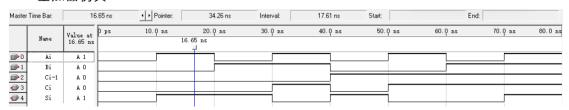
半加器仿真



2, 全加器



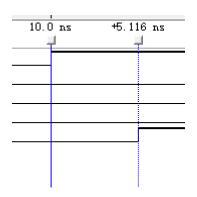
全加器仿真



半加器时序仿真

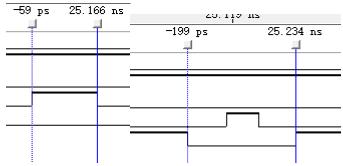
	Input Port	Output Port	RR	RF	FR	FF	
1	Αi	Ci	5.095			5.166	
2	Ai	Si	5.094	5.026	5.234	5.100	
3	Bi	Ci	5.107			5.178	
4 5	Bi	Si	5.107	5.035	5.234	5.114	
5	Ci-1	Ci	8.870			9.011	
6	Ci-1	Si	8.849	8.735	9.086	8.965	

		Value at	O ps	10.0 ns	20.0 ns	30.0 ns	40.0 ns	50.0 ns	60.0 ns	70.0 ns	80.0 ns
	Name	16.65 ns		16	.65 ns						
 0	Ai	A 1									
1 2 3 4	Bi	A O									
<u>■</u> 2	Ci−1	A O									
⊚ 3	Ci	A O									
€ 4	Si	A 1									

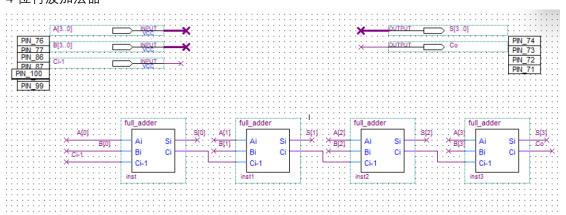


S 毛刺为 59ps

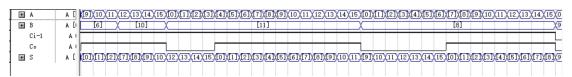
C 毛刺为 199ps



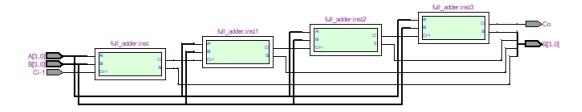
4 位行波加法器



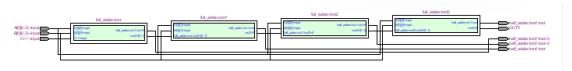
四位加法器仿真



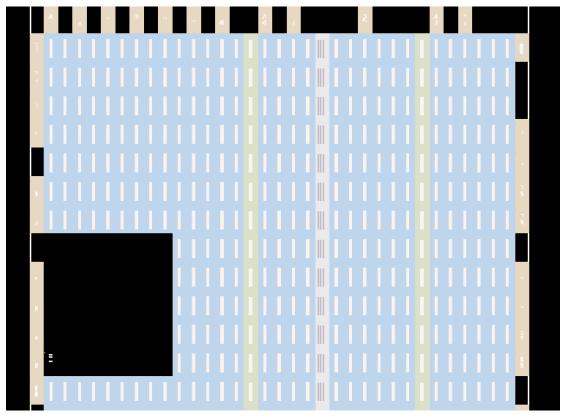
"RTL Viewer"查看电路综合结果



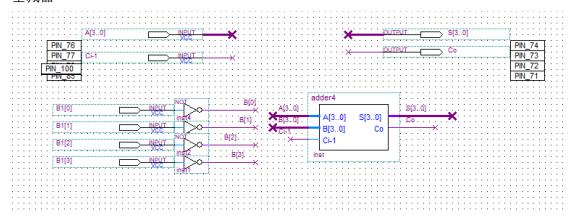
"Technology Map Viewer"查看电路 Map 结果



"Chip Planner"查看器件适配结果



全减器



全减器仿真

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¥ 5	₩ B1	[2]	[3]			[7]		X[4]
▶10	Ci-1							
№ 11	Co							\neg _
12	⊞ S	[1]\[2]\[3]\[4]\[5]\[6]\[7]\[8]\[9]\[10]\[11]\[12]\[13]	[14]	[11] [12] [13]	[14] [15]	(0) (1) (2)	X[3] X[4] X[5] X[6] X[7] X[[8] [12]