ELEC6234 – FPGA processor synthesis

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ABSTRACT: *A small picoMIPS architecture with a set of machine code for the affine transformation is presented. The design of the processor including program counter (PC), program memory (ROM), decoder, general purpose register (RAM) and* Arithmetic Logic Unit (ALU) *are discussed. The simulation results show this processor works properly to implement the affine transformation algorithm. And the processor is running properly on Altera DE0 development board. By this assignment, a clear understanding of picoMIPS architecture is gained and what benefits the learning of Embedded Processors.*

1. Introduction

The objectives of this assignment are to design an 8-bit picoMIPS architecture and implement an affine transformation algorithm on it. The design of this processor has to be as small as possible but sufficient to run the required algorithm.

An affine transformation is a geometrical transformation that preserves co-linearity. For 2-D images, it can be formulated below:
$\begin{bmatrix} x_2 \\ y_2 \end{bmatrix} = A \times \begin{bmatrix} x_1 \\ y_1 \end{bmatrix} + B$, where (x_1, y_1) are the coordinates of a pixel before the transformation and (x_2, y_2) – after the transformation. 2×2 matrix $A = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix}$ and two-element vector $B = \begin{bmatrix} b_1 \\ b_2 \end{bmatrix}$ provide the transformation coefficients.

Therefore, the formula can also be expressed as: $\begin{cases} x_2 = a_{11} \cdot x_1 + a_{12} \cdot y_1 + b_1 \\ y_2 = a_{21} \cdot x_1 + a_{22} \cdot y_1 + b_2 \end{cases}$
In addition, set the coefficients of matrix A are 2's complement signed fixed-point fractions in the range -1 ... +1 – 2^{-8}, while B in the range -128...127, and both of them are 8-bit format. In this implementation, the selected data sets are:

$A = \begin{bmatrix} 0.75 & 0.5 \\ -0.5 & 0.75 \end{bmatrix}$, $B = \begin{bmatrix} 20 \\ -20 \end{bmatrix}$, Thus the implementation should be: $\begin{cases} x_2 = 0.75 \cdot x_1 + 0.5 \cdot y_1 + 20 \\ y_2 = -0.5 \cdot x_1 + 0.75 \cdot y_1 - 20 \end{cases}$

The formula above clearly shows there are four multiplications and two addition in total. According to this, the ALU (Arithmetic Logic Unit) just need an adder and a multiplier. Thus 2-bit operation code is enough.

What is more, there are some embedded multipliers in the FPGA, only one is needed, which is able to make the design much smaller. Besides, due to the pattern of calculation, at least four 8-bit GPR (general purpose register) needed to store the result from each process.

Then the width of instruction should be 14-bit included one 2-bit operation code, two 2-bit address code, and one 8-bit immediate or address code. So the decoder is 6-bit, the program memory should be 32×14-bit and with 5-bit program counter (up to 32 instructions).

2. Instruction format, decoder design, program memory and program counter

The block diagram of my picoMIPS design is shown below:

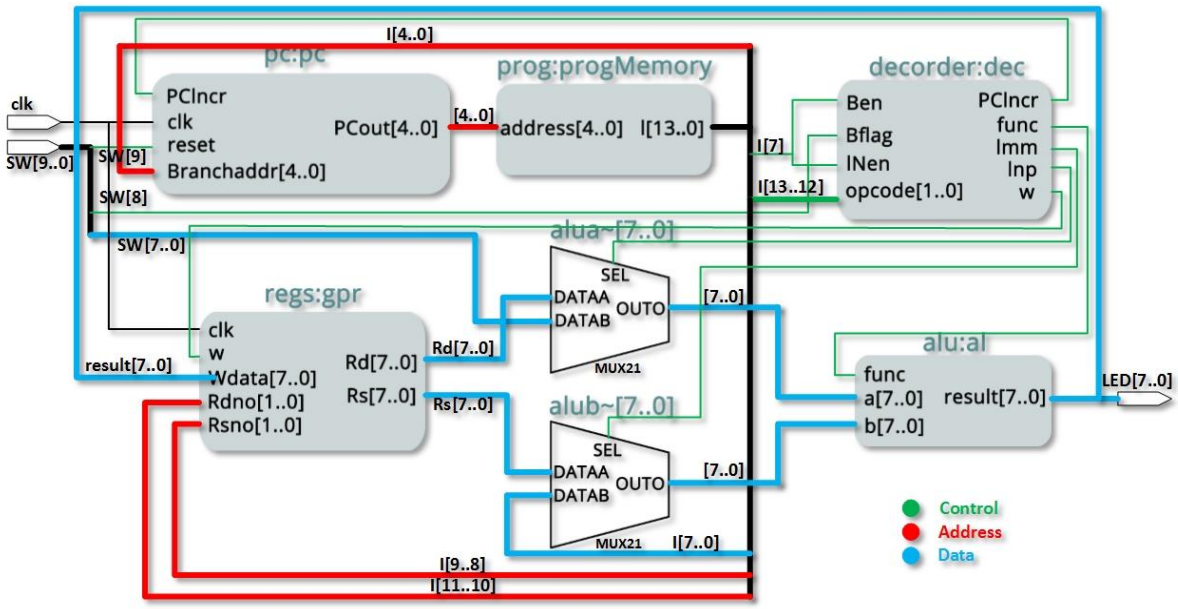

Figure 1 the block diagram of my picoMIPS

2.1 Instruction set

Although there are only four operation codes, there are more than four functions. The instruction format is shown below.

Instruction	Bit 13-12 (opcode)	Bit 11-10 (destination register)	Bit 9-8 (source register)	Bit 7-0 (Data/Address/Flag)	Description	
ADD	2'b00	Rdno	Rsno	a, 7'bxxxxxxx	a = 0	ADD %d, %s; %d = %d + %s
					a = 1	INP %d, d%; %d = input num
ADDI	2'b01	Rdno	Rsno	8-bit operand	ADDI %d, %s, operand; %d = %s +operand	
MULI	2'b10	Rdno	Rsno	8-bit operand	MULI %d, %s, operand; %d = %s * operand	
B	2'b11	Rdno	Rsno	b, 2'b00, 5-bit address	b = 0	if (SW[8] == 0) branch to address
					b = 1	if (SW[8] == 1) branch to address

Table 1 Instruction format table

As shown in Table 1 above, three of four instruction is multi-functional. To be detailed, if bit 7 of ADD instruction is 1, the ADD will act as input to store the input value from switches to GPR. ADD can also act as NOP if all the bits are 0. Moreover, MULI is used to multiply the input number with matrix A. It can also use to clear the destination register by multiply 0 with the source register.

Plus, B is used to branch 'PCout' to target address. If the value of handshaking functionality SW [8] is same as the bit 7 of B, then branching to the address set in bit 4-0, which supplies flexibility. All of the four instructions are fully used in the implementation of the affine transformation algorithm.

2.2 Decoder design

The decoder is used to decode the operation code then control relative operation or select the specific function. It is used in every clock cycle, controlling the operation of the processor.

The full code of decoder is in attached zip file. The test bench code and simulation result is shown at below.

```
module decodertest;
logic [1:0] opcode;
logic Bflag, Ben, INen;
logic PCincr,func, inp, imm,w;

decoder  D (.opcode(opcode), // Instruction opcode
            .Bflag(Bflag),
            .Ben(Ben),
            .INen(INen),
            .PCincr(PCincr),
            .func(func), // ALU function
            .inp(inp), // Input port select
            .imm(imm), // immediate operand select
            .w(w)); // Write to registers
initial
    begin
        Bflag = 0; Ben = 0; INen = 0;
        #10 opcode = 2'b00; //ADD
        #10 INen = 1;
        #10 opcode = 2'b01; //ADDI
        #10 opcode = 2'b10; //MULI
        #10 opcode = 2'b11; //B
        #5  Ben = 1; Bflag = 0;
        #5  Ben = 0; Bflag = 1;
        #5  Ben = 1; Bflag = 1;
    end //initial
endmodule //module decodertest ----------------------
```

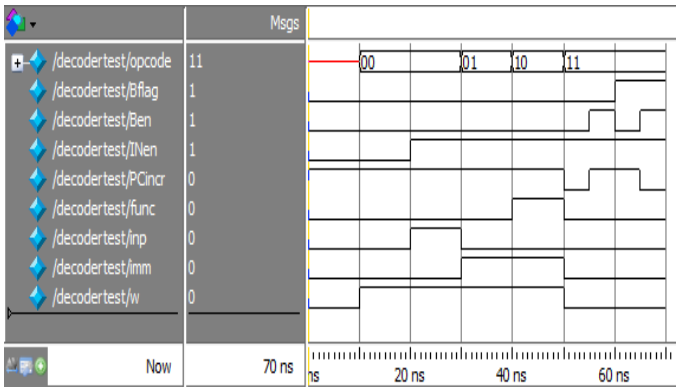

Figure 2 Decoder test bench and simulation waveform

The waveform indicates when the signal 'INen' (bit 7 of instruction) is 1, the ADD will be INP when the signal 'inp' is activated. Besides, when running the operation 'B', whether branching (PCincr is 1 or 0) to target address is dependent on if the 'Bflag' equals to 'Ben'. Moreover, the 'imm' and 'w' are the control signals to control immediate operand and write enable of general purpose register. While 'func' is ALU code to select the function of ALU (0 for addition and 1 for multiplication). The simulation result proved the decoder fully working.

2.3 Program memory design

```
//HEX///BINARY ////////////////// ASSEMBLER ////////////////////////////////
2000//0: 14'b10_00_00_00000000; //MULI 0 //CLEAR %0
3001//1: 14'b11_00_00_00000001; //B 0 PC=1
0080//2: 14'b00_00_00_10000000; //ADD  %0; %0 = inport x1
0480//3: 14'b00_01_00_10000000; //ADD  %1; %1 = inport x1
3084//4: 14'b11_00_00_10000100; //B 1 PC=4
3005//5: 14'b11_00_00_00000101; //B 0 PC=5
0880//6: 14'b00_10_00_10000000; //ADD  %2; %2 = inport y1
0C80//7: 14'b00_11_00_10000000; //ADD  %3; %3 = inport y1
3088//8: 14'b11_00_00_10001000; //B 1 PC=8
2060//9: 14'b10_00_00_01100000; //MULI %0, %0, 0.75; %0 = %0 * 0.75 // 0.75x1
25C0//10:14'b10_01_01_11000000; //MULI %1, %1, -0.5; %1 = %1 * -0.5 // -0.5x1
2A40//11:14'b10_10_10_01000000; //MULI %2, %2, 0.5; %2 = %2 * 0.5 // 0.5y1
2F60//12:14'b10_11_11_01100000; //MULI %3, %3, 0.5; %3 = %3 * 0.75 // 0.75y1
0200//13:14'b00_00_10_00000000; //ADD %0, %2; %0 = %0 + %2 // 0.75x1 + 0.5y1
0D00//14:14'b00_11_01_00000000; //ADD %3, %1; %3 = %3 + %1 // 0.75y1 - 0.5x1
1014//15:14'b01_00_00_00010100; //ADDI %0,  20;//%0 =%0+20//x2=0.75x1+0.5y1+20
3010//16:14'b11_00_00_00010000; //B 0 PC = 16
2000//17:14'b10_00_00_00000000; //MULI 0 //CLEAR %0
0300//18:14'b00_00_11_00000000; //ADD %0, %3; %0 = %0 + %3//y2=0.75x1+0.5y1+20
10EC//19:14'b01_00_00_11101100; //ADDI %0, -20; //%0 = %0 - 20 //DISP
3094//20:14'b11_00_00_10010100; //B 1 PC = 20
////////////////////////////////////////////////////////////////////////////////
```

Figure 3 Machine code of affine transformation algorithm

Program memory is a read-only memory (ROM) where stores the machine code for the affine transformation algorithm. The address width is 5-bit thus there could be up to 32 instructions stored in.

The whole list of machine code is shown at left, which took only 21 instructions. Moreover, this program is written following the pseudo code in assignment requirement.

The handshaking is implemented by branch, when 'Bflag' (SW[8]) is equal to 'Ben' (Bit 7 of instruction), the PC will output the address of bit 4 to 0.

In order to implement the functions $\begin{cases} x_2 = 0.75 \cdot x_1 + 0.5 \cdot y_1 + 20 \\ y_2 = -0.5 \cdot x_1 + 0.75 \cdot y_1 - 20 \end{cases}$, there are four registers (%0 ~ %3) needed to store the result of $0.75 \cdot x_1$, $(-0.5 \cdot x_1)$, $0.5 \cdot y_1$ and $0.75 \cdot y_1$, then add %0 with %2, %1 with %3. Afterwards add 20 to %0. The result of x2 is in %0. Then the result in %3 need to be moved to %0 and add (-20) in order to display.

In addition, the machine code can be save as hex file 'prog.hex' and called by command $readmemh("prog.hex", progMem). This could make it easier to write machine code and clearly show the code logic by adding comments aside.

2.4 Program counter design

```
module pctest;
logic clk;
logic reset;
logic PCincr;
logic [5:0] Branchaddr;
logic [5:0] PCout;
    pc #(.Psize(5)) pc (.clk(clk),
                        .reset(reset),
                        .PCincr(PCincr),
                        .Branchaddr(Branchaddr),
                        .PCout(PCout));/
initial
    begin
       clk = 1'b0;
       forever #5ns clk = ~clk;
    end
initial
    begin
        reset = 0; PCincr = 0; Branchaddr = 5'b0;
        #10 reset = 0; PCincr = 1;
        #10 reset = 1;
        #30 PCincr = 0; Branchaddr = 5'b01100;
        #10 reset = 1; PCincr = 1;
        #30 reset = 0;
        #10 reset = 1;
    end
endmodule //module pctest ----------------------
```

Program counter (PC) is used to drive the output of machine codes by address. The address width of it is 5-bit thus there could be up to 32 instructions in a loop.

The full code of program counter is in attached zip file. The test bench is shown at left.

The PC is driven by clock signal. When signal 'PCincr' is 1, the counter output will plus one in each clock cycle. If 'PCincr'is 0, the output will stuck at 'Branchaddr' until it turned to 1. And the activate low reset is used to turn counter output to 0. The simulation waveform is shown below.

In the waveform it is clear shown when 'PCincr' is 0 the 'PCout' is turned into 'Branchaddr'-12. Then 'reset' is activated to make 'PC' restart from 0. Moreover, when 'PCincr' is 1 and 'reset' is 0, the 'PCout' pluses one at each positive edge of clock signal. Thus it proved the program counter working.

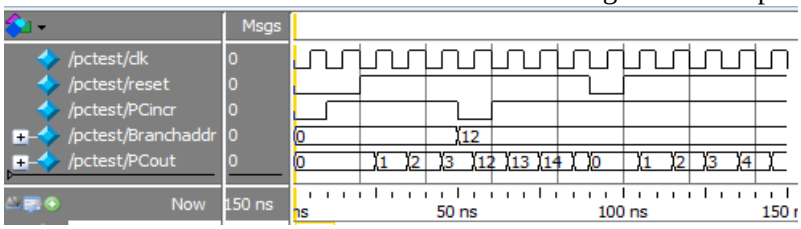

Figure 4 PC test bench and simulation waveform

2.5 Synthesis

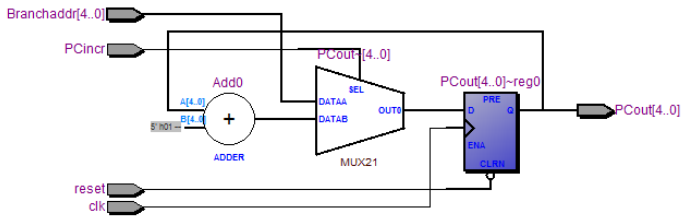

Figure 5 Synthesis of Program Counter

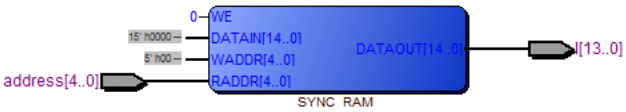

Figure 6 Synthesis of Program Memory

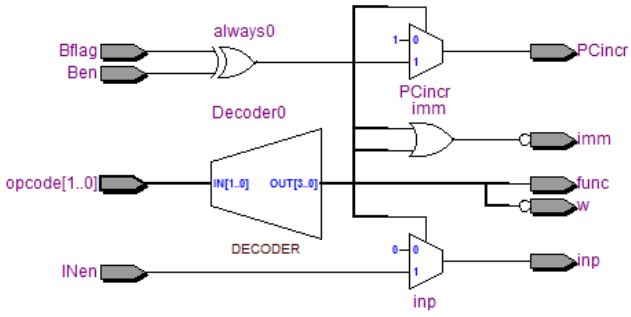

Figure 7 Synthesis of Decoder

The synthesis of PC, Program Memory and Decoder are shown at left.

In PC, an adder is used to count the address by adding one at each cycle. There is a 5-bit multiplexer to branch the address to the target.

The Program Memory is synthesised as a synchronous RAM block, but this RAM is implemented by logic elements (LE) rather than embedded M9K RAM blocks. This could be modified in the future. It acts as a ROM in this system.

As a controller, the Decoder sends control signal to other modules. What should be noticed is the decoder also handle the handshaking signal 'Bflag' which is from SW[8] . Moreover, the bit 7 of instruction are multi-functional which is also integrated in the Decoder module.

3. General Purpose Register file design, simulation and synthesis

The general purpose register (GPR) acts as random-access memory (RAM), used to store the operands in the processing of data. In this design, the GPR has four 8-bit registers to store the data. It has dual output bus where addressed as destination (Rdno) and source (Rsno) in this GPR. The first register %0 (Address 2'b00) is always 0 if it is used as source. The code of GPR and test bench is shown below.

```
module regs #(parameter n = 8)
      (input logic clk, w, //reset, clk and write control
       input logic [n-1:0] Wdata,
       input logic [1:0] Rdno, Rsno,//2-bit register number
       output logic [n-1:0] Rd, Rs);
// Declare 4 n-bit registers
logic [n-1:0] gpr [3:0];
// write to dest reg Rd, if w==1
always_ff @ (posedge clk)//or negedge reset)
    begin
        if (w)
            gpr[Rdno] <= Wdata;
    end
always_comb
    begin
    // dual output bus: Rd and Rs
        Rd = gpr[Rdno];
    //if %0 is selected as Rs(Rsno==0)then Rs is 0
        Rs = (Rsno==2'b00 ? {n{1'b0}} : gpr[Rsno]);
    end
endmodule // module regs
```

Figure 8 Source code and test bench of GPR

```
module regstest;
parameter n = 8;
logic clk, w;
logic [n-1:0] Wdata;
logic [1:0] Rsno,Rdno;
logic [n-1:0] Rs, Rd;

    regs #(.n(8)) gpr (.clk(clk),.w(w),
                       .Wdata(Wdata),
                       .Rdno(Rdno),
                       .Rsno(Rsno),
                       .Rd(Rd),.Rs(Rs));
    initial
        begin
          clk =  0;
          #5ns  forever #5ns clk = ~clk;
        end

    initial
        begin
            w = 1;
            Rdno = 2'b00; Wdata = 8'd10;
        #10 Rdno = 2'b01; Wdata = 8'd11;
        #10 Rdno = 2'b10; Wdata = 8'd12;
        #10 Rdno = 2'b11; Wdata = 8'd13;
        #10 w = 0;
        #10 Rdno = 2'b00;Rsno = 2'b00;
        #10 Rdno = 2'b01;Rsno = 2'b01;
        #10 Rdno = 2'b10;Rsno = 2'b10;
        #10 Rdno = 2'b11;Rsno = 2'b11;
        end
endmodule
```

The signal 'w' is write control, when 'w' is 1 the 8-bit data from 'Wdata' will be stored in the appointed destination address (Rdno). The input is synchronous.

There are two outputs Rd and Rs in this GPR, both of them are asynchronous, which only depend on the address of Rdno and Rsno.

In simulation, the idea is first to store four values (15, 16, 17, 18) into register %0, %1, %2 and %3. Then check the dual output bus by each address. What should be noticed is the output of Rs at address 2'b00 (%0) should be 0. The waveform is shown in Figure 6. The results proved the GPR working.

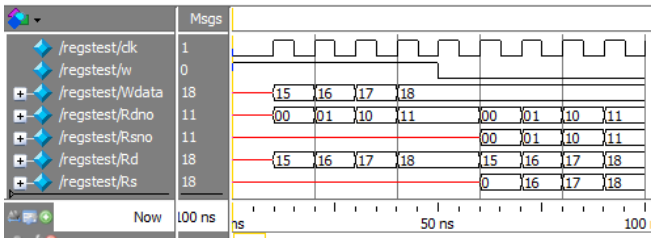

Figure 9 GPR simulation waveform

The synthesis result is shown below. The basic architecture of this GPR is a synchronous RAM with a multiplexer to make Rs output 0 when the address is 2'b00.

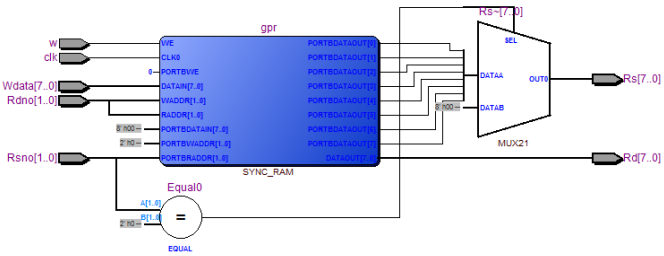

Figure 10 the synthesis of GPR

Overall, the general purpose register is actually a RAM which stores the operands. What should be focus is the GPR could also be implemented by embedded RAM blocks. In order to get a better use of the resources on chip, it is necessary to attempt to use the embedded blocks rather than use logic elements to build all.

4. Arithmetic Logic Unit and Multiplier design

There are two ways to design an Arithmetic Logic Unit (ALU). One is to make a complex ALU where a complex process could be achieved in on step. The other is to make it simple and some complex computing processes should be distributed into several simple computing.

In terms of the main objective of this assignment is to design a picoMIPS architecture which is sufficient to implement affine transformation algorithm (which contains only addition and multiplication). It seems better to design a simple ALU where are only an adder and a multiplier inside. This may make the algorithm processing complex but the total architecture of ALU will be very small.

Therefore in this design there are only two functions, add and multiply. The adder is an 8-bit adder while the multiplier is the embedded 9×9 signed multiplier (used to implement 8×8 signed multiplication). The source code is shown below.

```
module alu #(parameter n =8)
            (input logic signed [n-1:0] a, b,
             input logic func,
             output logic signed [n-1:0] result);

//------------- code starts here ---------
logic signed [n-1:0] ar; // add result
logic signed [15:0] mr; //mul result

always_comb
    begin
        if(func == `RMUL)
            mr = a * b;// embedded mul
        else
            mr = 0;

        if(func == `RADD)
            ar = a + b;
        else
            ar = 0;// n-bit adder
    end // always_comb

// create the ALU
always_comb
    begin
        result = a; // default
        case(func)
            `RADD:
                begin
                    result = ar;
                end

            `RMUL:
                begin
                    result = mr[14:7];
                end
        endcase
    end //always_comb
endmodule //end of module ALU
```

Figure 11 Source code of ALU

In the multiplication, the multiplicand is 2's complement integer while the multiplicator is 2's complement signed fixed-point fractions. The result of 8-bit ×8-bit is 16bit.

However, only bit 14 to 7 is needed because the result must be 8-bit integer. What is more, all the variables need to be declared as signed in order to compute them with signs.

Besides, the signal 'func' is from Decoder by decoding the operation code of instructions to select either add or multiply is used.

To test such a simple ALU, it just need to set the 'func' signal and input operands 'a' and 'b'. Then check if the result is correct. Thus it is necessary to set a test table, shown below.

Function	a	b	result
+	10	16	26
	-10	16	6
	10	-16	-6
	-10	-16	-26
×	16	0.5	8
	72	-0.25	-18
	-64	0.5	32
	-32	-0.5	16

Table 2 Test table for ALU

According to Table 2, the test bench can be designed as below.

```
module alutest;
logic signed [7:0] a, b;
logic func;
logic signed [7:0] result;
alu #(.n(8))
al (.a(a), .b(b),.func(func),
 .result(result));
initial
    begin
    func = `RADD;a='0;b='0;
#10 a=8'b00001010;//10+16
    b=8'b00010000;//=26

#10 a=8'b11110110;//-10+16
    b=8'b00010000;//=6

#10 a=8'b00001010;//10-16
    b=8'b11110000;//=-6

#10 a=8'b11110110;//-10-16
    b=8'b11110000;//=-26

#10 func = `RMUL;a='0;b='0;
#10 a=8'b00010000;//16*0.5
    b=8'b01000000;//=8

#10 a=8'b01001000;//72*-0.25
    b=8'b11100000;//=-18

#10 a=8'b11000000;//-64*0.5
    b=8'b01000000;//=-32

#10 a=8'b11100000;//-32*-0.5
    b=8'b11000000;//=16
    end
endmodule
```

Figure 13 Test bench for ALU

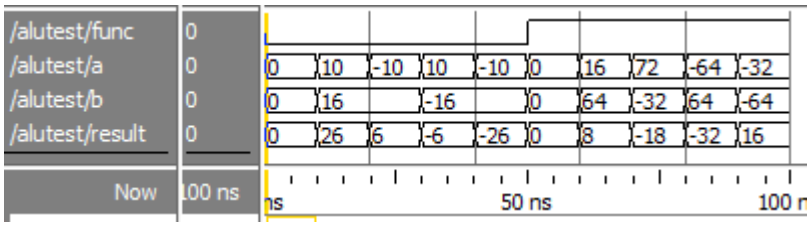

Figure 12 Simulation waveform of ALU

The figure above is the simulation result of the test.

There should be mentioned when function is additon (func is 0), both ‘a’ and ‘b’ are integer, but when it is multiplication, ‘a’ is integer and ‘b’ is fraction. Thus when the signal ‘func’ goes high (means it is in the multipilication), the numbers of b such as ‘64’, ’-32’, ‘64’, ‘-64’ are actually ‘0.5’, ’-0.25’, ‘0.5’, ‘-0.5’ according to 2’s complement signed fixed-point fraction. Therefore the results are all correct, which indicates the ALU is fully functional and it is sufficient used to implement the affine transformation algorithm.

The synthesis of ALU is shown below, it is clear that there are only one adder and one multiplier inside.

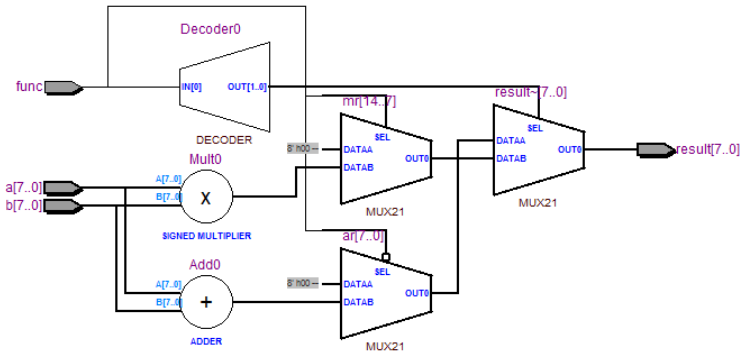

Figure 14 the synthesis of ALU

By now, all of the design and simulation works are done, next step is to implement the whole system on the FPGA. There are two kinds of FPGA development boards can be chosen, one is Altera DE0 and the other is Altera DE2. Due to the size of picoMIPS is very small, both of them are able to do this job. In this report, take Altera DE0 as the experimental platform.

5. Altera DE0 implementation

In order to implement the picoMIPS design on FPGA, a top-level module is needed to combine all of the modules into a picoMIPS processor. In addition, as shown in Figure 1, there are two multiplexer used to select input and immediate numbers. And the synthesis result is exactly like the block diagram in Figure 1, shown below:

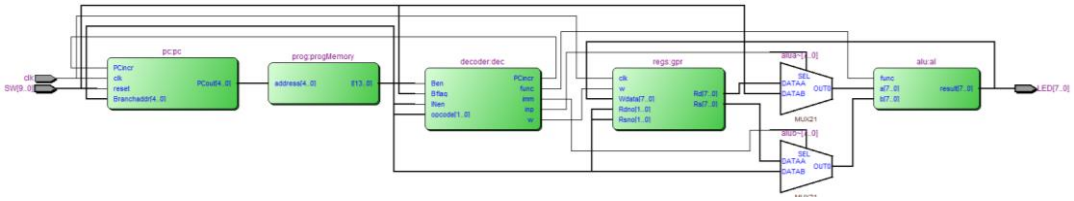

Figure 15 the synthesis of picoMIPS

Before testing, there is a counter supplied by assignment to divide the 50MHz clock frequency into around 10Hz. The purpose of the clock divider is to eliminate bouncing effects of the mechanical switches which are used to input data.

Therefore the whole structure is shown below:

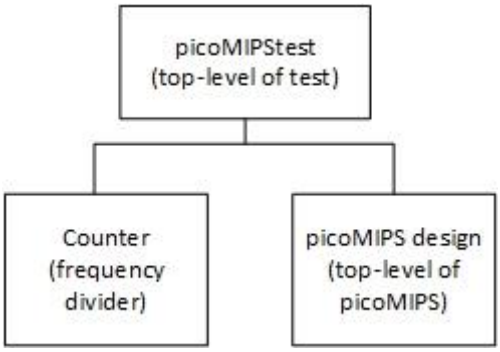

Figure 16 the structure of lab test

After programming the FPGA, there should be a test to evaluate the performance of processor and the accuracy of algorithm. The specific algorithm is shown below:

$$\begin{cases} x_2 = 0.75 \cdot x_1 + 0.5 \cdot y_1 + 20 \\ y_2 = -0.5 \cdot x_1 + 0.75 \cdot y_1 - 20 \end{cases}$$

To design an experiment table is always a good start, shown below.

INPUT		OUTPUT (theoretical value)		OUTPUT (actual value)	
x1	y1	x2	y2	x2	y2
21 (8'b00010101)	29 (8'b00011101)	50.25 (8'b00110010)	-8.75 (8'b11111000)	8'b00110001	8'b11110110
-128 (8'b10000000)	60 (8'b00111010)	-46 (8'b11010010)	89 (8'b01011001)	8'b11010001	8'b01010111
117 (8'b01110101)	-55 (8'b11001001)	80.25 (8'b01010000)	-119.7 (8'b10001001)	8'b01001111	8'b10000111
-88 (8'b10101000)	-63 (8'b11000001)	-77.5 (8'b10110011)	-23.25 (8'b11101001)	8'b10110010	8'b11101000

Table 3 the experiment table for test affine transformation algorithm

Then just need to input the values above one by one and note down the result into the table, as below:

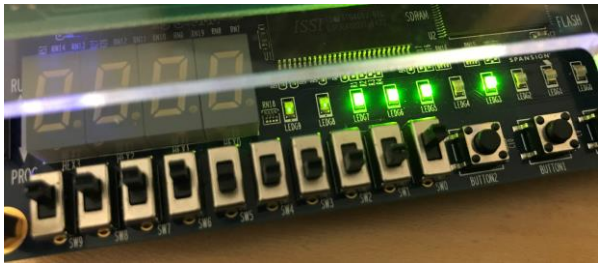

Figure 17 the experiment process

The experiment worked smoothly. However, it is clearly shown in Table 3 that the actual results are slightly different from the theoretical results. That is because the fraction part is discarded entirely in the multiplication, thus the results sometimes would smaller than its theoretical value.

Although there are slight difference, the results can be defined as approximately correct and the performance of processor is qualified. Eventually the whole development work is done.

6. Conclusion

To summarise, the objectives of this assignment have all been achieved and every required functions have been implemented. Moreover, the modules and algorithms in this design work properly. In other words, a processor with a small picoMIPS architecture has been designed and tested while the affine transformation algorithm is run successfully on it, which is very excited.

The synthesis report is shown below.

Top-level Entity Name	picoMIPS
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	113 / 114,480 (< 1 %)
Total combinational functions	108 / 114,480 (< 1 %)
Dedicated logic registers	37 / 114,480 (< 1 %)
Total registers	37
Total pins	19 / 529 (4 %)
Total virtual pins	0
Total memory bits	0 / 3,981,312 (0 %)
Embedded Multiplier 9-bit elements	1 / 532 (< 1 %)
Total PLLs	0 / 4 (0 %)

Figure 18 the synthesis report of picoMIPS

According to the cost calulation formula below:

Cost = number of Logic Elements used + max(0,number of embedded multipliers used – 2) +30 x Kbits of RAM used

The cost of this picoMIPS design is 113, which is very small (it takes less than 1% of resource).

However, it still costs too much compared with other plans. For an example, to make a complex ALU can simplify the program memeory to reduce the LEs what store the program. A lot of desgin plans can be disccussed and tried.

Generally, this assignment is finished successfully. A lot of techniques and knowledges are learned when working on it. Also, there are a lot of difficulties in the beginning but it is enjoyable to overcome them.

In additon, here is a trade-off in designing this processor. Due to the main objective of this assignment is to design a as small as possible processor, this processor is designed not only sufficient to do affine transformation, but also enough to do other algorithm. Thus in order to make the cost as small as possible, to make a specific ALU for affine transformation would be necessary. Plus, the embedded RAM blocks in FPGA could be used to save more LEs. There are many ways worth to be used to optimize and improve the design and it will be processed in the fututre.

7. References

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