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K = 4-way set associative Cache size = 32kB = 32 * 1024 = 32768

of blocks, N = 32768 / 64 = 512

Number of bits in address = 32

Number of sets, S = N/k = 512/4 = 128

Block offset = log2(B) = log2(64) = 6Index = log2(S) = log2(128) = 7

Tag = Block address bits - Index - Block offset = 32 - 7 - 6= 19

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Number of blocks available = 8 * 1024 / 64 = 128 Each block will hold 64 / 8 = 8 elements
For the Code Fragment A, there will be cache misses every after every 8th element, since it is a direct-mapped cache.
The number of cache miss will be:
1024*1024 / 8 = 131072
For the Code Fragment B, the array is being indexed with columns first and rows. Since there are more elements than—there are number of blocks available, and entire column will be brought into the cache, and will not be there the next
time it will be accessed, causing cache misses.
Hence, the number of cache misses = 1024 * 1024 = 1048576

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24-bit virtual address 16-bit physical address 1KB = 1024B page size = 2^10 B

Number of virtual pages =

2^ 24 / 2^10 = 2^14 = 16,384

Number of physical pages: 2^16 / 2^10 = 2^6 = 64

Number of bits in virtual page number = 24 - 10 = 14

Number of bits in physical page number = 16 - 10 = 6

Number of bits in page offset =

Log2(1024) = 10

- b)
 Data write at 000000000011 0011001100
 physical address is 001010 0011001100
 Data write is possible.
- c)
 Instruction fetch at 111111111111 000000000
 Physical address 001100 000000000
 Access violation, because the flag "not executable" is present at that address.