RAJASTHAN TECHNICAL UNIVERSITY, KOTA

Syllabus

II Year-III Semester: B.Tech. Computer Science and Engineering (Data Science)

3CDS3-04: Digital Electronics

Credit-3 **Max. Marks : 100 (IA:30, ETE:70)**

3L+0T+0P **End Term Exam: 3 Hours**

SN	CONTENTS	Hours
1	**Fundamental concepts:** Number systems and codes, Basic logic Gates and Boolean algebra: Sign & magnitude representation, Fixed point representation, complement notation, various codes & arithmetic in different codes & their inter conversion. Features of logic algebra, postulates of Boolean algebra.Theorems of Boolean algebra.	8
2	**Minimization Techniques and Logic Gates**: Principle of Duality - Boolean expression -Minimization of Boolean expressions — Minterm – Maxterm - Sum of Products (SOP) – Product of Sums (POS) – Karnaugh map Minimization – Don't care conditions – Quine - McCluskey method of minimization.	8
3	**Digital Logic Gate Characteristics:** TTL logic gate characteristics. Theory & operation of TTL NAND gate circuitry. Open collector TTL. Three state output logic. TTL subfamilies.MOS& CMOS logic families. Realization of logic gates in RTL, DTL, ECL, C-MOS & MOSFET.	8
4	**Combinational Circuits:** Combinational logic circuit design, adder, subtractor, BCD adder encoder, decoder, BCD to 7-segment decoder, multiplexer demultiplexer.	8
5	**Sequential Circuits:** Latches, Flip-flops - SR, JK, D, T, and Master-Slave Characteristic table and equation,counters and their design, Synchronous counters – Synchronous Up/Down counters – Programmable counters – State table and state transition diagram ,sequential circuits design methodology. Registers –shift registers.	8
	TOTAL	40

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