
STM32
CubeMX

1. Description

1.1. Project

Project Name	Lazuli
Board Name	custom
Generated with:	STM32CubeMX 6.11.0
Date	04/14/2024

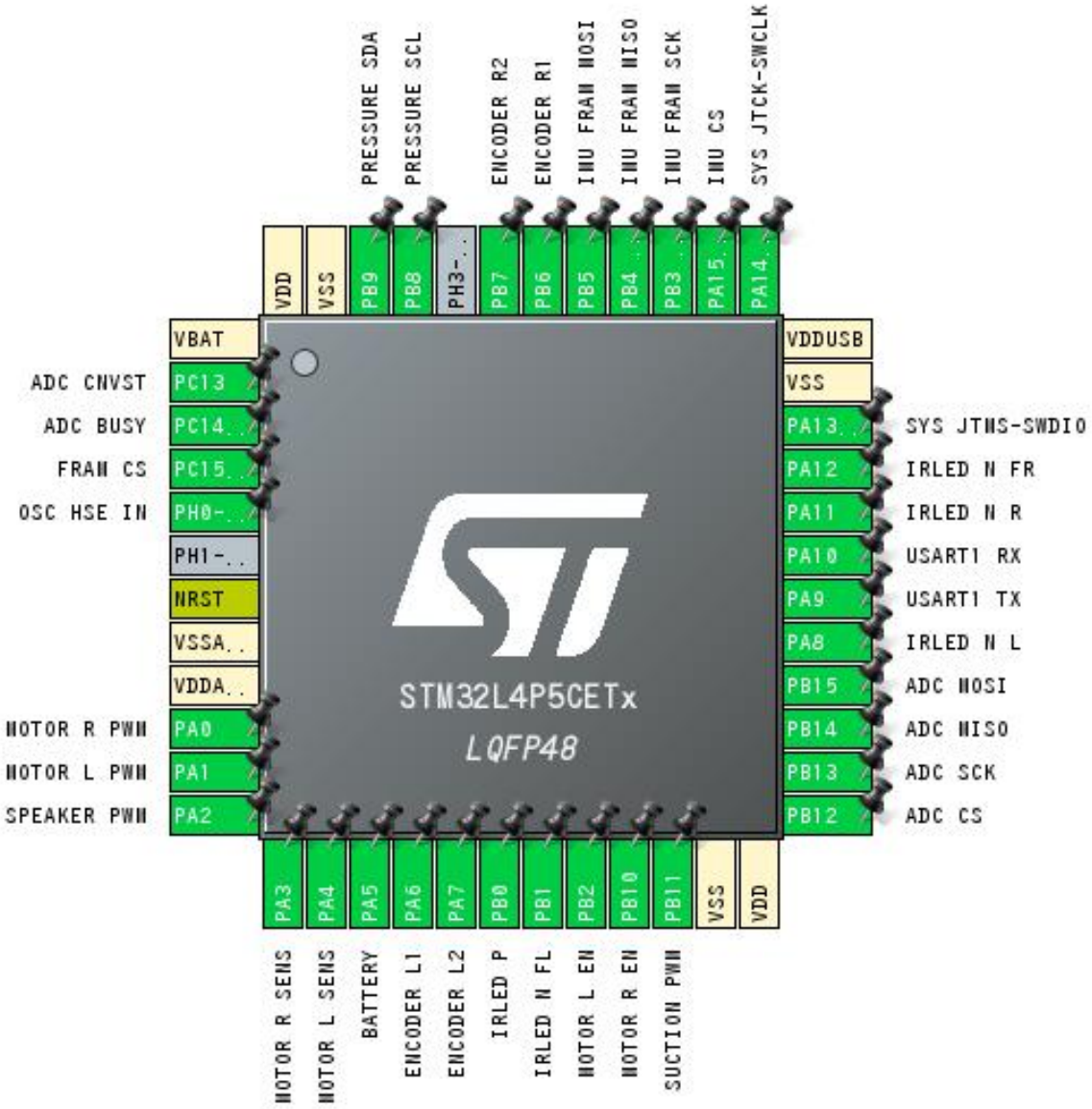
1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4P5/Q5
MCU name	STM32L4P5CETx
MCU Package	LQFP48
MCU Pin number	48

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



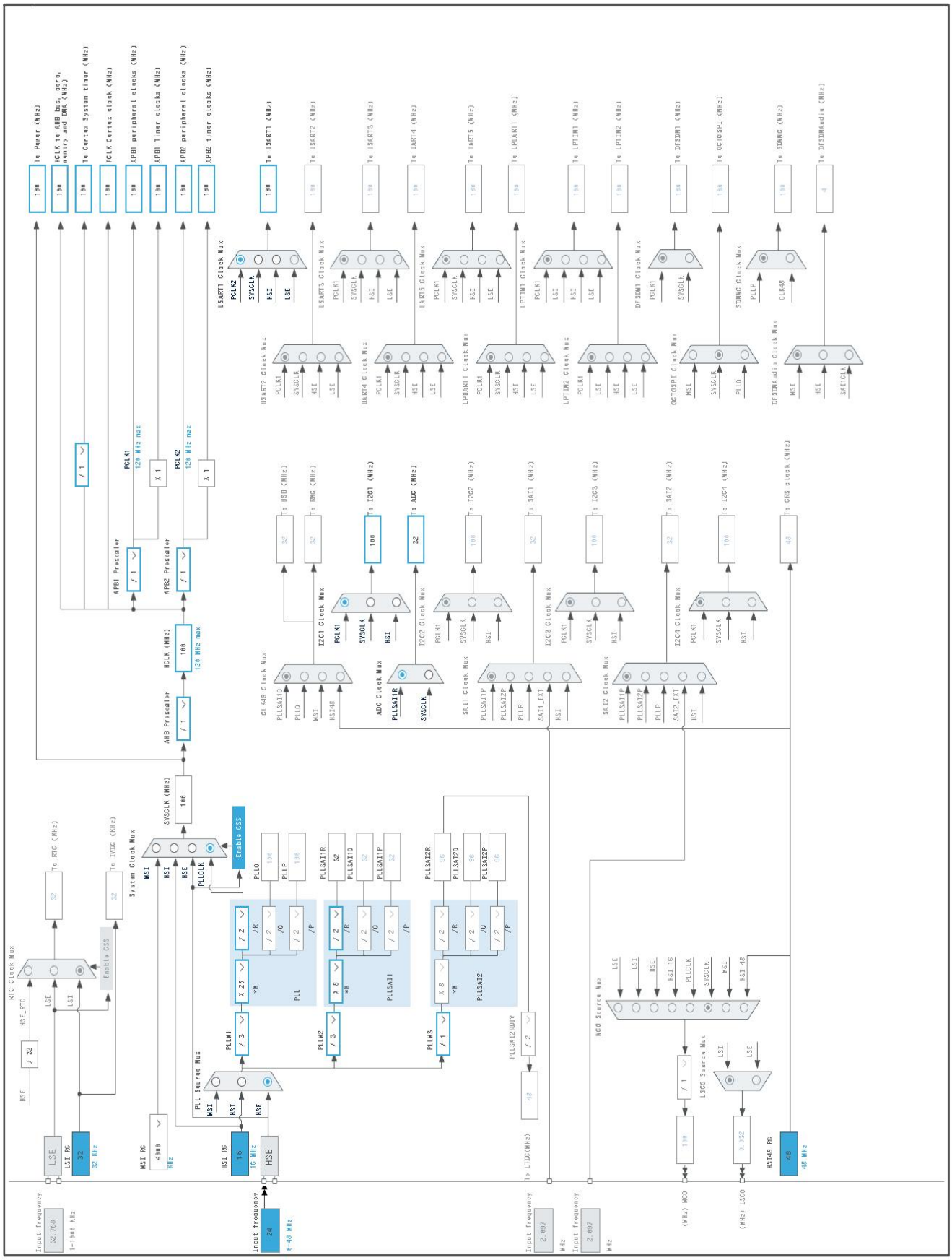
3. Pins Configuration

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13 *	I/O	GPIO_Output	ADC_CNVST
3	PC14-OSC32_IN (PC14) *	I/O	GPIO_Input	ADC_BUSY
4	PC15-OSC32_OUT (PC15) *	I/O	GPIO_Output	FRAM_CS
5	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	OSC_HSE_IN
7	NRST	Reset		
8	VSSA/VREF-	Power		
9	VDDA/VREF+	Power		
10	PA0	I/O	TIM2_CH1	MOTOR_R_PWM
11	PA1	I/O	TIM2_CH2	MOTOR_L_PWM
12	PA2	I/O	TIM15_CH1	SPEAKER_PWM
13	PA3	I/O	ADC1_IN8	MOTOR_R_SENS
14	PA4	I/O	ADC1_IN9	MOTOR_L_SENS
15	PA5	I/O	ADC1_IN10	BATTERY
16	PA6	I/O	TIM3_CH1	ENCODER_L1
17	PA7	I/O	TIM3_CH2	ENCODER_L2
18	PB0 *	I/O	GPIO_Output	IRLED_P
19	PB1 *	I/O	GPIO_Output	IRLED_N_FL
20	PB2 *	I/O	GPIO_Output	MOTOR_L_EN
21	PB10 *	I/O	GPIO_Output	MOTOR_R_EN
22	PB11	I/O	TIM2_CH4	SUCTION_PWM
23	VSS	Power		
24	VDD	Power		
25	PB12	I/O	SPI2_NSS	ADC_CS
26	PB13	I/O	SPI2_SCK	ADC_SCK
27	PB14	I/O	SPI2_MISO	ADC_MISO
28	PB15	I/O	SPI2_MOSI	ADC_MOSI
29	PA8 *	I/O	GPIO_Output	IRLED_N_L
30	PA9	I/O	USART1_TX	
31	PA10	I/O	USART1_RX	
32	PA11 *	I/O	GPIO_Output	IRLED_N_R
33	PA12 *	I/O	GPIO_Output	IRLED_N_FR
34	PA13 (JTMS/SWDIO)	I/O	SYS_JTMS-SWDIO	
35	VSS	Power		
36	VDDUSB	Power		

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
37	PA14 (JTCK/SWCLK)	I/O	SYS_JTCK-SWCLK	
38	PA15 (JTDI) *	I/O	GPIO_Output	IMU_CS
39	PB3 (JTDO/TRACESWO)	I/O	SPI3_SCK	IMU_FRAM_SCK
40	PB4 (NJTRST)	I/O	SPI3_MISO	IMU_FRAM_MISO
41	PB5	I/O	SPI3_MOSI	IMU_FRAM_MOSI
42	PB6	I/O	TIM4_CH1	ENCODER_R1
43	PB7	I/O	TIM4_CH2	ENCODER_R2
45	PB8	I/O	I2C1_SCL	PRESSURE_SCL
46	PB9	I/O	I2C1_SDA	PRESSURE_SDA
47	VSS	Power		
48	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	Lazuli
Project Folder	/home/nonoho/Nextcloud/MicroMouse2/Project/lazuli/STM32CubeMX/Lazuli
Toolchain / IDE	CMake
Firmware Package Name and Version	STM32Cube FW_L4 V1.18.0
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x4000

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_ADC1_Init	ADC1
5	MX_I2C1_Init	I2C1
6	MX_SPI2_Init	SPI2
7	MX_SPI3_Init	SPI3
8	MX_TIM2_Init	TIM2
9	MX_TIM3_Init	TIM3
10	MX_TIM4_Init	TIM4
11	MX_TIM5_Init	TIM5

Rank	Function Name	Peripheral Instance Name
12	MX_USART1_UART_Init	USART1
13	MX_TIM15_Init	TIM15

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4P5/Q5
MCU	STM32L4P5CETx
Datasheet	DS12903_Rev0

1.2. Parameter Selection

Temperature	25
Vdd	3.0

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

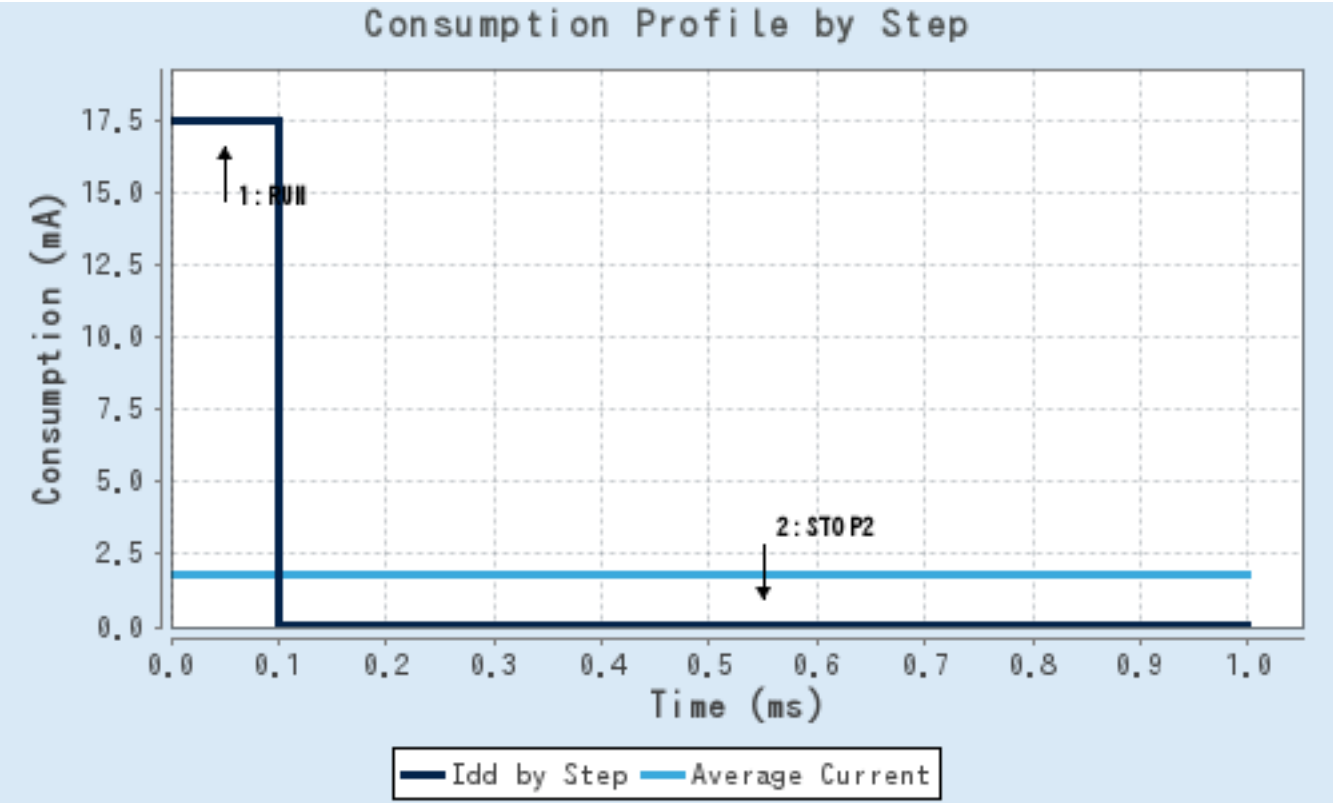
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP2
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-High	NoRange
Fetch Type	FLASH/SingleBank	NA
CPU Frequency	120 MHz	0 Hz
Clock Configuration	HSE BYP PLL ART	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	17.5 mA	2.95 µA
Duration	0.1 ms	0.9 ms
DMIPS	150.0	0.0
Ta Max	102.11	105
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	1.75 mA
Battery Life	2 months, 19 days, 19 hours	Average DMIPS	150.0 DMIPS

1.6. Chart


Consumption Profile by Step
Consumption (mA)
17.5
15.0
12.5
10.0
7.5
5.0
2.5
0.0
1:RUN
2:STOP2
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

2. Peripherals and Middlewares Configuration

2.1. ADC1

IN8: IN8 Single-ended

IN9: IN9 Single-ended

IN10: IN10 Single-ended

2.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**Asynchronous clock mode divided by 8 ***
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 8
Sampling Time	2.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

2.2. I2C1

I2C: I2C

2.2.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	**Fast Mode ***
I2C Speed Frequency (KHz)	400
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x009034B6 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

2.3. RCC

High Speed Clock (HSE): BYPASS Clock Source

2.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	**3 ***
Instruction Cache	Enabled
Prefetch Buffer	**Enabled ***
Data Cache	Enabled
Flash Latency(WS)	4 WS (5 CPU cycle)

RCC Parameters:

HSI Calibration Value	64
MSI Calibration Value	0
MSI Auto Calibration	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1 boost

2.4. SPI2

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

2.4.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**50.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	**Disabled ***
NSS Signal Type	Output Hardware

2.5. SPI3

Mode: Full-Duplex Master

2.5.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**16 ***
Baud Rate	**6.25 MBits/s ***
Clock Polarity (CPOL)	**High ***
Clock Phase (CPHA)	**2 Edge ***

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

2.6. SYS

Debug: Serial Wire

Timebase Source: SysTick

2.7. TIM2

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel4: PWM Generation CH4

2.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

2.8. TIM3

Combined Channels: Encoder Mode

2.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

2.9. TIM4

Combined Channels: Encoder Mode

2.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0

Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

2.10. TIM5

mode: Clock Source

2.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

2.11. TIM15

Channel1: PWM Generation CH1

2.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

2.12. USART1

Mode: Asynchronous

2.12.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)

Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

3. System Configuration

3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA3	ADC1_IN8	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	MOTOR_R_SENS
	PA4	ADC1_IN9	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	MOTOR_L_SENS
	PA5	ADC1_IN10	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	BATTERY
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	**Very High ***	PRESSURE_SCL
	PB9	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	**Very High ***	PRESSURE_SDA
RCC	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	OSC_HSE_IN
SPI2	PB12	SPI2_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ADC_CS
	PB13	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ADC_SCK
	PB14	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ADC_MISO
	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ADC_MOSI
SPI3	PB3 (JTDO/TRACESWO)	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	IMU_FRAM_SCK
	PB4 (NJTRST)	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	IMU_FRAM_MISO
	PB5	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	IMU_FRAM_MOSI
SYS	PA13 (JTMS/SWDIO)	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14 (JTCK/SWCLK)	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM2	PA0	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOTOR_R_PWM
	PA1	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOTOR_L_PWM
	PB11	TIM2_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	SUCTION_PWM

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
TIM3	PA6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	ENCODER_L1
	PA7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	ENCODER_L2
TIM4	PB6	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	ENCODER_R1
	PB7	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	ENCODER_R2
TIM15	PA2	TIM15_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	SPEAKER_PWM
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
GPIO	PC13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ADC_CNVST
	PC14-OSC32_IN (PC14)	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ADC_BUSY
	PC15-OSC32_OUT (PC15)	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	FRAM_CS
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IRLED_P
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IRLED_N_FL
	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR_L_EN
	PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR_R_EN
	PA8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IRLED_N_L
	PA11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IRLED_N_R
	PA12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IRLED_N_FR
	PA15 (JTDI)	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IMU_CS

3.2. DMA configuration

DMA request	Stream	Direction	Priority
USART1_RX	DMA1_Channel1	Peripheral To Memory	Low
USART1_TX	DMA1_Channel2	Memory To Peripheral	Low
SPI3_TX	DMA1_Channel3	Memory To Peripheral	**High ***
SPI3_RX	DMA1_Channel4	Peripheral To Memory	**High ***
SPI2_RX	DMA1_Channel5	Peripheral To Memory	**High ***
SPI2_TX	DMA1_Channel6	Memory To Peripheral	**High ***
I2C1_RX	DMA1_Channel7	Peripheral To Memory	Low
I2C1_TX	DMA2_Channel1	Memory To Peripheral	Low
ADC1	DMA2_Channel2	Peripheral To Memory	**Medium ***

USART1_RX: DMA1_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART1_TX: DMA1_Channel2 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SPI3_TX: DMA1_Channel3 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SPI3_RX: DMA1_Channel4 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SPI2_RX: DMA1_Channel5 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SPI2_TX: DMA1_Channel6 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

I2C1_RX: DMA1_Channel7 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

I2C1_TX: DMA2_Channel1 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

ADC1: DMA2_Channel2 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

3.3. NVIC configuration

3.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
Flash global interrupt	true	0	0
DMA1 channel1 global interrupt	true	0	0
DMA1 channel2 global interrupt	true	0	0
DMA1 channel3 global interrupt	true	0	0
DMA1 channel4 global interrupt	true	0	0
DMA1 channel5 global interrupt	true	0	0
DMA1 channel6 global interrupt	true	0	0
DMA1 channel7 global interrupt	true	0	0
ADC1 and ADC2 global interrupt	true	0	0
I2C1 event interrupt	true	0	0
I2C1 error interrupt	true	0	0
SPI2 global interrupt	true	0	0
USART1 global interrupt	true	0	0
TIM5 global interrupt	true	0	0
SPI3 global interrupt	true	0	0
DMA2 channel1 global interrupt	true	0	0
DMA2 channel2 global interrupt	true	0	0
FPU global interrupt	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused		
RCC global interrupt	unused		
TIM1 break interrupt and TIM15 global interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		

3.3.2. NVIC Code generation

Enabled interrupt Table	Select for init	Generate IRQ	Call HAL handler

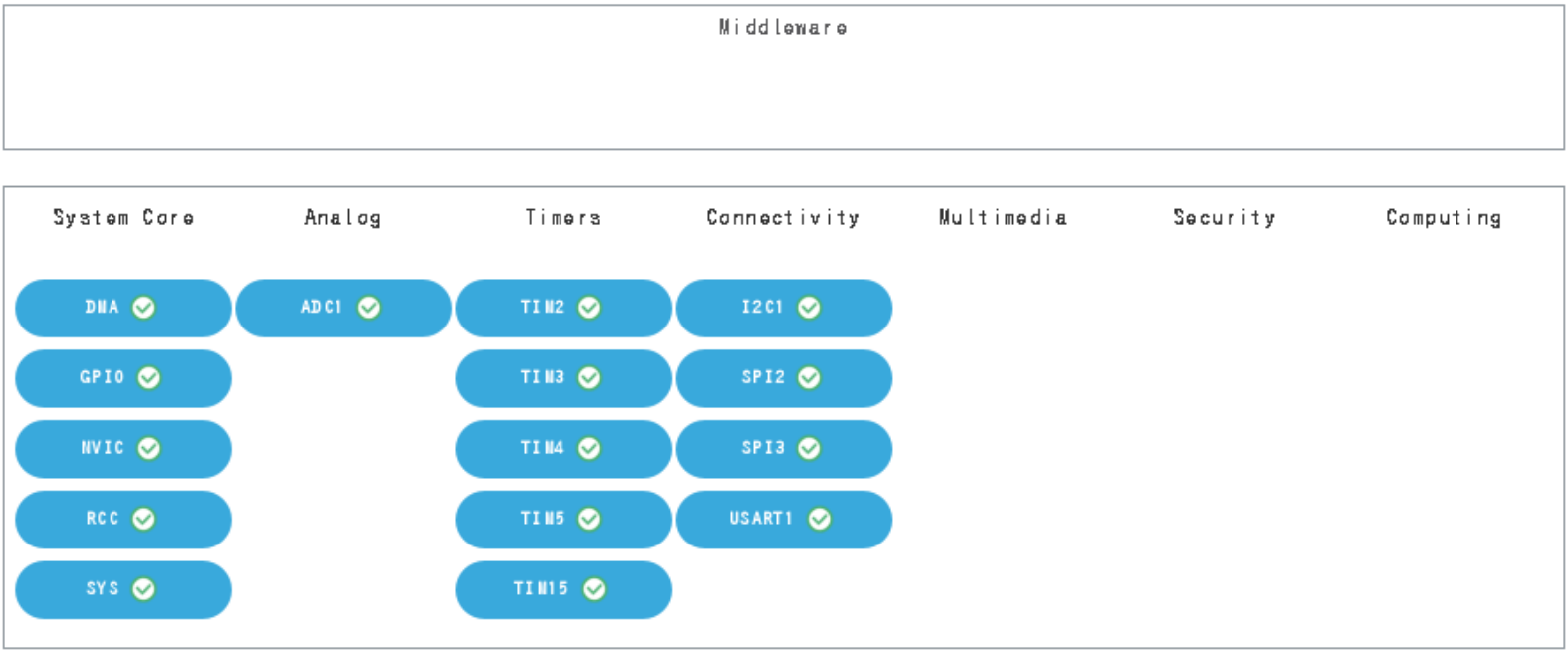
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
Flash global interrupt	false	true	true
DMA1 channel1 global interrupt	false	true	true
DMA1 channel2 global interrupt	false	true	true
DMA1 channel3 global interrupt	false	true	true
DMA1 channel4 global interrupt	false	true	true
DMA1 channel5 global interrupt	false	true	true
DMA1 channel6 global interrupt	false	true	true
DMA1 channel7 global interrupt	false	true	true
ADC1 and ADC2 global interrupt	false	true	true
I2C1 event interrupt	false	true	true
I2C1 error interrupt	false	true	true
SPI2 global interrupt	false	true	true
USART1 global interrupt	false	true	true
TIM5 global interrupt	false	true	true
SPI3 global interrupt	false	true	true
DMA2 channel1 global interrupt	false	true	true
DMA2 channel2 global interrupt	false	true	true
FPU global interrupt	false	true	false

*** User modified value**

4. System Views

4.1. Category view

4.1.1. Current



5. Docs & Resources

Type	Link