### Group 12

# HARTLEY OSCILLATOR USING BJT CONFIGURATION

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### INTRODUCTION

Topology: BJT-based Hartley oscillator
Tank Circuit: Tapped (or series) inductors +
capacitor determine oscillation frequency
Output: Stable, continuous sine wave at the
desired frequency

Biasing: Transistor bias set for proper amplification and linear operation

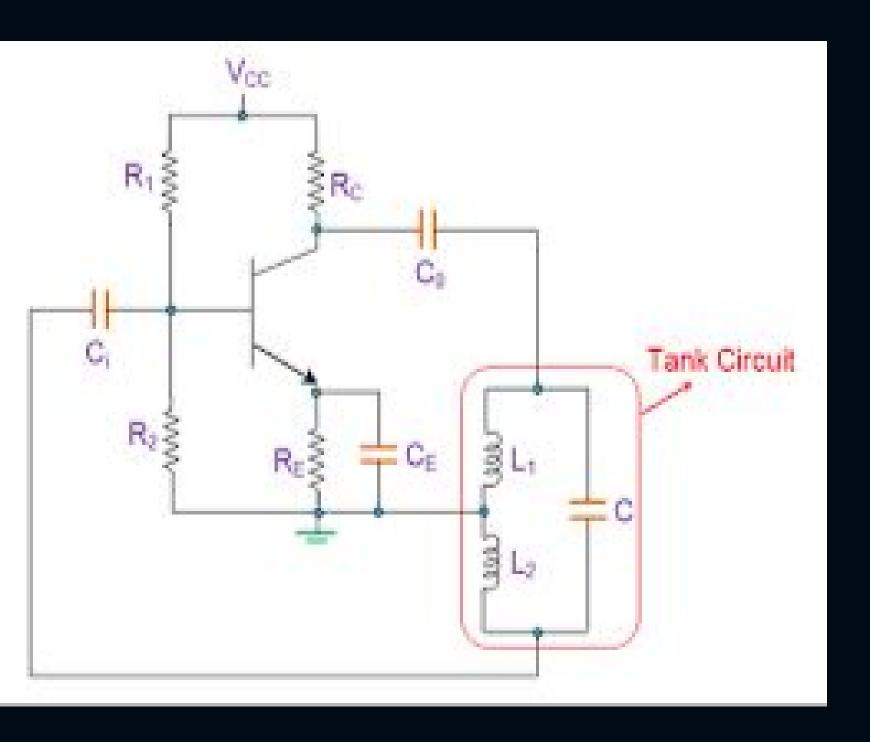
Feedback: Inductive feedback ensures sustained oscillation

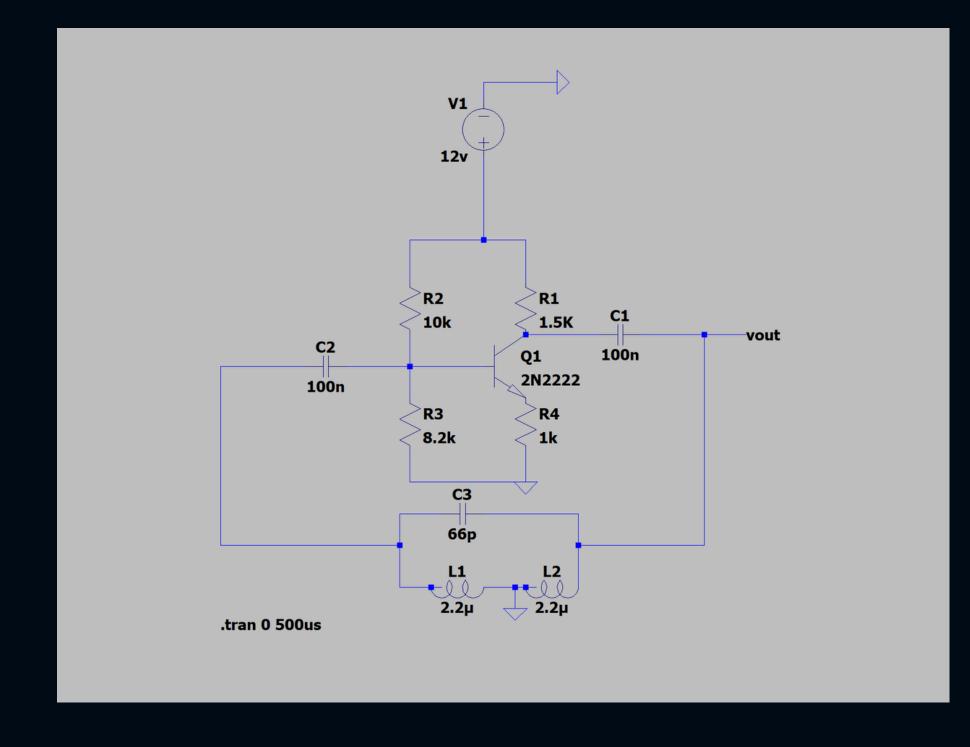
Applications: RF signal sources, audio generators, and timing circuits

### HARTLEY OSCILLATOR

The Hartley Oscillator is a popular type of LC oscillator that generates sinusoidal waveforms. It uses a combination of inductors (L) and a capacitor (C) toform a resonant (tank) circuit. A BJT (Bipolar Junction Transistor) is used to provide amplification and positive feedback, necessary for sustained oscillations.

- PRODUCES PURE SINUSOIDAL WAVEFORMS.
- FREQUENCY IS DETERMINED BY INDUCTORS AND CAPACITOR (LC TANK CIRCUIT).
- POSITIVE FEEDBACK IS PROVIDED USING A TAPPED COIL OR TWO INDUCTORS.
- USES A BJT AS THE ACTIVE AMPLIFYING DEVICE.
- SIMPLE, COMPACT, AND EASY TO DESIGN CIRCUIT.
- FREQUENCY CAN BE EASILY ADJUSTED BY CHANGING INDUCTANCE OR CAPACITANCE.
- SUITABLE FOR HIGH-FREQUENCY (RF) SIGNAL GENERATION.
- STABLE OUTPUT WITH PROPER BIASING.
- Frequency of Oscillation F =  $I/2\pi\sqrt{((L_1+L_2+2M)+C)}$

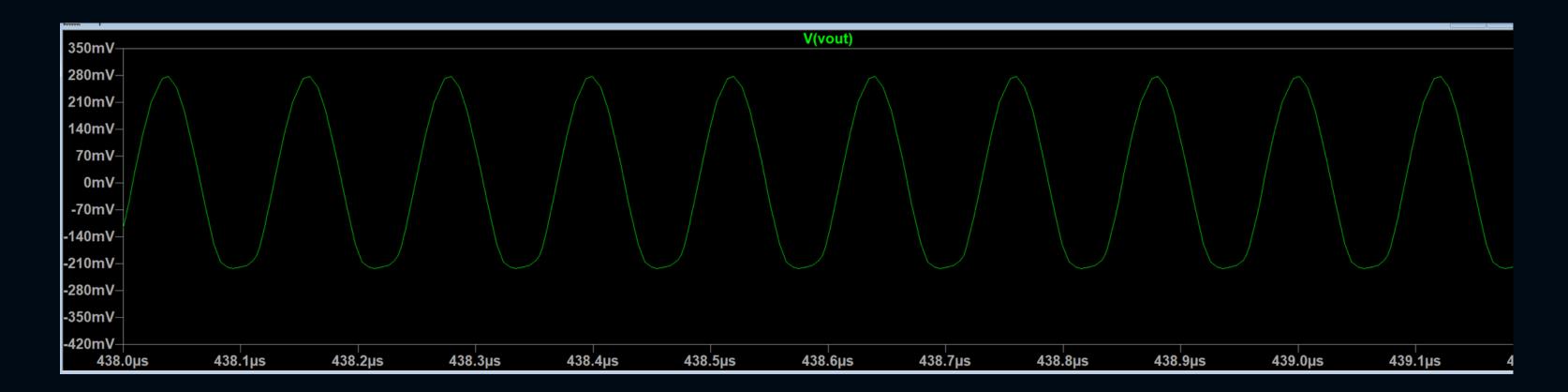


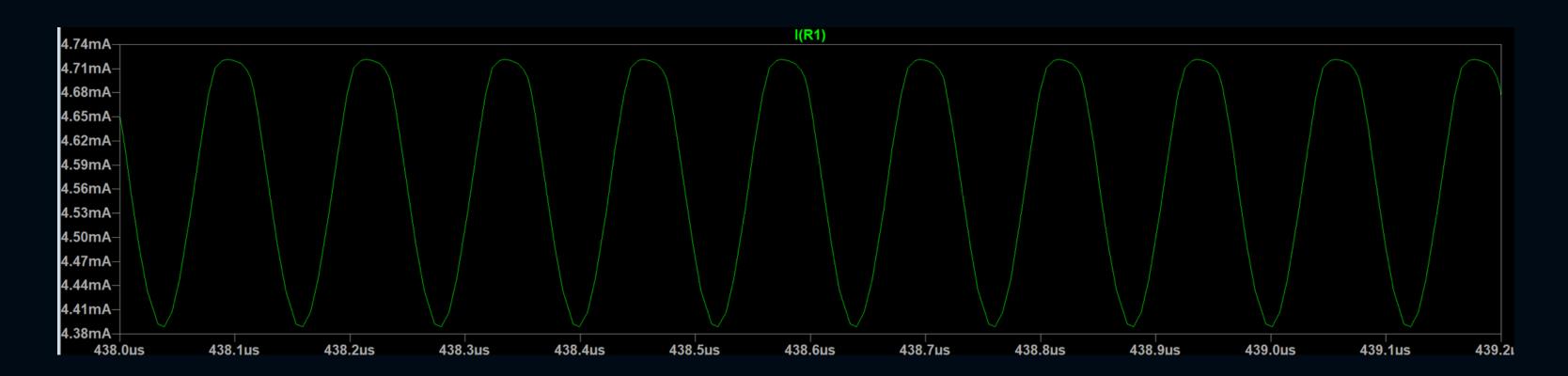


CIRCUIT DIAGRAM

LTSPICE CIRCUIT

### **OUTPUT WAVEFORM**





5

• Tank inductance

$$L_{
m eq} = L_1 + L_2 = 2.2\,
m \mu H + 2.2\,
m \mu H = 4.4\,
m \mu H$$

• Resonant capacitor

$$C=66\,\mathrm{pF}$$

• Resonant frequency

$$f_0 = rac{1}{2\pi \sqrt{L_{
m eq}\,C}} = rac{1}{2\pi \sqrt{4.4 imes 10^{-6} imes 66 imes 10^{-12}}} pprox 9.3 \, {
m MHz}$$

Base voltage	$V_B = 12 \cdot rac{8.2}{10+8.2}$	5.406 V
Emitter voltage	$V_E=V_B-0.7$	4.707 V
Emitter/collector current	$I_C pprox V_E/R_4$	4.707 mA
Ideal R₁ for mid-rail (6 V)	$R_1=rac{6}{I_C}$	1.275 kΩ
Using $R_1$ =1.5 $k\Omega \rightarrow V_C$	$12-I_C\cdot 1.5 \mathrm{k}\Omega$	4.94 V
Resulting V_CE	$V_C-V_E$	0.23 V
Transconductance	$g_m=I_C/V_T$	0.188 S

$$-g_m R_1$$

### 1. Feedback path (the tapped inductor)

Write the divider as a complex ratio:

$$eta(j\omega) = rac{V_{
m fb}}{V_{
m out}} = -rac{Z_{L_2}}{Z_{L_1} + Z_{L_2}} = -rac{j\omega L_2}{j\omega (L_1 + L_2)} = -rac{L_2}{L_1 + L_2} \quad ext{(real, negative)}$$

- The leading "-" is a 180° flip from the dot-convention.
- The magnitude is  $\frac{L_2}{L_1+L_2}=0.5$ .
- Phase:

$$\angle \beta = \angle (-1) + \angle \left(\frac{L_2}{L_1 + L_2}\right) = 180^{\circ} + 0^{\circ} = 180^{\circ}.$$

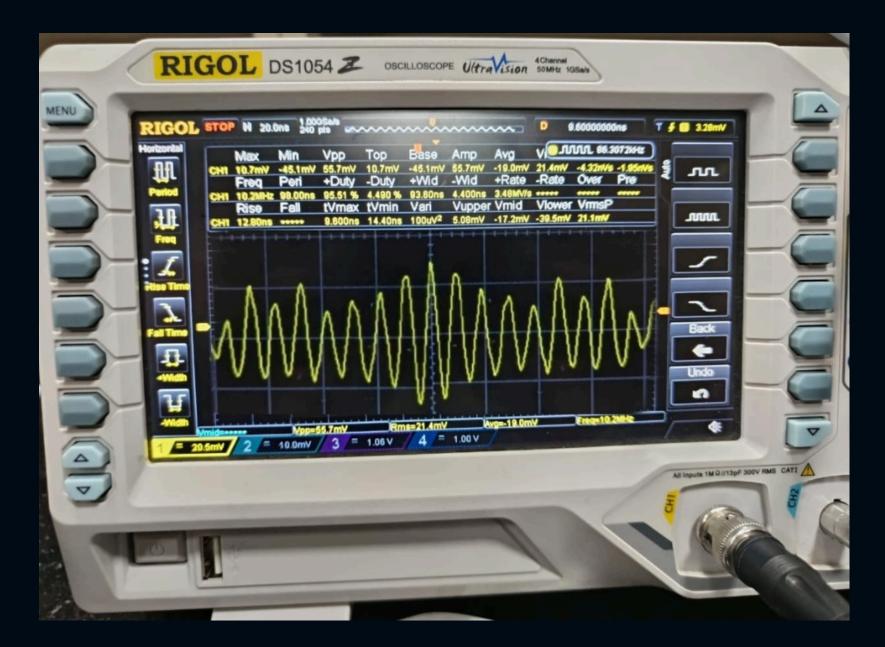
### 2. Amplifier path (common-emitter with R₄ un-bypassed)

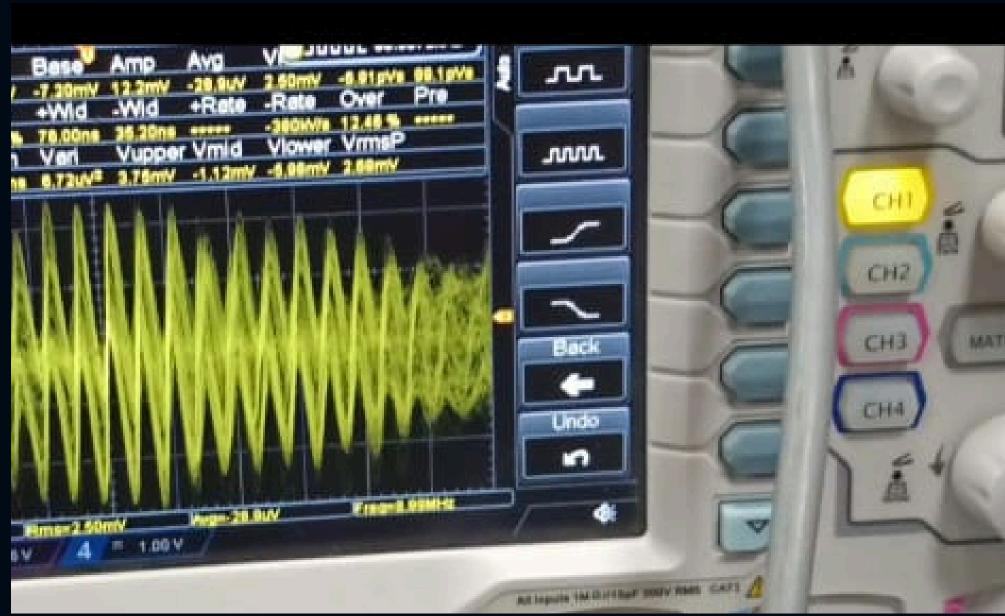
At mid-band (well below any transistor internal poles), the small-signal gain is purely real (and negative):

$$A_v = -rac{R_1}{R_4 + r_e} \implies \angle A_v = 180^\circ.$$

# Circuit

### **OBSERVATIONS**





- Resonant frequency close to design: the tank of two 2.2 µH coils and ~66 pF yields ≈9–10 MHz in practice (shifts ±1 MHz if parasitics aren't minimized).
- Feedback ratio fixed at ½: because L₁=L₂, β=L₂/(L₁+L₂)=0.5, so the amplifier must deliver ≥2× gain for Barkhausen's magnitude criterion.
- Clean sine on compact layout: on a PCB or tightly-wired perf-board you'll see a pure sine with low distortion; on a solderless breadboard stray C/L kills Q and causes drop-outs or harmonics.

9

# Challenges Faced

- Higher Frequencies are not supported on breadboard.(Stray Capacitance).
- Using pF caps resulted in very parasitic effect and stray capacitance.
- High Values of R have parasitic effect at high frequencies.
- Mainting the amplitude in DSO, as croc cables attenuate them.
- Dealing with all the losses involved in the process.

## Future Improvements

• We can create a PCB which might beetter when it comes to handle higher frequencies.

# THANK YOU!

FOR YOUR ATTENTION