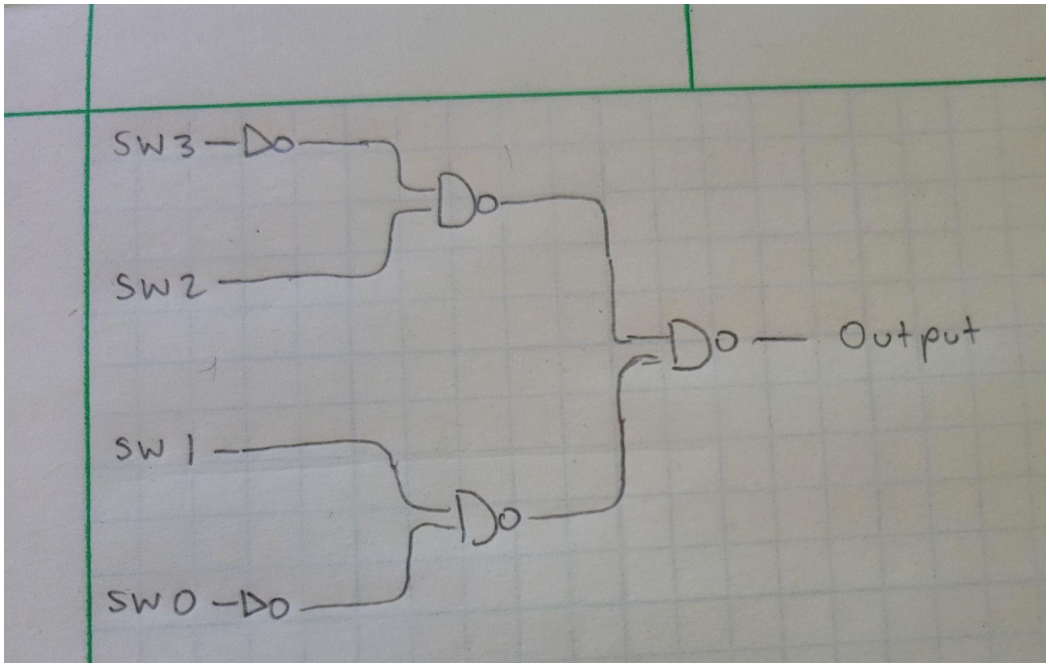
Lab 1: Introduction to Verilog and Digital Components

a. Name and Class Number: Juan Trejo (1939336) and EE 271 A.
b. The mux4_1.sv circuit is system that consists of two mux2_1's. The output of the system is true when either of the mux2_1's , m0 or m1 complete their conditional statements. This means that if either m0 or m1 has their respective "sel" input as 0 and equal to their i0 or "sel" is 1 and equal to their i1, the output of the system is TRUE.
c. The value of the signal that makes the LEDR's light up is FALSE (GND).
d. The position of the slider switches that cause the output TRUE is flicked down going away the LEDR.
e. The position of the pushbuttons that causes the output to be TRUE is when pressed down.
f. My output would be true for the number 6 as that is the last number of my student ID.



g.