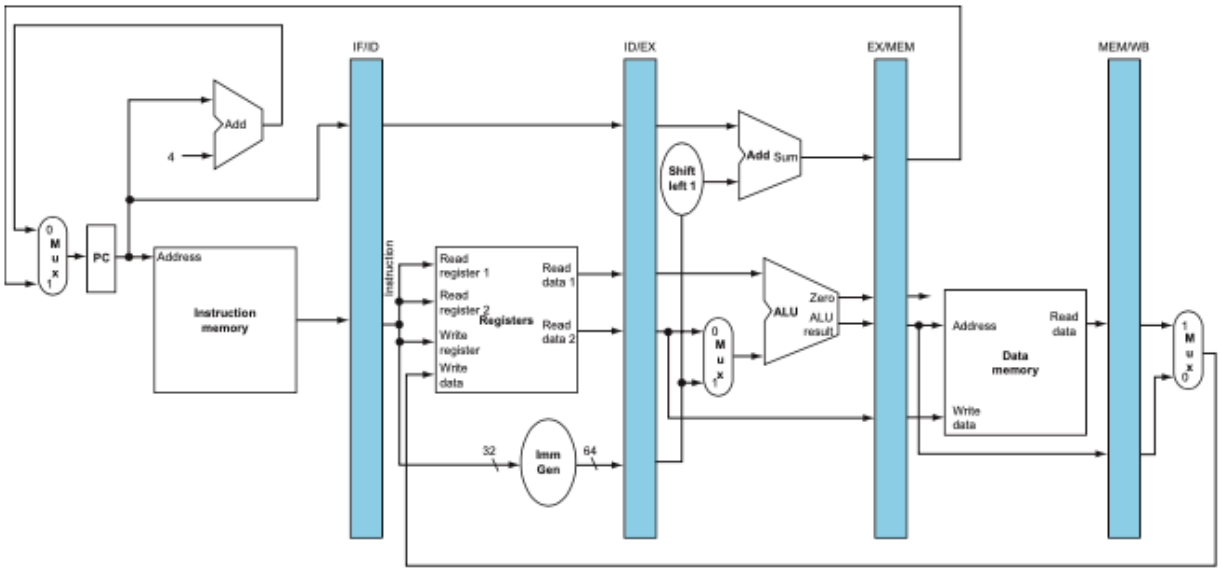
CSE/EE 469 Wi 2023: Lab 2
Due: Mar 3rd, 2021

Goal of This Lab

Add 5-stage pipelining to your RISC-V cpu from lab 1. All of the requirements of the CPU and everything else are the same as lab 1, only difference is now you need to add pipelining.

Here is a simplified diagram of the pipelined RISC-V architecture from the textbook:



The 5 pipeline stages are:

- Fetch: read the instruction from code memory
- Decode/Register access: decode the instruction and read the register file
- Execute: execute the instruction
- Memory write: read or write from memory
- Write back: Write the results back to the register file

Testing

SIMULATE, **SIMULATE** and **SIMULATE** your design.
It is highly recommended that you test every single verilog module on its own before testing your entire design. Use a simulation software (like ModelSim, IVerilator, Vivado, etc.) to test your design.

A recommended approach is to implement one pipeline stage at a time and test and make sure your code works before moving onto the next pipeline stage.

Submissions and Demos

Sign up for demos (TBD) and submit code on Canvas.
During the demo:

- you will walk the TA through your cpu code,
- show that the pipelines are working in your simulation,
- show that it can run printf.

TA check in: 27 Feb - 1 Mar
Submission deadline: 3rd Mar
Demos: Mar 6- 10th