CAD 1: MOSFET Characteristics

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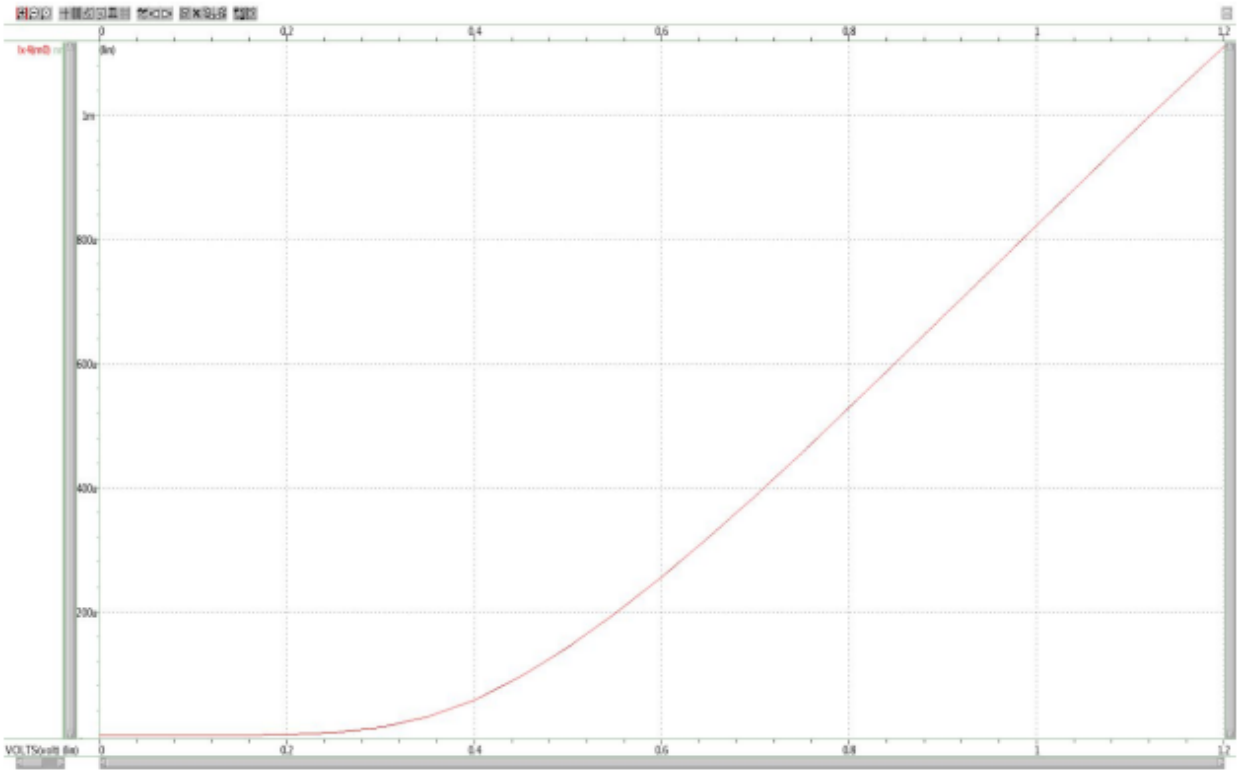
1: IV Characteristics

Part A

In part A, we are tasked with determining the IV characteristics of an NMOS transistor with a width (W) of 1µm and a length (L) of 50nm. In Cadence, I constructed the required circuit and defined two voltage sources: one set to 1.2 volts for Vdd and the other set to 1.2 volts for Vg. To generate a plot depicting Ids as a function of Vgs, I established a DC analysis with Vgs ranging from 0 volts to 1.2 volts. The resulting Ids versus Vgs plot is presented below. This plot aligns with expectations, as when Vgs exceeds approximately 0.2 volts, the NMOS transistor turns on, exhibiting the characteristics described.

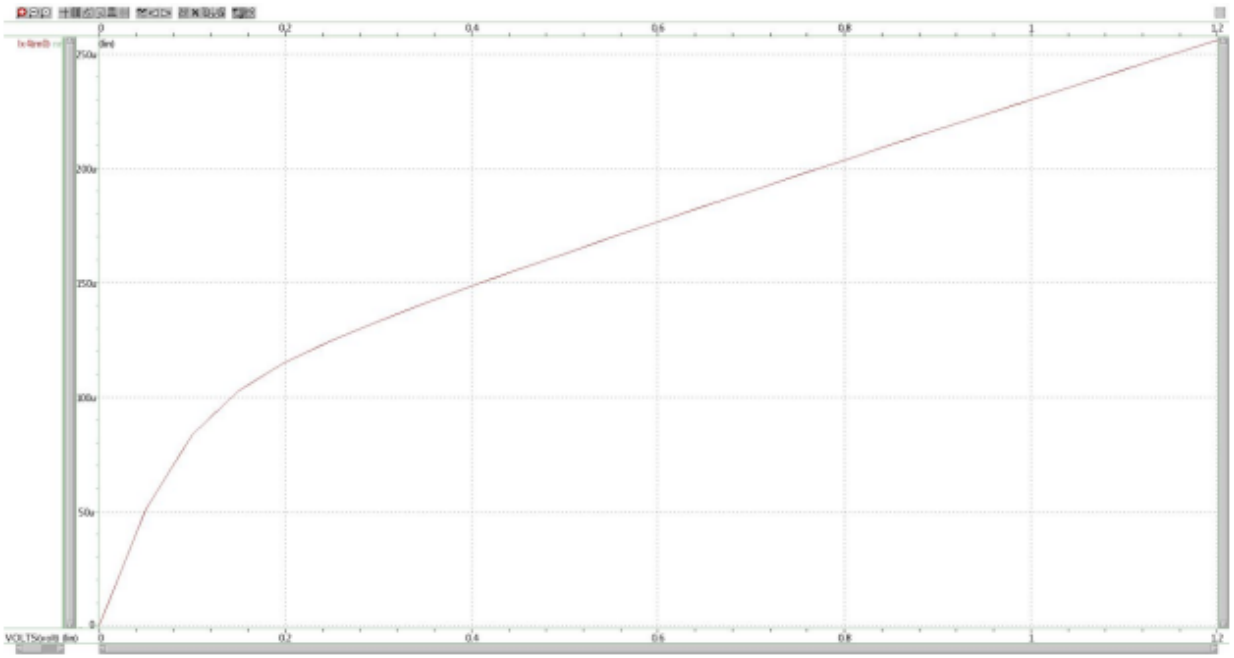


Part B

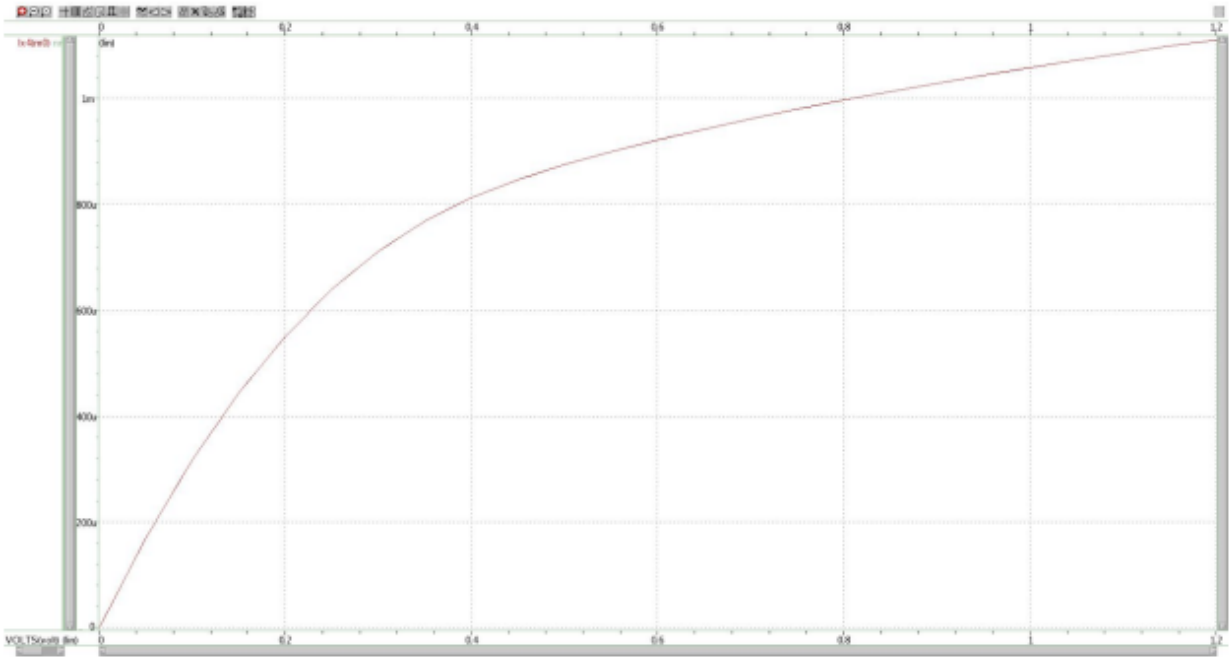
In part B, we are tasked with obtaining the IV characteristics of an NMOS transistor with two different Vgate values: one set at 0.6 volts and the other at 1.2 volts. To generate plots depicting Ids as a function of Vds in order to understand the behavior of the NMOS transistor in various

operational regions, we need to conduct a DC analysis that varies the voltage across the NMOS device.

To accomplish this, I configured my control file with a voltage source set at 1.2 volts for Vdd. I connected Vg to the ground and supplied it with the required voltages of 0.6 volts and 1.2 volts separately. The waveforms presented below represent the results for Vg = 0.6 volts.



In this scenario, initially, the NMOS operates in the cutoff region, then transitions into the triode region, and ultimately settles into the saturation region. When it reaches the saturation region, the Vds stabilizes at around 0.4 volts. This behavior is in line with the fact that Vgs is set to 0.6 volts, and the threshold voltage (Vth) is approximately 0.2 volts. The waveforms presented below represent the results for Vg = 1.2 volts.

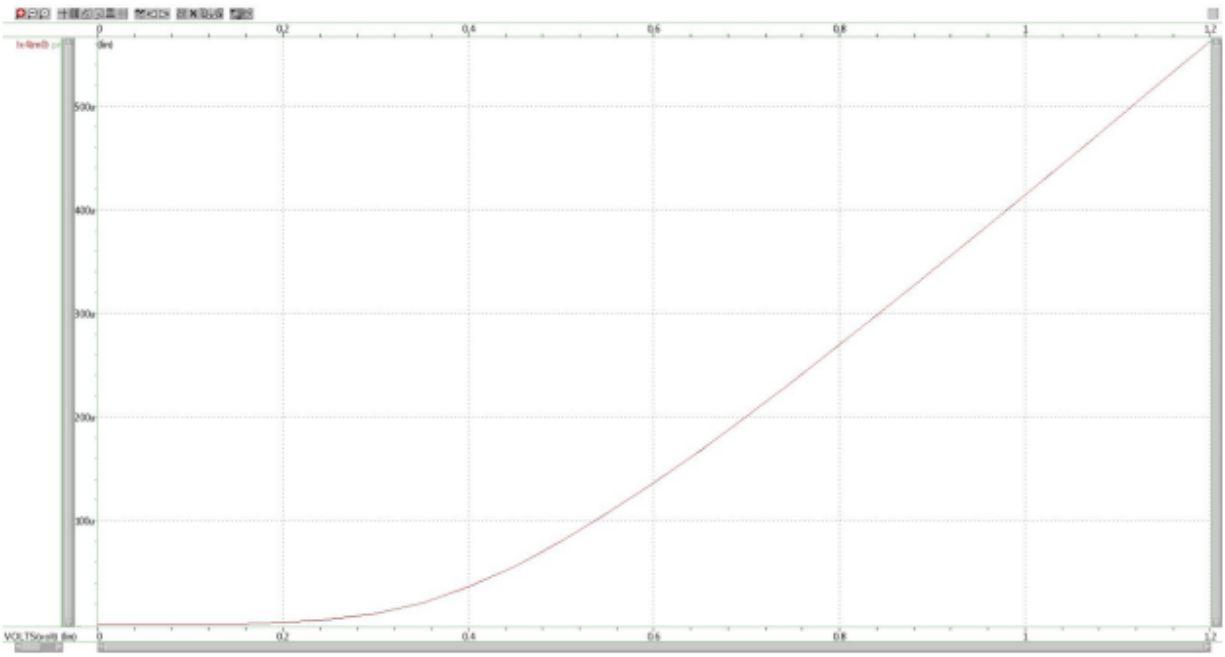


In this scenario, initially, the NMOS operates in the cutoff region, then progresses into the triode region, and eventually settles into the saturation region. As it enters the saturation region, the Vds stabilizes at approximately 1 volt. This behavior aligns with the condition where Vgs is set at 1.2 volts, and the threshold voltage (Vth) is approximately 0.2 volts.

Part C

In part C, we are instructed to replicate the same process for the PMOS transistor as we did for the NMOS. The PMOS transistor chosen has characteristics with a width (W) of 1µm and a length (L) of 50nm. I constructed the circuits according to the provided specifications.

Since our goal is to obtain the IV characteristics, specifically Isd versus Vsg, I configured my control file. I set the voltage source Vdd to 1.2 volts and established a DC analysis in which I connected Vdd to Vg. This allowed the voltage between them to vary from 0 volts to 1.2 volts. The resulting waveform is entirely accurate because as we increase Vsg, the PMOS transistor first turns on and then transitions into the triode region before reaching saturation.

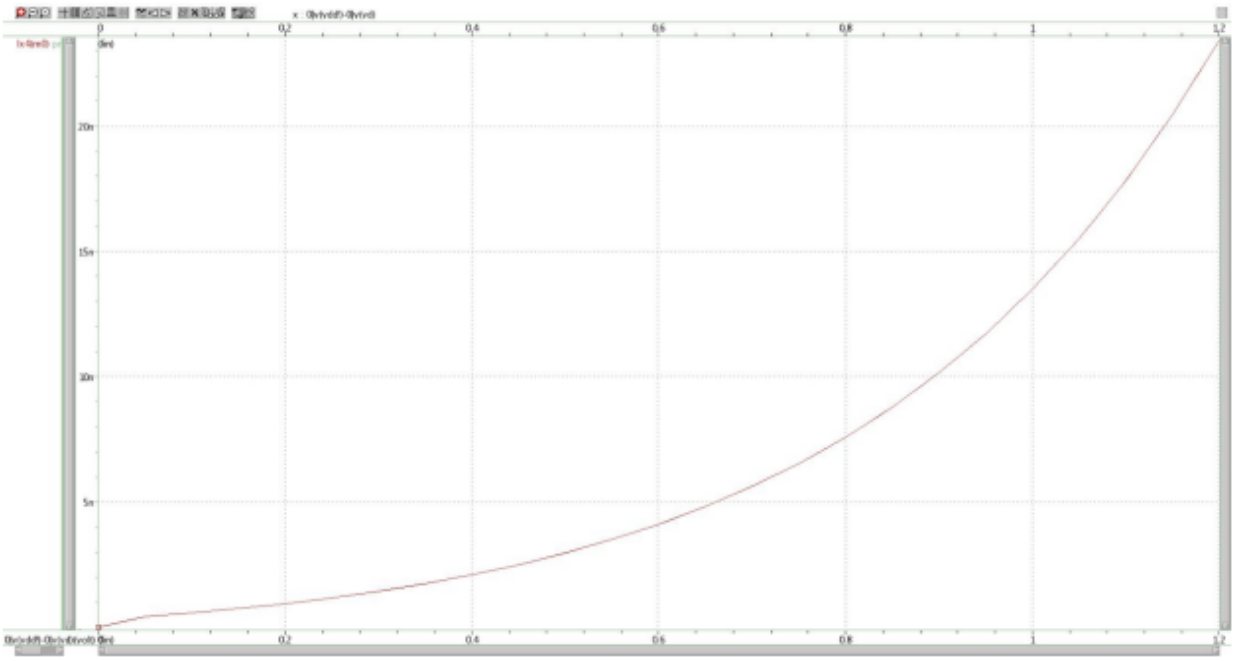


Part D

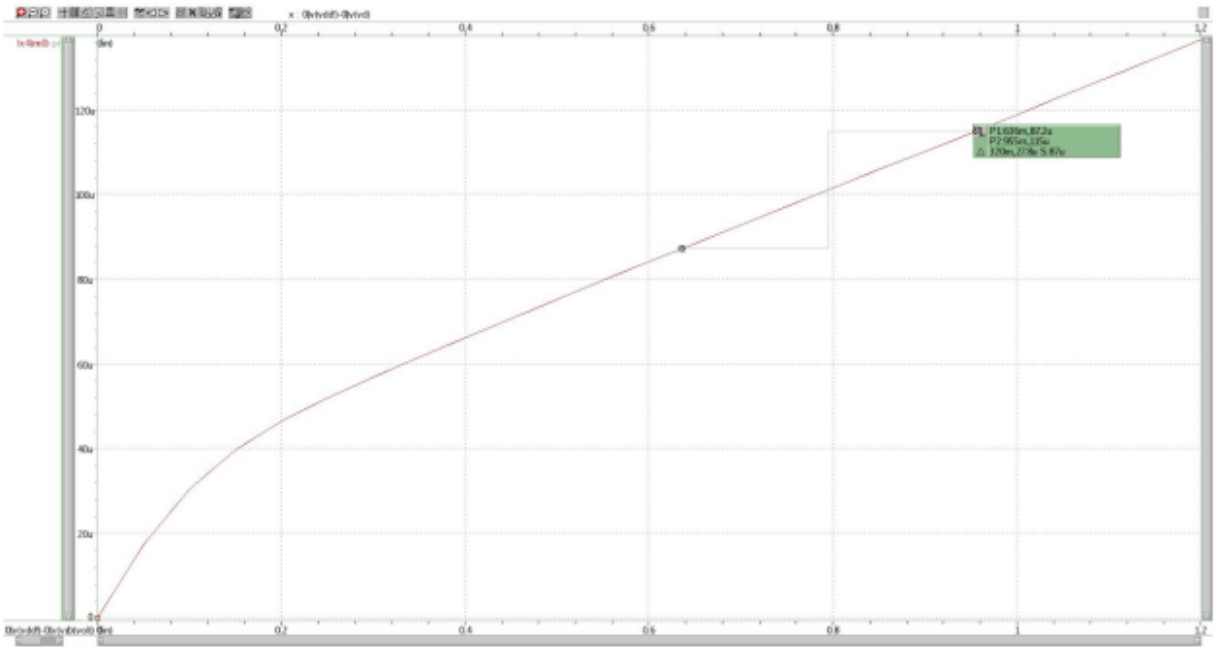
In part D, we followed a similar procedure with the PMOS transistor as we did in part B. To understand the behavior of the PMOS device across different operational regions, we aimed to capture the waveform of Isd versus Vsd. To achieve this, we established two sets of Vg values: one set at 1.2 volts and the other at 0.6 volts.

Within my control file, I configured three voltage sources: one for Vg (gate voltage), one for Vdd set to 1.2 volts, and a voltage supply connecting the PMOS transistor to the ground to maintain a stable Vgs and avoid Vds changes. Then, I executed a DC analysis that varied the voltage supply from 1.2 volts to 0 volts, thereby allowing Vsd to change from 0 volts to 1.2 volts.

As we had set up a DC analysis concerning Vsupply, but our interest lay in the waveform of Vsd, I adjusted the waveform axis using a built-in function to display Vsd on the x-axis rather than Vsupply. The results are presented below for Vg = 1.2 volts.



As indicated by the data, the PMOS transistor remains consistently in the cutoff region for Vg = 0.6 volts.



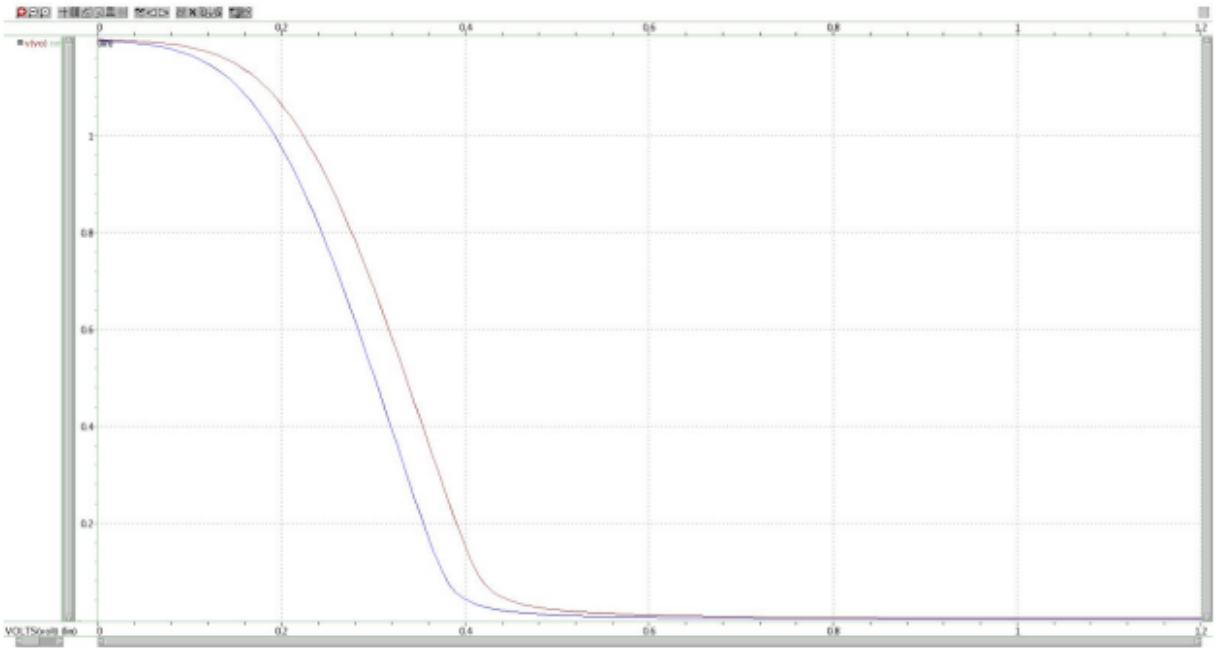
As depicted in the waveform, the PMOS transistor begins in the cutoff region, transitions to the triode region, and eventually reaches the saturation region. Upon entering the saturation region, the Vds stabilizes at approximately 0.8 volts.

2: FET's with Resistances

Part A

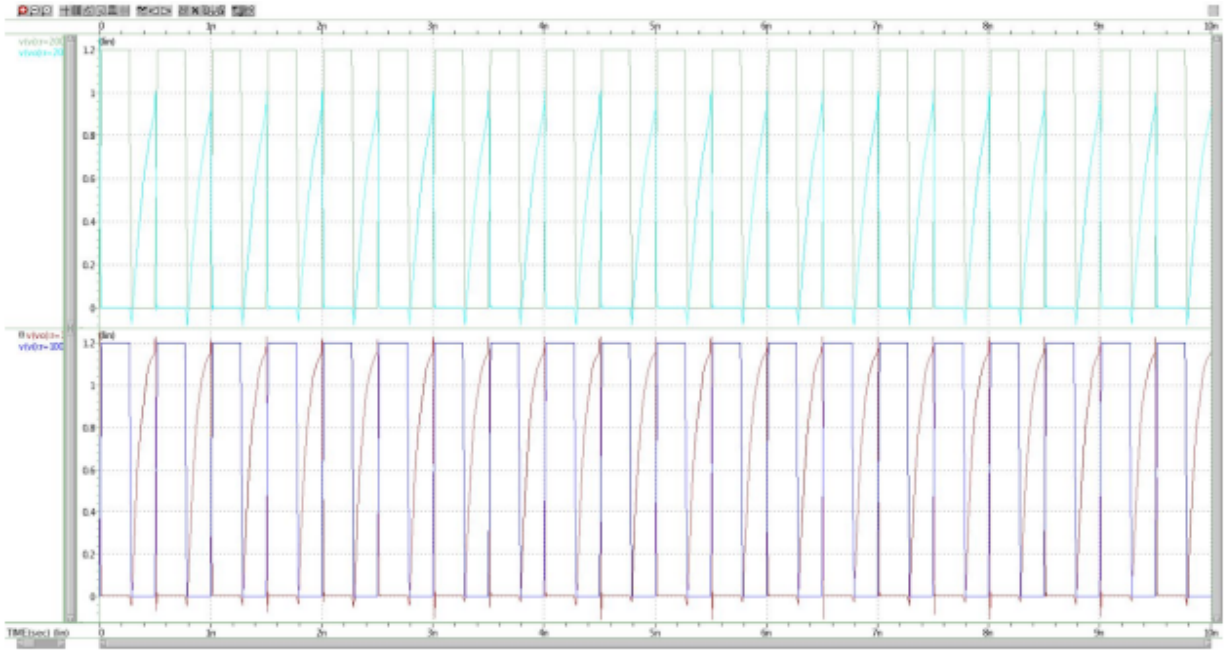
In part A, our task was to determine the drain voltage of the NMOS transistor with varying resistors while altering the gate voltage from 0 volts to 1.2 volts. In my Cadence setup, I constructed the necessary circuit according to the provided specifications, omitting the connection of resistors. Instead, I left the resistors and the NMOS transistor unconnected at the schematic level.

However, in my control file, I introduced the resistors into the DC analysis, allowing them to range from 100k to 200k in a single step, thus obtaining two different resistor settings simultaneously. Additionally, I included Vgate in the DC analysis to vary it from 0 volts to 1.2 volts, and I established a voltage source at Vdd set to 1.2 volts. The obtained results are presented below.



Part B

The fundamental configuration remains identical to that in part B. However, we modified Vgate into a square wave voltage source with the following parameters: T = 500 picoseconds, Trise = 20 picoseconds, and Tfall = 20 picoseconds. The resulting outcomes are depicted below.

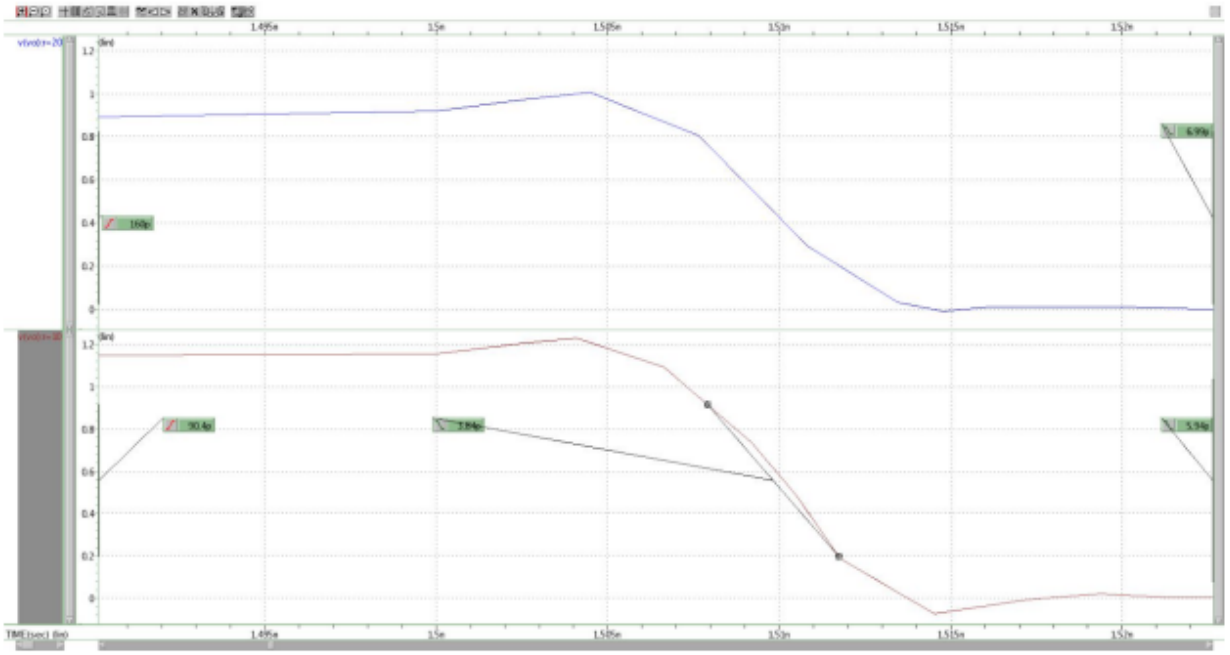


Part C

In part C, our objective is to determine the rise time and fall time of Vo with a resistor of 100kΩ using both the '.MEAS' method and the Measurement Tool. In the '.MEAS' approach, I simply employed the '.MEAS' command for rise time and fall time.

Within the '.mt0' file, which houses my measurement results, I obtained a rise_time of 8.931e-11 seconds and a fall_time of 3.973e-11 seconds using this method.

For the Measurement Tool, I selected the fall time and rise time functions and expanded the signal segment that I was interested in, encompassing the fall time and rise time portions. The results from the Measurement Tool are presented as follows. Remarkably, my Measurement Tool results closely approximate those from the '.MEAS' method, indicating the reliability of my findings.



3: FET’s as Resistances

In Procedure 3, our objective is to determine the resistance of the NMOS transistor. The fundamental approach involves measuring the current passing through the transistor and then dividing Vds by it to obtain the corresponding resistance. In my control file, I configured a DC analysis for Vdd, allowing it to vary from 25mV to 250mV, enabling me to obtain resistances corresponding to different Vds values simultaneously. Additionally, I set Vgate to 1.2 volts, as required.

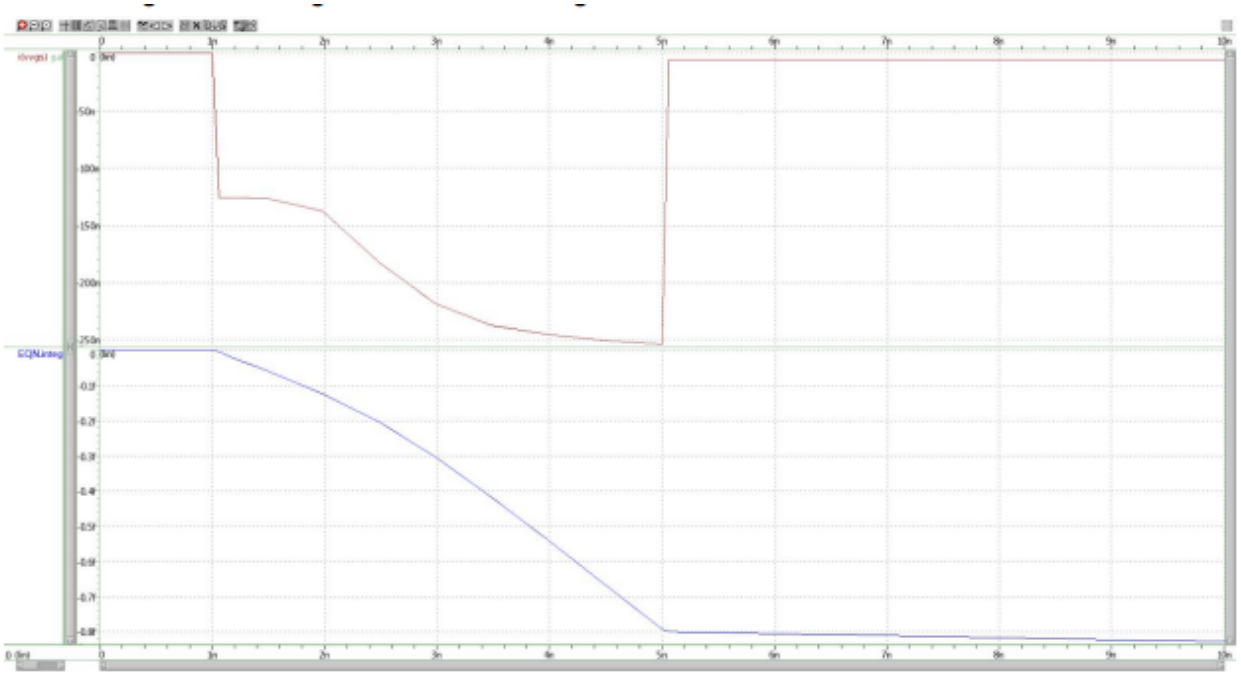
Regarding the '.MEAS' command, I initiated the process by instructing it to FIND the current flowing through the transistor. Subsequently, I used '.MEAS' to calculate Vds/Ids, and the result, as stored in the '.ms0' file, represents the desired resistance values.

In my '.ms0' file, I obtained the following results: when Vds is 25mV, the resistance is 2.845e02Ω, and when Vds is 250mV, the resistance is 3.090e02Ω.

4: Gate Capacitance

In Procedure 4, our goal is to determine the capacitance of the gate. The fundamental approach involves generating a pulse voltage and then using the '.MEAS' command to identify the current flowing through the gate. Following the measurement, we utilize the gate current waveform and the silicon explore function to calculate the charge passing through the gate over time, employing the equation $Q = \int idt$. I constructed the circuit in accordance with the provided specifications and used the PWL command to create a pulse where the gate voltage rises from 0 volts to 1 volt within 1 picosecond. Then, I employed the '.MEAS' command to compute Q.

In my '.mt0' file, I obtained a value of Q equal to -8.053e-16 Coulombs. Given that C = Q/V, the capacitance is calculated as c = 8.053e-16 F/V. To ensure the reliability of the obtained data, I utilized the Measurement Tool's function to generate an integral waveform and obtained the following result.



The accumulated charge across the gate is approximately 0.8 Coulombs, which signifies the reliability of the data in the '.mt0' file.

5: Additional Questions

Part A

In part A, my initial objective was to determine Vth. To achieve this, I identified the saturation region in my waveform and then calculated the slope of the tangent line at that point. By identifying the point where the tangent line intersected the x-axis, I calculated Vth to be approximately 0.38 volts.

Subsequently, I selected two arbitrary points within the saturation region: one with V1 = 1.19 volts and I1 = 1.1 mA, and another with V2 = 1.18 volts and I2 = 1.08 mA. Utilizing these data points along with Vth in the equation $I = \beta(V_{gs} - Vth)$, I derived a pair of equations. When I divided these equations, I effectively canceled out β and obtained a new equation in terms of n: 1 - V/n. By solving for n, I found it to be approximately 1.8. Finally, when I substituted n back into the equations, I calculated β to be approximately 0.002241.

Part B

Using a procedure similar to that in part A, we obtained the following values: Vth = 0.39 volts, n = 2.1375, and $\beta = 0.001142$.

(Point1: V1 = 1.18 volts, I1 = 551 uA; Point2: V2 = 1.19 volts, I2 = 559 uA)

Part C

1.9657

Part D

λ represents the slope of the saturation region, and I easily determined it using the Measurement Tool within Silicon Explorer by calculating the difference function. The result was $\lambda = 271$ μA/V.

Part E

Using the same procedure from part d, I get $\lambda = 87$ μA/V.

6: Bonus

To determine the capacitance components within a MOSFET device (CGS, CGD, CGB), we can set up a simulation experiment. First, we would create a circuit model of the MOSFET in a simulation tool like SPICE or Cadence. Then, we'd apply a small voltage pulse to the gate (Vgs) and monitor the resulting currents and voltages. By analyzing the waveforms, we can extract CGS (gate-to-source capacitance) from the change in Vgs and the gate current, CGD (gate-to-drain capacitance) from the change in Vgd and the drain current, and CGB (gate-to-body capacitance) from the change in Vgb and the body current. These capacitance components are essential for understanding the behavior and performance of MOSFETs in various applications like digital circuits and amplifiers.