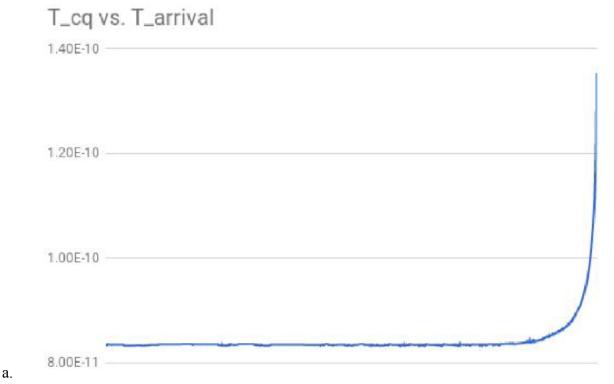
CAD 4: Master-slave Flip Flop

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Part 6: Additional Questions



- b. 1.2v. Because compared with 0.8v, 1.2v setting has smaller Tcq, which means lower delay, and smaller Tsetup and Thold, which means data can be stable within a shorter time.
- c. R+C+CC, because it has larger power consumption.
- d. R+C+CC has larger resistance, larger rise time but smaller fall time. Circuits with or without load can have huge differences.