# CAD 1: MOSFET Characteristics

EE 476 | University of Washington

## Notes

1. All MOSFET components should be from the NCSU_Devices_FreePDK45 library. The NMOS transistor is called "NMOS_VTL", and the PMOS transistor is called "PMOS_VTL".
2. The files `q1a.ctl` and `q1b.ctl` in `/home/projects/ee476/common/spice/cad1/` on ECE Linux server are templates for HSPICE control files that students may use to get started
3. Students may want to read the **Delivery** sub-sections, and **File Submission** section *before* starting

## Setup

Prepare your CAD1 directory as discussed in *Tutorial 1: Getting Started*. For instance, the design library for CAD assignment No.1 should be called "cad1." Following the guidelines for directory hygiene ensures that the TA/grader will be able to locate a student's files should any problems arise.

## CAD 1 Overview

The purpose of this lab is to build familiarity with the basic circuit characteristics of MOS transistors. This includes the behavior of NMOS and PMOS devices under various applied voltages (Part 1), as well as the characteristics of a MOSFET as a resistive device (Parts 2 and 3). The final part (Part 4) involves the measurement of MOSFET gate capacitance. Besides the concepts mentioned above, this CAD is an introduction to running experiments with standard VLSI tools, namely HSPICE and Silicon Explorer.

## WARNING!

WARNING: The figures show $L/W$ for this CAD for all Question $L = 50nm$ and $W = 1\mu m$

# 1 IV Characteristics

For each question below, use Cadence Virtuoso to create the corresponding circuit, and analyze the circuit's behavior with HSPICE and Silicon Explorer.

**a.** For the NMOS in Figure 1, plot $I_{DS}$ versus $V_{GS}$ for $V_{GS} \in [0V, 1.2V]$ (sweep $V_{GS}$ from 0V to 1.2V).

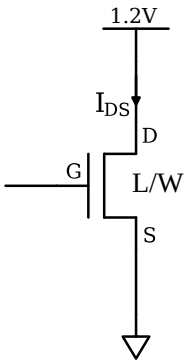


Figure 1: NMOS transistor with $W = 1\mu m$, L=50 nm.

**b.** For the two configurations in Figure 2, sweep $V_{DS}$ from 0V to 1.2V and plot $I_{DS}$ versus $V_{DS}$. In each case, what operating region(s) is the transistor in? If the transistor enters the saturation operating region, around what drain-source voltage does it do so?

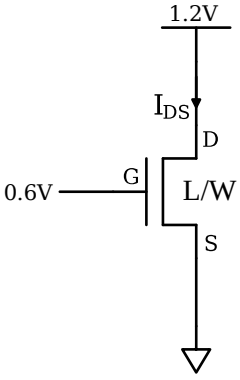


Figure 2.1

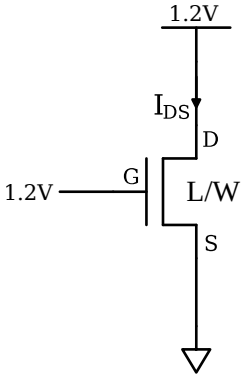


Figure 2.2

**c.** For the PMOS in Figure 3, plot $I_{SD}$ versus $V_{SG}$ for $V_{SG} \in [0V, 1.2V]$ (sweep $V_{SG}$ from 0V to 1.2V).

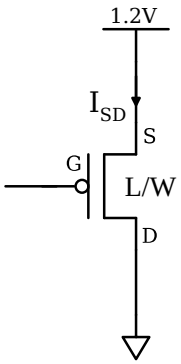


Figure 3

**d.** For the two configurations in Figure 4, sweep $V_{SD}$ from 0V to 1.2V and plot $I_{SD}$ versus $V_{SD}$. In each case, what operating region(s) is the transistor in? If the transistor enters the saturation operating region, around what drain-source voltage does it do so? (Note: $V_{SG}$ must be constant when sweeping $V_{SD}$. Do not attach the drain to the ground; use a DC voltage or make the drain as an input pin to sweep $V_{SD}$. Observe the shape and the magnitude of PMOS current in these two cases.)

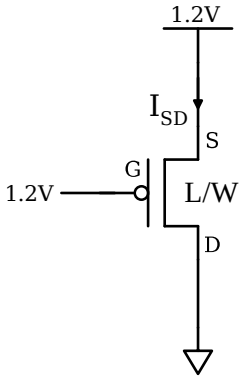


Figure 4.1

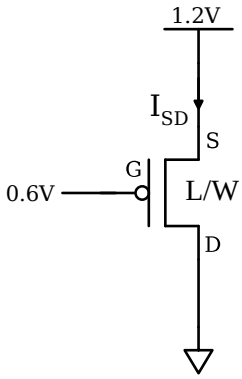


Figure 4.2

## Delivery

a. $I_{DS}$ v.s. $V_{GS}$ plot

b. $I_{DS}$ v.s. $V_{DS}$ plot for each configuration

c. $I_{SD}$ v.s. $V_{SG}$ plot

d. $I_{SD}$ v.s. $V_{SD}$ plot for each configuration

# 2 FET's *with* Resistances

**a.** Consider the two cases in Figure 5. Plot $V_o$ versus $V_i$ (sweep $V_i$ from 0V to 1.2V). Try using an HSPICE `SWEEP` to avoid manually changing the resistor value. For instance, given the line "`c0 vo vss! 10e-15`" in a circuit netlist, which denotes a 10fF capacitor named `c0`, we could change the line to "`c0 vo vss! capval`", and then use an HSPICE `SWEEP` on the parameter `capval`.

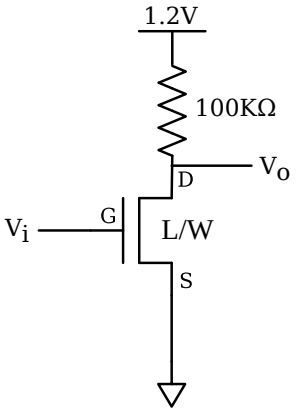


Figure 5.1

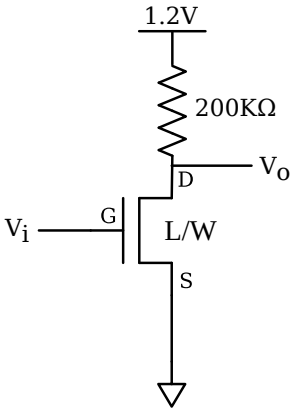


Figure 5.2

**b.** For the two configurations (Fig. 5), plot $V_o$ and $V_i$ v.s. time, where the input is a square wave. The square wave applied to $V_i$ should have a period of 500ps with a 50% duty cycle, and rise-time and fall-time of 20ps.

**c.** What is the rise-time and fall-time of $V_o$ (20% to 80%) for the circuit with the 100KΩ resistance, using the square wave from above as input? Use HSPICE to automatically collect these measurements, and the graphical measurement tools in Silicon Explorer to validate the correctness of your HSPICE measurements. (hint: use HSPICE `.measure` statements)

## Delivery

a. Plots of $V_o$ vs $V_i$ for the two configurations

b. Plots of $V_i$ and $V_o$ v.s. time for the two configurations (square wave input)

c. Rise-time and fall-time measurements (see `rise_time` and `fall_time` in the given `specifications.json` file)

# 3 FET's *as* Resistances

The two NMOSFET's below have near-zero drain-source voltages that differ by a factor of 10. What is the resistance (the small signal resistance) of the NMOS transistor at the bias point shown in each case? (Use HSPICE measurement statements.)

**a.**

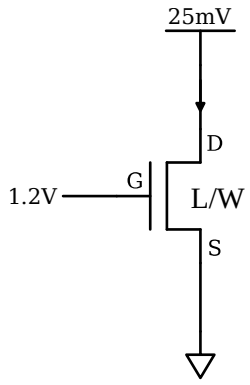


Figure 6

**b.**

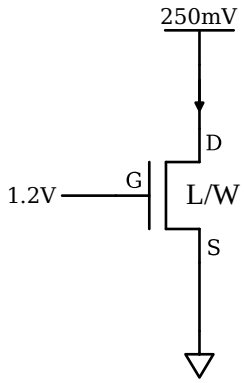


Figure 7

## Delivery

a. Resistance measurement (`resistance_25mv`)

b. Resistance measurement (`resistance_250mv`)

# 4 Gate Capacitance

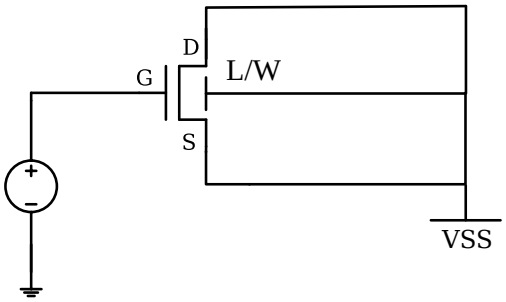


Figure 8

**a.** For the configuration shown in Figure 8, by tracking the charge delivered by the ideal voltage supply as it switches from 0V to 1V, calculate the effective capacitance of the MOSFET gate. Perform the charge measurement with HSPICE measurement statements, and use Silicon Explorer to validate the results.

Note: don't include the voltage source in your Cadence schematic. Instead, it will be easier to make the gate an input pin and model the voltage source using Spice as done in Tutorial 2.

## Delivery

a. Gate capacitance measurement (`gate_cap`)

# 5 Additional Questions

**a.** The MOSFET saturation current equation we use in class ($I_{DS} = \frac{1}{2}\beta(V_{GS} - V_{Th})^2$) is only an approximation. A slightly better approximation is $I_{DS} = \frac{1}{2}\beta(V_{GS} - V_{Th})^n$. Use the waveform you generated in Part 1.a to determine the parameters $V_{Th}$, $\beta$, and $n$ for this particular NMOS device.

**b.** Determine the same parameters from **a.** for the PMOS in Part 1.c.

**c.** What is the beta ratio of our 65nm process? Use the saturation currents of a NMOS device with $V_{GS} = 0.6$ V and $V_{DS} = 1.2$ V, and a PMOS device with $V_{SG} = 0.6$ V and $V_{SD} = 1.2$ V. (The "beta ratio" is the ratio of the NMOS to PMOS $\beta$ parameters, and is a metric to compare the relative difference in drive strength between the NMOS and PMOS devices in a particular process.)

**d.** What is the $\lambda$ (the channel-length modulation parameter) for the NMOS in Figure 2.1?

**e.** What is $\lambda$ for the PMOS in Figure 4.2?

# 6 Bonus

Describe, but do not carry out, an experiment (simulation) to determine the following capacitance components within a MOSFET device: $C_{GS}$, $C_{GD}$, $C_{GB}$. [0.2 bonus points]

## Delivery

Write a short description of the simulation setup that was used for bonus questions, and any assumptions that were made. Explain the experiments with labelled schematics.

# File Submission

All plots and answers to questions should go in a short report titled "`cad1_report.pdf`" (formats other than PDF will not be accepted). Measurements can be submitted by filling out the provided `specifications.json` file (see the *CAD Submission and Grading* document for more information).

Note: In this CAD, students do not have to submit any circuit netlists. However, in future labs where the circuits are more complex, students will usually submit netlists along with any corresponding measurements.