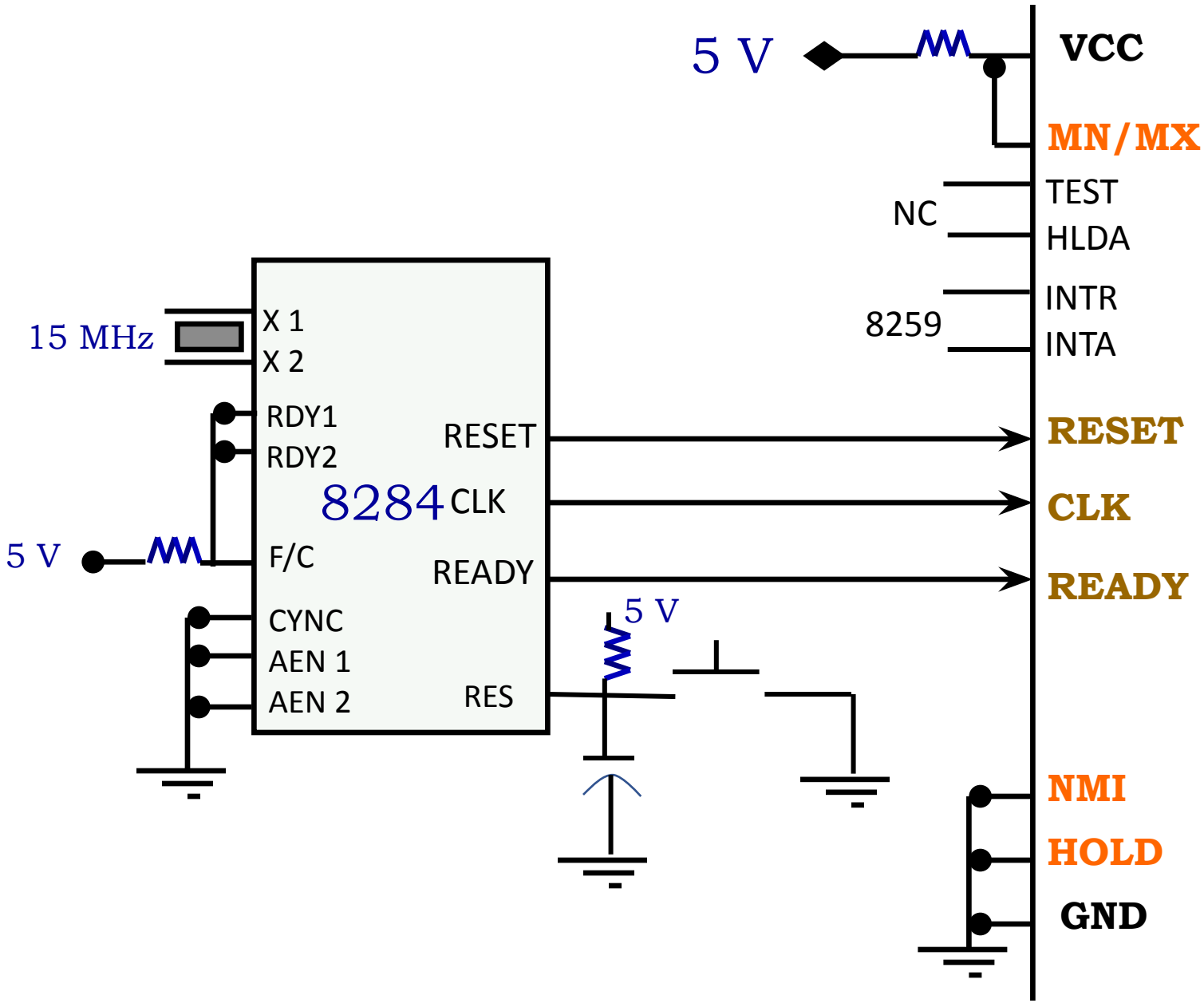
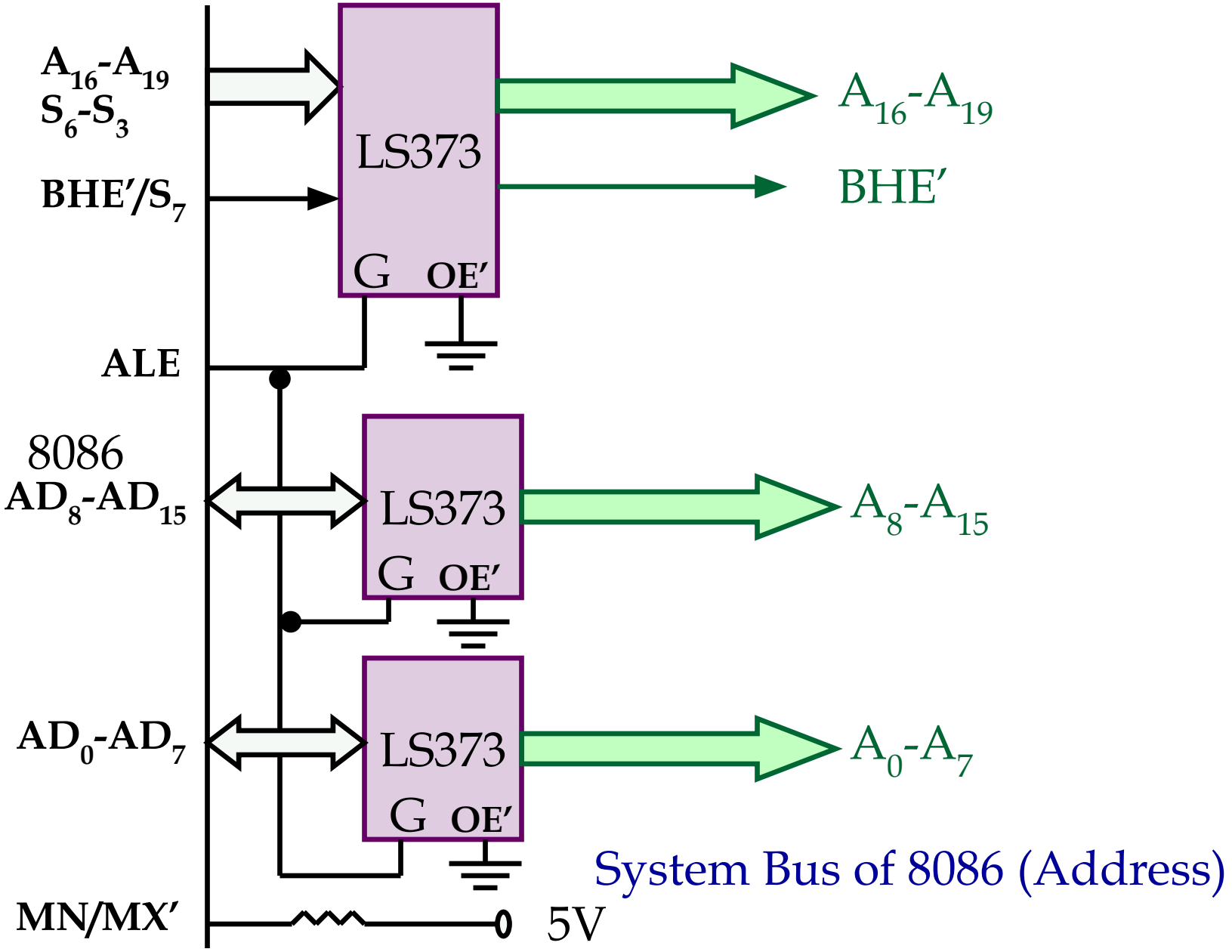
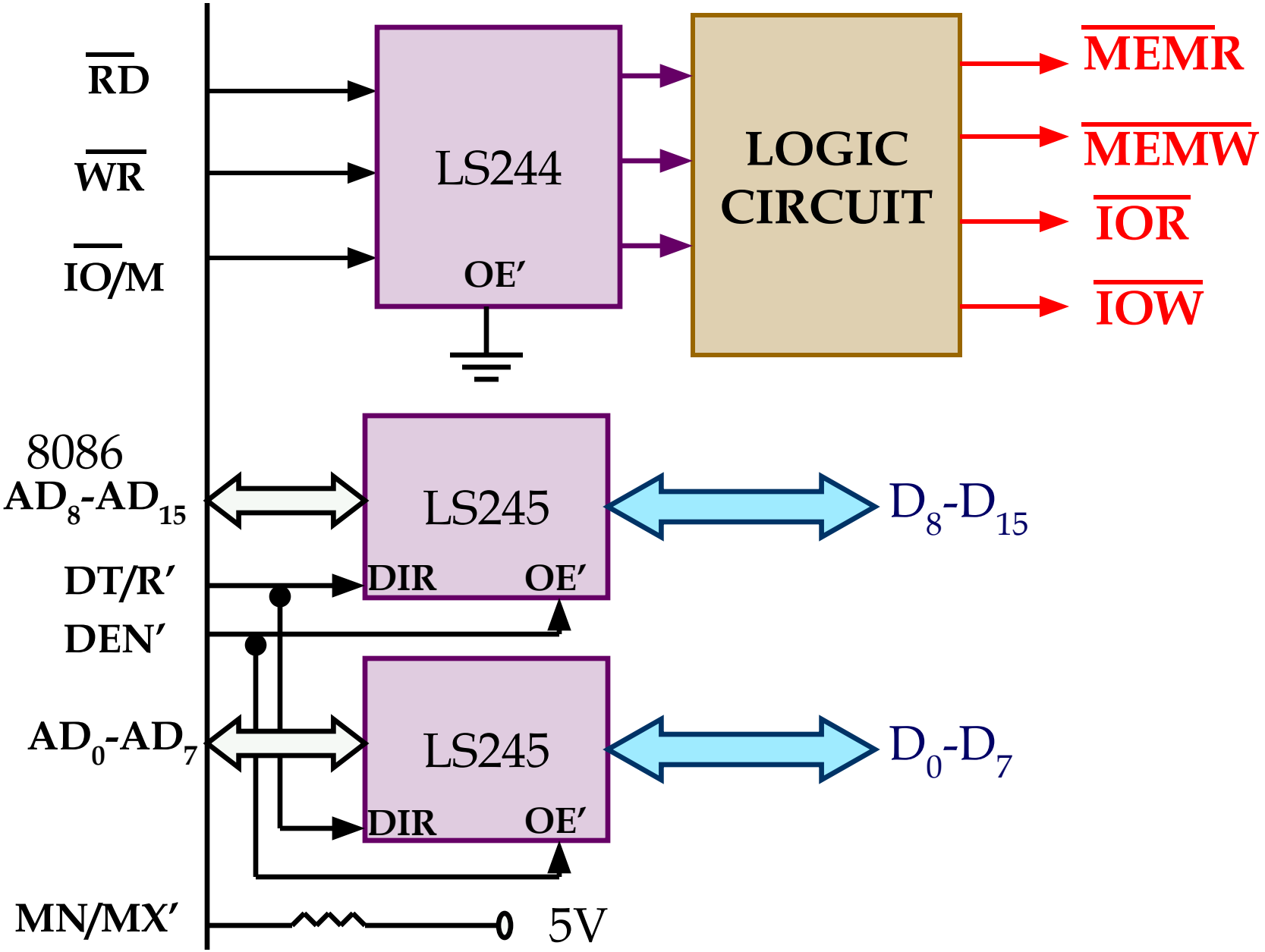

5 V
VCC
MN/MX
TEST
NC
HLDA
INTR
8259
INTA
15 MHz
X 1
X 2
RDY1
RDY2
RESET
8284
CLK
5 V
F/C
READY
CYNC
AEN 1
AEN 2
RES
5 V
RESET
CLK
READY
NMI
HOLD
GND

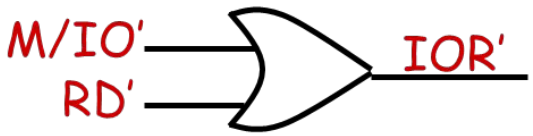
8086 Inputs

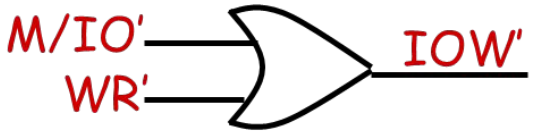


System Bus of 8086 (Address)

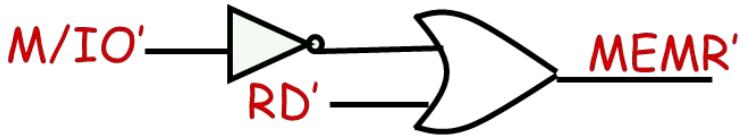


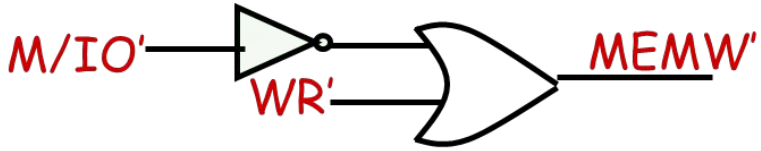
System Bus of 8086(Data + Control)



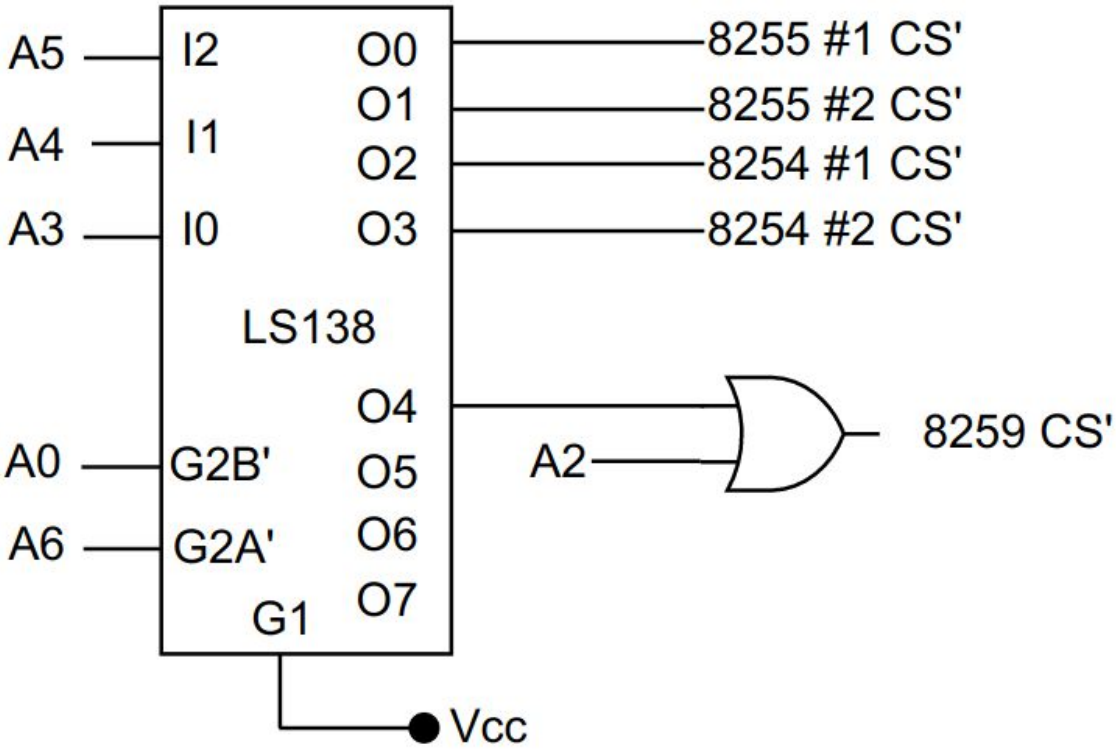


M/IO'	RD'	WR'	Bus cycle
1	0	1	MEMR'
1	1	0	MEMW'
0	0	1	IOR'
0	1	0	IOW'

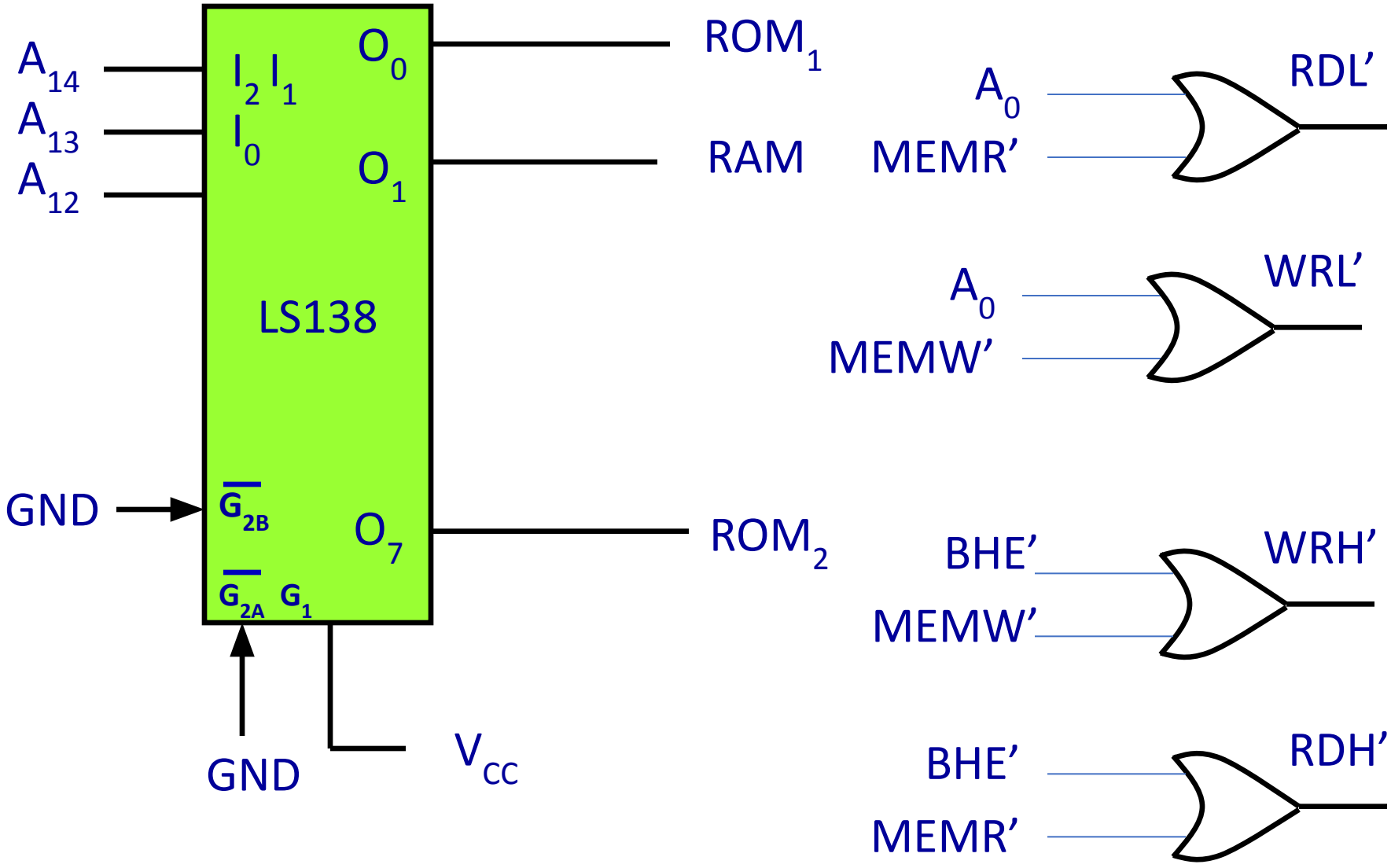




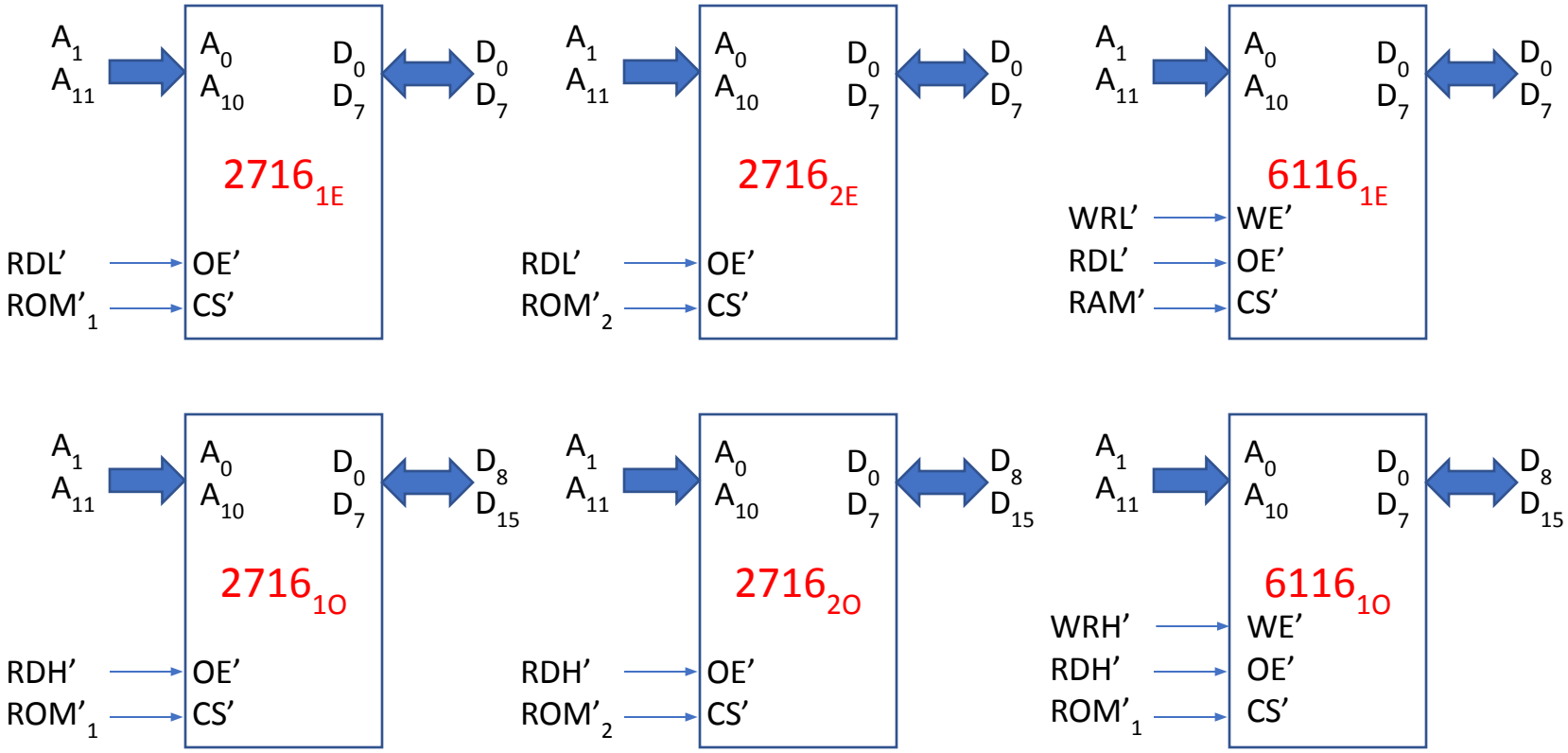
back


A5
I2
O0
8255 #1 CS'
O1
8255 #2 CS'
A4
I1
O2
8254 #1 CS'
A3
I0
O3
8254 #2 CS'
LS138
O4
8259 CS'
A0
G2B'
O5
A2
A6
G2A'
O6
O7
G1
Vcc

I/O Decoding

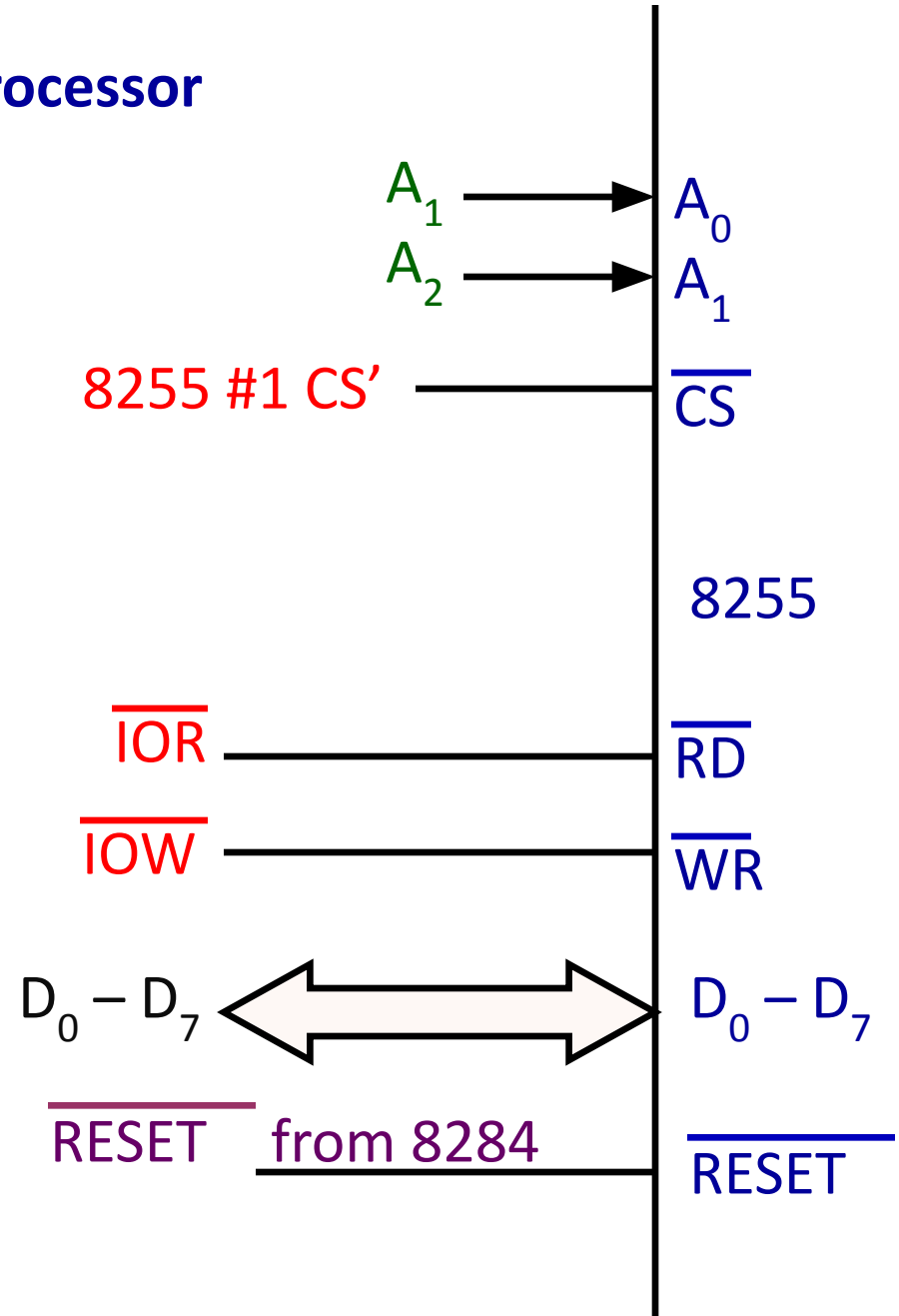


Memory Decoder

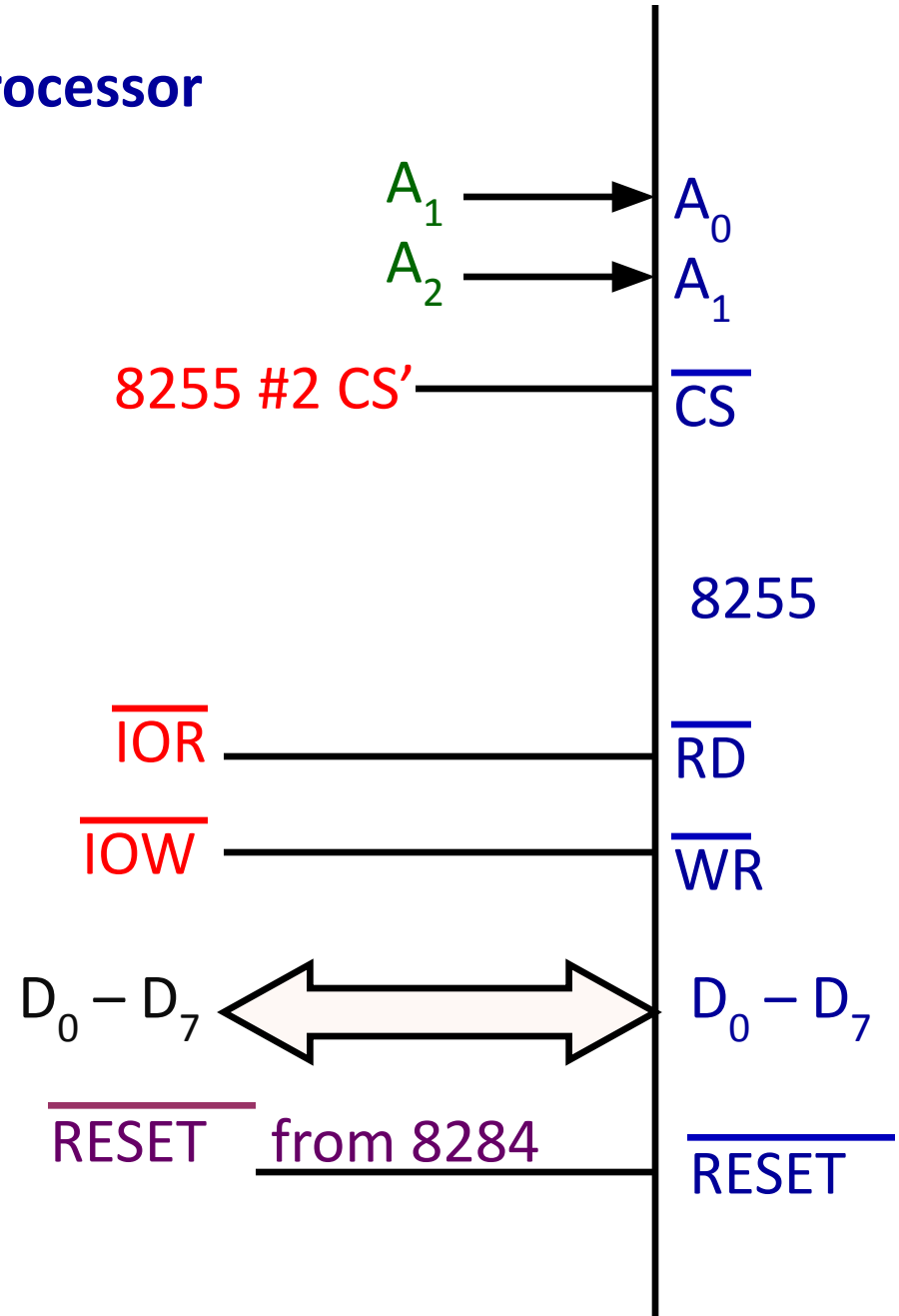


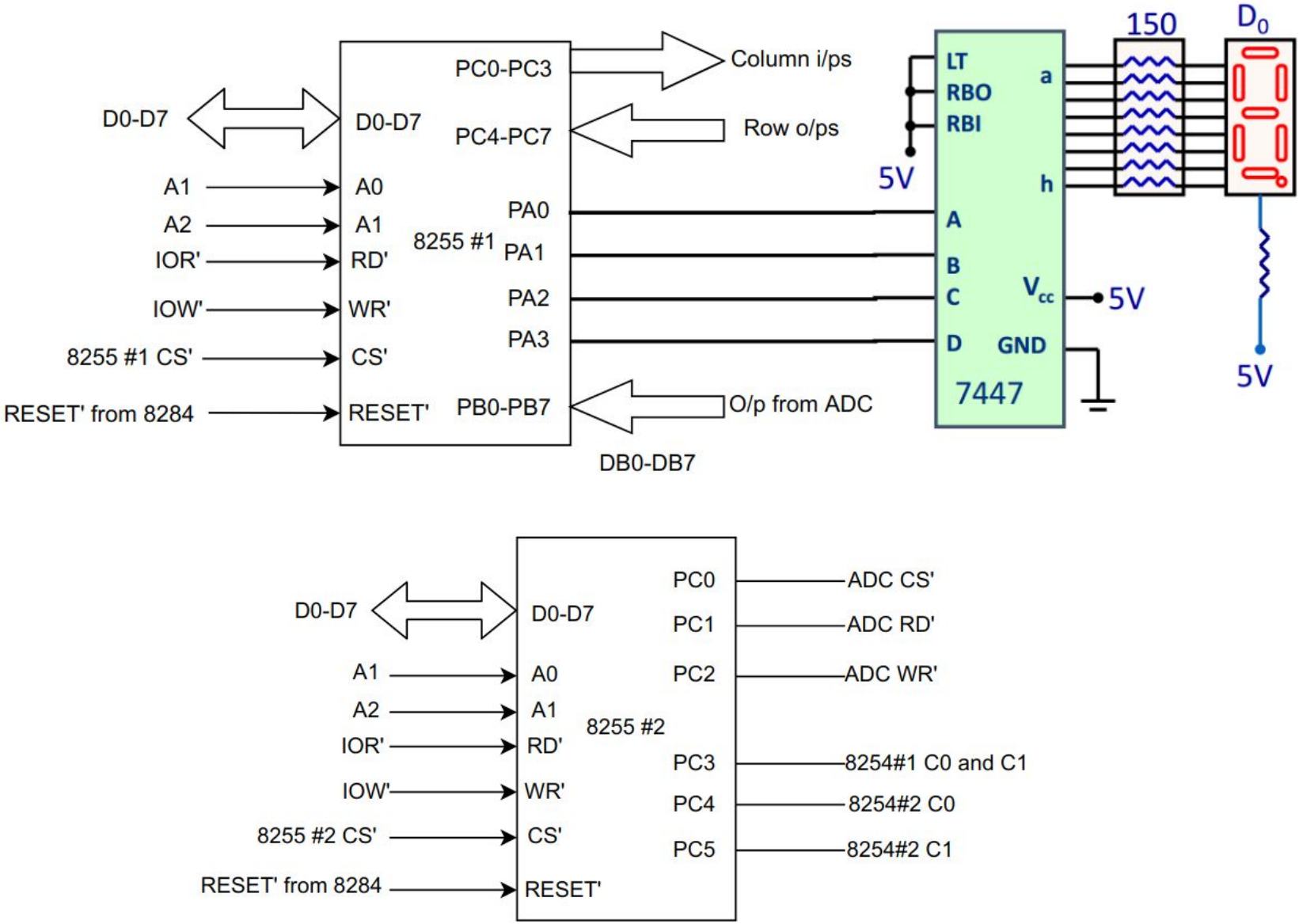
Memory Interfacing

8255 #1 Interface to the processor



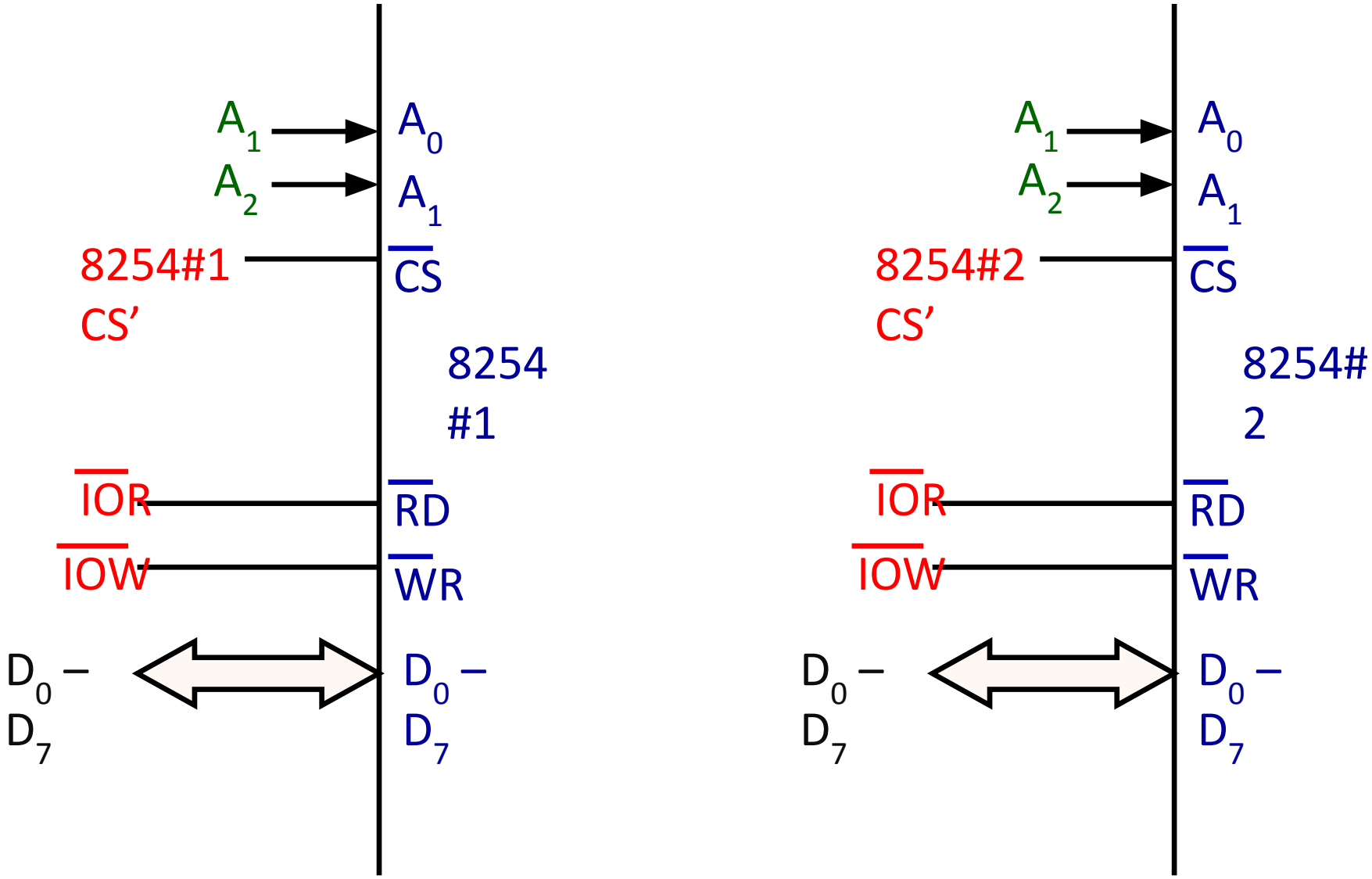
8255 #2 Interface to the processor



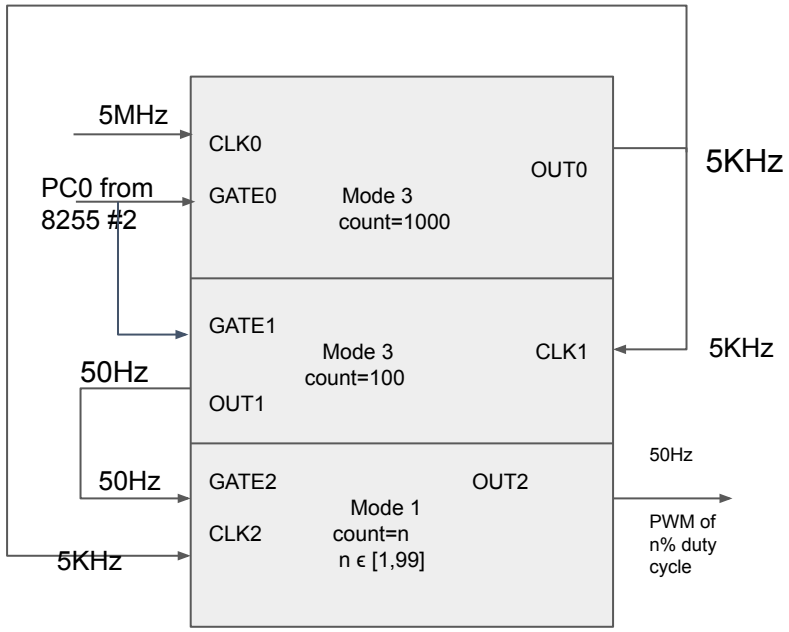

D0-D7
D0-D7
PC0-PC3
Column i/ps
PC4-PC7
Row o/ps
A1
A0
A2
A1
IOR'
RD'
8255 #1
IOW'
WR'
8255 #1 CS'
CS'
RESET' from 8284
RESET'
PA0
PA1
PA2
PA3
PB0-PB7
O/p from ADC
DB0-DB7
LT
RBO
RBI
5V
a
h
A
B
C
D
Vcc
5V
GND
7447
150
D0
5V
D0-D7
D0-D7
PC0
ADC CS'
PC1
ADC RD'
A1
A0
PC2
ADC WR'
A2
A1
IOR'
RD'
8255 #2
PC3
8254#1 C0 and C1
IOW'
WR'
PC4
8254#2 C0
8255 #2 CS'
CS'
PC5
8254#2 C1
RESET' from 8284
RESET'

8255 Pin Out

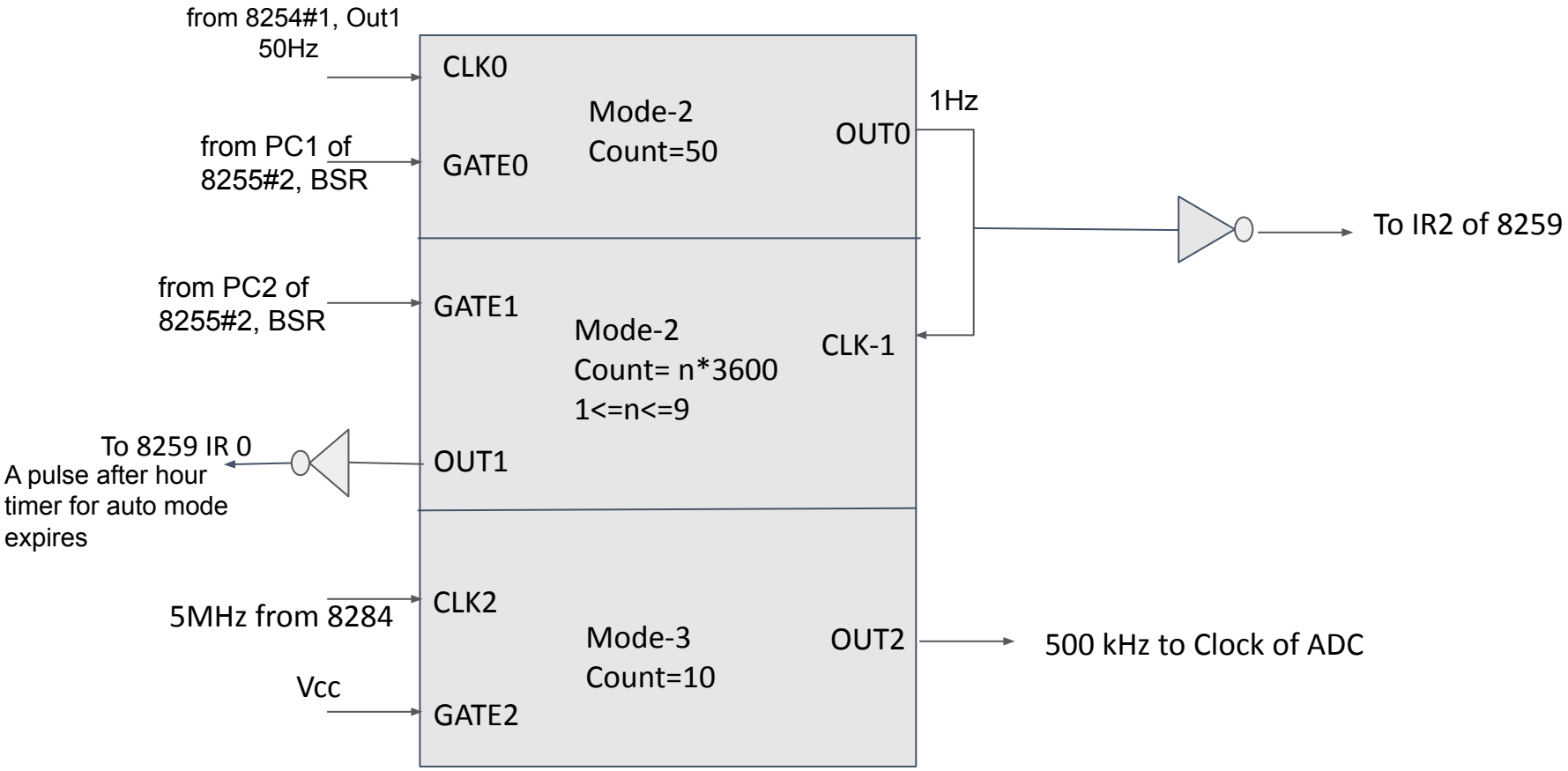
8254 Interface to the processor



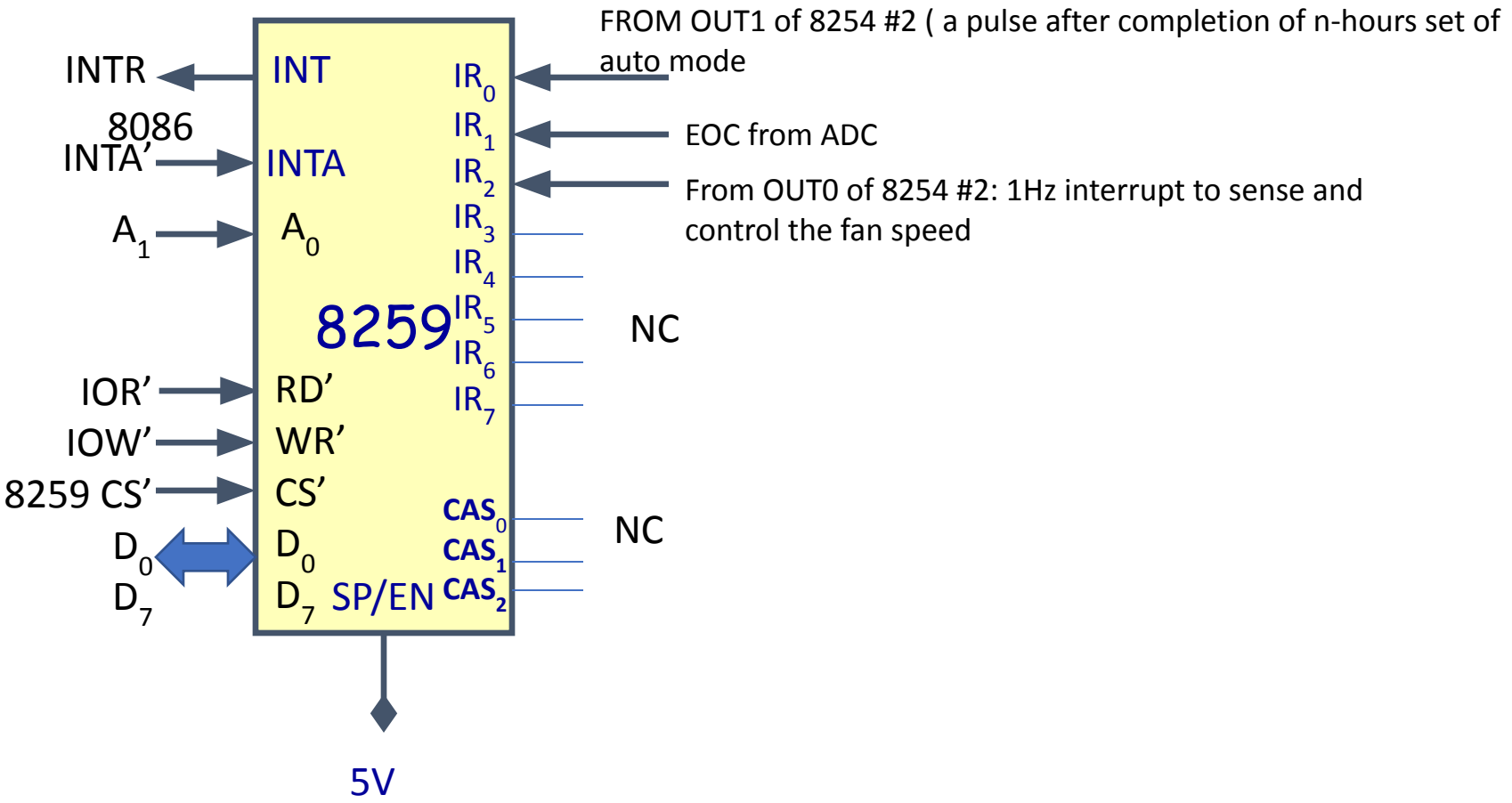
8254 Counters



8254 #1

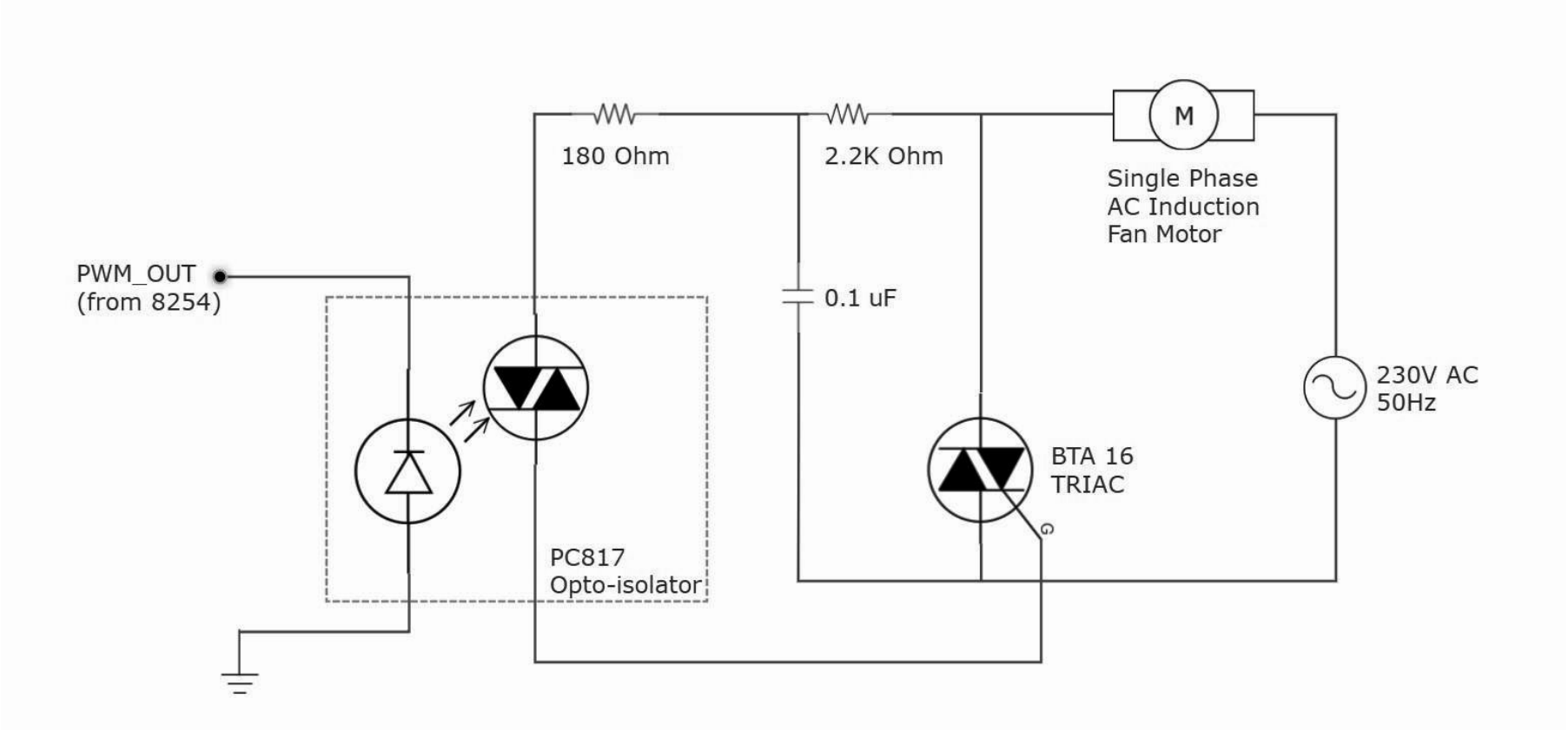

from 8254#1, Out1
50Hz
CLK0
Mode-2
Count=50
OUT0
1Hz
from PC1 of
8255#2, BSR
GATE0
To IR2 of 8259
from PC2 of
8255#2, BSR
GATE1
Mode-2
Count= n*3600
1<=n<=9
CLK-1
To 8259 IR 0
A pulse after hour
timer for auto mode
expires
OUT1
5MHz from 8284
CLK2
Mode-3
Count=10
OUT2
500 kHz to Clock of ADC
Vcc
GATE2

8254 #2


INTR
8086
INTA'
A1
IOR'
IOW'
8259 CS'
D0
D7
INT
INTA
A0
8259
RD'
WR'
CS'
D0
D7
SP/EN
IR0
IR1
IR2
IR3
IR4
IR5
IR6
IR7
CAS0
CAS1
CAS2
5V
FROM OUT1 of 8254 #2 (a pulse after completion of n-hours set of auto mode
EOC from ADC
From OUT0 of 8254 #2: 1Hz interrupt to sense and control the fan speed
NC
NC

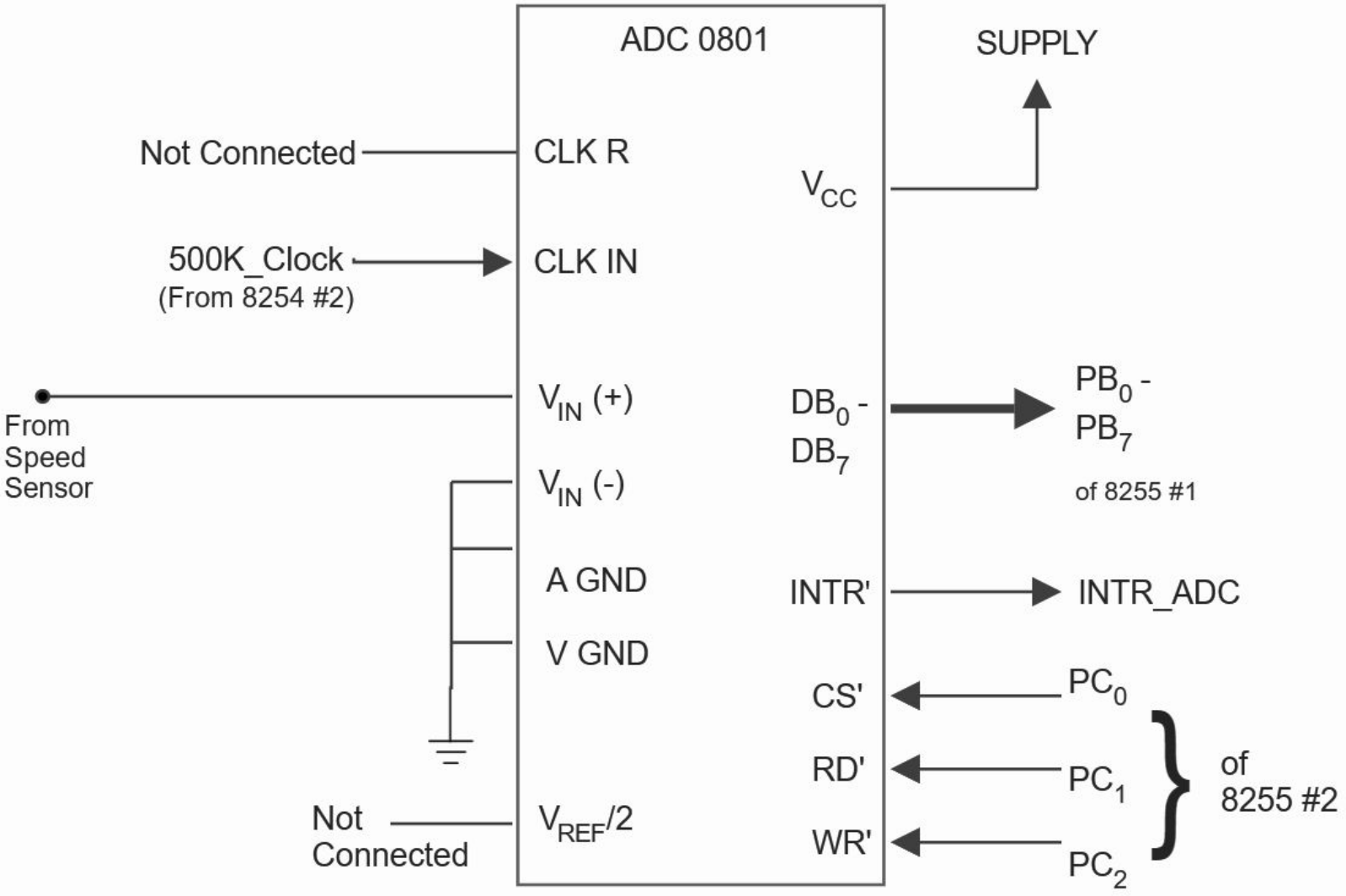
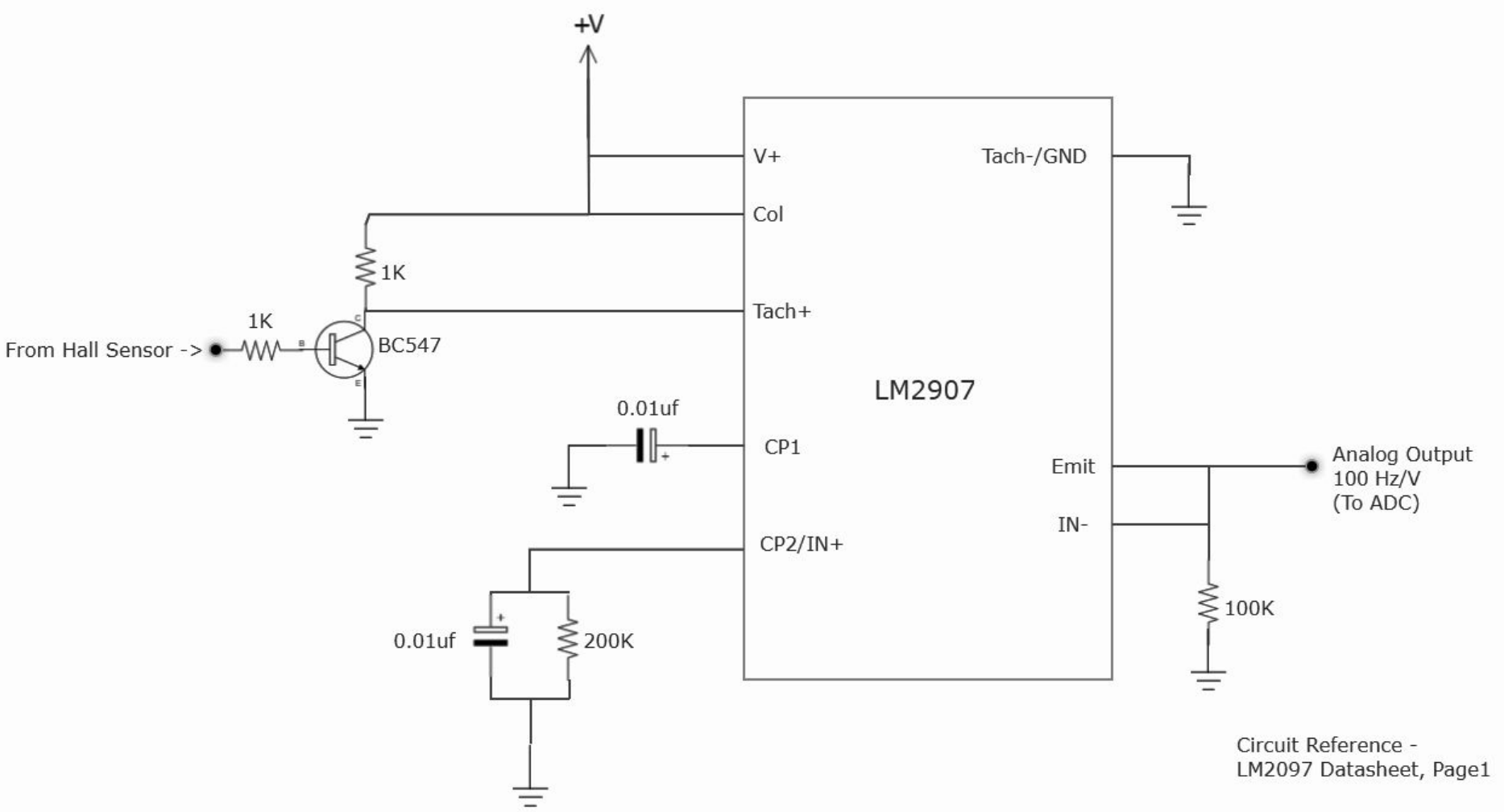
8259

Fan Controller



ADC 0801

Circuit reference -
Datasheet of ADC 0801



Fan Speed Sensor Ckt diagram