EE 709 Mid-Semester Assignment

Sarim Zafeer Farooqui
Roll Number: 24M1204
Email: 24M1204@iitb.ac.in

October 28, 2024

Instructor Information

Instructor: Madhav P. Desai
Course: Testing and Verification

Assignment Objectives

This assignment involves using SAT solving techniques to determine tests for stuck-at-faults in digital circuits. Specifically, the tasks are:

1. Constructing CNFs for good and faulty circuits.
2. Deriving the final CNF to detect faults.
3. Using SAT to determine tests for faults in small circuits and the 74181 ALU.

Problem 1: Warmup

Steps to Solve E s-a-0

1. **Good Circuit CNF (G_{cnf}):** Describe the circuit using CNF clauses. The variables are the nets A, B, ..., J. The good circuit CNF can be written as:

$$G_{cnf} = \textbf{(~(e\^{}~(a\&b))\&~(h\^{}~(a\&e))\&~(i\^{}~(b\&e))\&~(j\^{}~(h\&i)))}$$

   Here, each clause represents a condition in the good circuit, where the logic expressions correspond to the connections between the variables.

2. **Faulty Circuit CNF (F_{cnf}):** Append the clause $\bar{E}'$ to the faulty circuit's CNF. The faulty circuit CNF is modified by changing the affected variable to its negation. The faulty circuit CNF can be written as:

F_{cnf} =

(~(e1^~(a&b))&~(h1^~(a&e1))&~(i1^~(b&e1))&~(j1^~(h1&i1)))

Here, E' represents the faulty version of E, and similarly, other faulty variables such as $C', D', \ldots$ are represented accordingly.

3. **Final CNF:** Combine G_{cnf}, F_{cnf}, and the condition $J = J'$. This condition ensures that J and J' are not equal, which is modeled using multiple CNF clauses.

Final CNF for E s-a-0: $G_{cnf} \cdot F_{cnf} \cdot (J \neq J')$

(~(e^~(a&b))&~(h^~(a&e))&~(i^~(b&e))&~(j^~(h&i)))&(~(e1^~(a&b))&~(h1^~(a&e1))&~(i1^~(b&e1))&~(j1^~(h1&i1)))&(~(j^(a^b))^~(j1))

4. **SAT Solution:** Use a SAT solver to find a solution for the final CNF. The SAT solver will provide the values of A, B that detect the fault. These values are:

```
p cnf 11 27
-3 -1 -2 0
3 1 0
3 2 0
-4 -1 -3 0
4 1 0
4 3 0
-5 -2 -3 0
5 2 0
5 3 0
-6 -4 -5 0
6 4 0
6 5 0
-8 -1 -7 0
8 1 0
8 7 0
-9 -2 -7 0
9 2 0
9 7 0
-10 -8 -9 0
10 8 0
10 9 0
-11 -6 -10 0
-11 6 10 0
11 -6 10 0
11 6 -10 0
11 0
-7 0
```

```
Variable Mapping:
 A -> 1
B -> 2
E -> 3
H -> 4
I -> 5
J -> 6
E' -> 7
H' -> 8
I' -> 9
J' -> 10
K -> 11
```

```
SATISFIABLE
root@16b24952c6da:/verificatior
SAT
-1 2 3 4 -5 6 -7 8 9 -10 11 0
```

Results for Fault E s-a-0

- Test for E s-a-0: The SAT solver provides the values of A and B that detect the stuck-at-0 fault at E. For example,

$$A = 0, \quad B = 1$$

Steps to Solve F s-a-0

1. **Good Circuit CNF (G_{cnf}):** The good circuit CNF for the F fault involves the same approach as in E s-a-0, where the circuit is described with CNF clauses. The good circuit CNF is:

$$G_{cnf} = \mathbf{(\sim(e\hat{}\sim(a\&b))\&\sim(h\hat{}\sim(a\&e))\&\sim(i\hat{}\sim(b\&e))\&\sim(j\hat{}\sim(h\&i)))}\cdot$$

2. **Faulty Circuit CNF (F_{cnf}):** For F s-a-0, the faulty circuit CNF is obtained by appending the clause $\neg F'$. The faulty CNF is:

$$F_{cnf} = \mathbf{(\sim(e\hat{}\sim(a\&b))\&\sim(h2\hat{}\sim(a\&f))\&\sim(i\hat{}\sim(b\&e))\&\sim(j2\hat{}\sim(h2\&i)))}\cdot$$

   Here, F' represents the faulty version of F, and other faulty variables are similarly represented.

3. **Final CNF:** Combine G_{cnf}, F_{cnf}, and the condition $J \neq J'$. The final CNF is:

$$\text{Final CNF for F s-a-0: } G_{cnf} \cdot F_{cnf} \cdot (J \neq J')$$

(~(e^~(a&b))&~(h^~(a&e))&~(i^~(b&e))&~(j^~(h&i)))&(~(e^~(a&b))&~(h2^~(a&f))&

~(i^~(b&e))&~(j2^~(h2&i)))&(~(j^(a^b))^~(j2^(~a&b)))

4. **SAT Solution:** Use a SAT solver to find a solution for the final CNF. The SAT solver will provide the values of A, B that detect the fault. These values are:

```
SATISFIABLE
root@16b24952c6da:/verification_resou
SAT
1 -2 3 -4 5 6 -7 8 -9 10 0
root@16b24952c6da:/verification_resou
```

Results for Fault F s-a-0

- Test for F s-a-0: The SAT solver provides the values of A and B that detect the stuck-at-0 fault at F. For example,

$$A = 1, \quad B = 0$$

Problem 2: 74181 ALU

- **Test for A1 s-a-0:**

  1. **Good Circuit CNF:** The good circuit is represented with the nets A_1, B_1, C_1, ..., and logic gates. The CNF for the good circuit is derived from the datasheet and logic diagram.

(~B0 & ~B0') & (~B1 & ~B1') & (~B2 & ~B2') & (~B3 & ~B3') & (~M & ~M') & (A0 & A0 & Z1) & (B0 & S0 & Z2) & (~B0 & S1 & Z3) & (~B0 & S2 & A0 & Z4) & (B0 & A0 & S3 & Z5) & (A1 & A1 & Z6) & (B1 & S0 & Z7) & (~B1 & S1 & Z8) & (A1 & ~B1 & S2 & Z9) & (A1 & B1 & S3 & Z10) & (A2 & A2 & Z11) & (B2 & S0 & Z12) & (~B2 & S1 & Z13) & (A2 & ~B2 & S2 & Z14) & (A2 & B1 & S3 & Z15) & (A3 & A3 & Z16) & (B3 & S0 & Z17) & (~B3 & S1 & Z18) & (A3 & ~B3 & S2 & Z19) & (A3 & B3 & S3 & Z20) & ~(Z1 | Z2 | Z3) & Y1 & ~(Z4 | Z5) & Y2 & ~(Z6 | Z7 | Z8) & Y3 & ~(Z9 | Z10) & Y4 & ~(Z11 | Z12 | Z13) & Y5 & ~(Z14 | Z15) & Y6 & ~(Z16 | Z17 | Z18) & Y7 & ~(Z19 | Z20) & Y8 & (Y1 ^ Y2 & X1) & (Y3 ^ Y4 & X2) & (Y5 ^ Y6 & X3) & (Y7 ^ Y8 & X4) & ~(M' & C') & W1 & (M' & Y1 & W2) & (M' & C' & Y2 & W3) & (M' & Y3 & W4) & (M' & Y4 & Y1 & W5) & (M' & C' & Y4 & Y2 & W6) & (M' & Y5 & W7) & (M' & Y6 & Y3 & W8) & (M' & Y1 & Y4 & Y6 & W9) & (M' & C' & Y2 & Y6 & Y4 & W10) & ~(W2 | W3) & V1 & ~(W4 | W5 | W6) & V2 & ~(W7 | W8 | W9 | W10) & V3 & (X1 ^ W1 & F0) & (X2 ^ V1 & F1) & (X3 ^ V2 & F2) & (X4 ^ V3 & F3)

  2. **Faulty Circuit CNF:** The faulty circuit CNF includes the clause $\neg A'_1$, indicating that A_1 is stuck-at-0.

(~fB0 & ~fB0') & (~fB1 & ~fB1') & (~fB2 & ~fB2') & (~fB3 & ~fB3') & (~fM & ~fM') & (fA0 & fA0 & fZ1) & (fB0 & fS0 & fZ2) & (~fB0 & fS1 & fZ3) & (~fB0 & fS2 & fA0 & fZ4) & (fB0 & fA0 & fS3 & fZ5) & (fA1 & fA1 & fZ6) & (fB1 & fS0 & fZ7) & (~fB1 & fS1 & fZ8) & (fA1 & ~fB1 & fS2 & fZ9) & (fA1 & fB1 & fS3 & fZ10) & (fA2 & fA2 & fZ11) & (fB2 & fS0 & fZ12) & (~fB2 & fS1 & fZ13) & (fA2 & ~fB2 & fS2 & fZ14) & (fA2 & fB1 & fS3 & fZ15) & (fA3 & fA3 & fZ16) & (fB3 & fS0 & fZ17) & (~fB3 & fS1 & fZ18) & (fA3 & ~fB3 & fS2 & fZ19) & (fA3 & fB3 & fS3 & fZ20) & ~(fZ1 | fZ2 | fZ3) & fY1 & ~(fZ4 | fZ5) & fY2 & ~(fZ6 | fZ7 | fZ8) & fY3 & ~(fZ9 | fZ10) & fY4 & ~(fZ11 | fZ12 | fZ13) & fY5 & ~(fZ14 | fZ15) & fY6 & ~(fZ16 | fZ17 | fZ18) & fY7 & ~(fZ19 | fZ20) & fY8 & (fY1 ^ fY2 & fX1) & (fY3 ^ fY4 & fX2) & (fY5 ^ fY6 & fX3) & (fY7 ^ fY8 & fX4) & ~(fM' & fC') & fW1 & (fM' & fY1 & fW2) & (fM' & fC' & fY2 & fW3) & (fM' & fY3 & fW4) & (fM' & fY4 & fY1 & fW5) & (fM' & fC' & fY4 & fY2 & fW6) & (fM' & fY5 & fW7) & (fM' & fY6 & fY3 & fW8) & (fM' & fY1 & fY4 & fY6 & fW9) & (fM' & fC' & fY2 & fY6 & fY4 & fW10) & ~(fW2 | fW3) & fV1 & ~(fW4 | fW5 | fW6) & fV2 & ~(fW7 | fW8 | fW9 | fW10) & fV3 & (fX1 ^ fW1 & fF0) & (fX2 ^ fV1 & fF1) & (fX3 ^ fV2 & fF2) & (fX4 ^ fV3 & fF3)

  3. **Final CNF:** The final CNF combines the good circuit CNF and faulty CNF, along with the condition $F \not\equiv F'$ to detect any faults.

(F0 ^ fF0 & alpha) & (F1 ^ fF1 & beta) & (F2 ^ fF2 & gamma) & (F3 ^ fF3 & delta) & (alpha | beta & kk) & (kk | gamma & kkk) & (kkk | delta & root) (~fB0 & ~fB0') & (~fB1 & ~fB1') & (~fB2 & ~fB2') & (~fB3 & ~fB3') & (~fM & ~fM') & (fA0 & fA0 & fZ1) & (fB0 & fS0 & fZ2) & (~fB0 & fS1 & fZ3) & (~fB0 & fS2 & fA0 & fZ4) & (fB0 & fA0 & fS3 & fZ5) & (fA1 & fA1 & fZ6) & (fB1 & fS0 &

fZ7) & (~fB1 & fS1 & fZ8) & (fA1 & ~fB1 & fS2 & fZ9) & (fA1 & fB1 & fS3 & fZ10) & (fA2 & fA2 & fZ11) & (fB2 & fS0 & fZ12) & (~fB2 & fS1 & fZ13) & (fA2 & ~fB2 & fS2 & fZ14) & (fA2 & fB1 & fS3 & fZ15) & (fA3 & fA3 & fZ16) & (fB3 & fS0 & fZ17) & (~fB3 & fS1 & fZ18) & (fA3 & ~fB3 & fS2 & fZ19) & (fA3 & fB3 & fS3 & fZ20) & ~(fZ1 | fZ2 | fZ3) & fY1 & ~(fZ4 | fZ5) & fY2 & ~(fZ6 | fZ7 | fZ8) & fY3 & ~(fZ9 | fZ10) & fY4 & ~(fZ11 | fZ12 | fZ13) & fY5 & ~(fZ14 | fZ15) & fY6 & ~(fZ16 | fZ17 | fZ18) & fY7 & ~(fZ19 | fZ20) & fY8 & (fY1 ^ fY2 & fX1) & (fY3 ^ fY4 & fX2) & (fY5 ^ fY6 & fX3) & (fY7 ^ fY8 & fX4) & ~(fM' & fC') & fW1 & (fM' & fY1 & fW2) & (fM' & fC' & fY2 & fW3) & (fM' & fY3 & fW4) & (fM' & fY4 & fY1 & fW5) & (fM' & fC' & fY4 & fY2 & fW6) & (fM' & fY5 & fW7) & (fM' & fY6 & fY3 & fW8) & (fM' & fY1 & fY4 & fY6 & fW9) & (fM' & fC' & fY2 & fY6 & fY4 & fW10) & ~(fW2 | fW3) & fV1 & ~(fW4 | fW5 | fW6) & fV2 & ~(fW7 | fW8 | fW9 | fW10) & fV3 & (fX1 ^ fW1 & fF0) & (fX2 ^ fV1 & fF1) & (fX3 ^ fV2 & fF2) & (fX4 ^ fV3 & fF3) (~B0 & ~B0') & (~B1 & ~B1') & (~B2 & ~B2') & (~B3 & ~B3') & (~M & ~M') & (A0 & A0 & Z1) & (B0 & S0 & Z2) & (~B0 & S1 & Z3) & (~B0 & S2 & A0 & Z4) & (B0 & A0 & S3 & Z5) & (A1 & A1 & Z6) & (B1 & S0 & Z7) & (~B1 & S1 & Z8) & (A1 & ~B1 & S2 & Z9) & (A1 & B1 & S3 & Z10) & (A2 & A2 & Z11) & (B2 & S0 & Z12) & (~B2 & S1 & Z13) & (A2 & ~B2 & S2 & Z14) & (A2 & B1 & S3 & Z15) & (A3 & A3 & Z16) & (B3 & S0 & Z17) & (~B3 & S1 & Z18) & (A3 & ~B3 & S2 & Z19) & (A3 & B3 & S3 & Z20) & ~(Z1 | Z2 | Z3) & Y1 & ~(Z4 | Z5) & Y2 & ~(Z6 | Z7 | Z8) & Y3 & ~(Z9 | Z10) & Y4 & ~(Z11 | Z12 | Z13) & Y5 & ~(Z14 | Z15) & Y6 & ~(Z16 | Z17 | Z18) & Y7 & ~(Z19 | Z20) & Y8 & (Y1 ^ Y2 & X1) & (Y3 ^ Y4 & X2) & (Y5 ^ Y6 & X3) & (Y7 ^ Y8 & X4) & ~(M' & C') & W1 & (M' & Y1 & W2) & (M' & C' & Y2 & W3) & (M' & Y3 & W4) & (M' & Y4 & Y1 & W5) & (M' & C' & Y4 & Y2 & W6) & (M' & Y5 & W7) & (M' & Y6 & Y3 & W8) & (M' & Y1 & Y4 & Y6 & W9) & (M' & C' & Y2 & Y6 & Y4 & W10) & ~(W2 | W3) & V1 & ~(W4 | W5 | W6) & V2 & ~(W7 | W8 | W9 | W10) & V3 & (X1 ^ W1 & F0) & (X2 ^ V1 & F1) & (X3 ^ V2 & F2) & (X4 ^ V3 & F3)

&(~A1) &(root)

4. **SAT Solution:** Use a SAT solver to find the input tests for A_1 s-a-0 that cause a fault to be detected.
5. **We gave constraints in the final CNF A1=0 and Output of XOR(root)=1**

```
============================[ Problem Statistics ]=============================
|                                                                             |
|  Number of variables:          130                                          |
|  Number of clauses:            405                                          |
|  Parse time:                  0.00 s                                        |
|                                                                             |
============================[ Search Statistics ]==============================
| Conflicts |          ORIGINAL         |          LEARNT          | Progress |
|           |    Vars  Clauses Literals |    Limit  Clauses Lit/Cl |          |
===============================================================================
===============================================================================
restarts              : 1
conflicts             : 13             (11207 /sec)
decisions             : 85             (0.00 % random) (73276 /sec)
propagations          : 769            (662931 /sec)
conflict literals     : 25             (0.00 % deleted)
Memory used           : 6.00 MB
CPU time              : 0.00116 s

SATISFIABLE
root@16b24952c6da:/verification_resources/minisat_for_class/test# cat 10.result
SAT
-1 2 3 -4 -5 6 7 -8 9 -10 -11 -12 -13 -14 -15 -16 17 -18 19 -20 -21 -22 -23 -24 -25 -26 27 28 -29 -30 31 32 -33 -34 -35
-36 -37 -38 -39 -40 -41 -42 -43 44 -45 -46 -47 -48 49 -50 -51 52 -53 -54 -55 -56 -57 -58 -59 -60 -61 -62 -63 -64 65 -66
67 -68 69 -70 71 -72 -73 -74 -75 -76 -77 -78 79 80 -81 -82 -83 84 85 -86 -87 88 -89 -90 -91 -92 -93 -94 -95 -96 -97 -98
-99 -100 -101 -102 -103 -104 -105 -106 107 -108 -109 -110 -111 -112 -113 -114 -115 -116 -117 -118 -119 120 -121 -122 -12
3 -124 -125 126 -127 -128 129 130 0
root@16b24952c6da:/verification_resources/minisat_for_class/test#
```

6.

- **Test for A2 s-a-1 and F2 s-a-1:**

1. **Good Circuit CNF:** The good circuit is described using the nets and logic diagram, as shown in the datasheet.

(~B0 & ~B0') & (~B1 & ~B1') & (~B2 & ~B2') & (~B3 & ~B3') & (~M & ~M') & (A0 & A0 & Z1) & (B0 & S0 & Z2) & (~B0 & S1 & Z3) & (~B0 & S2 & A0 & Z4) & (B0 & A0 & S3 & Z5) & (A1 & A1 & Z6) & (B1 & S0 & Z7) & (~B1 & S1 & Z8) & (A1 & ~B1 & S2 & Z9) & (A1 & B1 & S3 & Z10) & (A2 & A2 & Z11) & (B2 & S0 & Z12) & (~B2 & S1 & Z13) & (A2 & ~B2 & S2 & Z14) & (A2 & B1 & S3 & Z15) & (A3 & A3 & Z16) & (B3 & S0 & Z17) & (~B3 & S1 & Z18) & (A3 & ~B3 & S2 & Z19) & (A3 & B3 & S3 & Z20) & ~(Z1 | Z2 | Z3) & Y1 & ~(Z4 | Z5) & Y2 & ~(Z6 | Z7 | Z8) & Y3 & ~(Z9 | Z10) & Y4 & ~(Z11 | Z12 | Z13) & Y5 & ~(Z14 | Z15) & Y6 & ~(Z16 | Z17 | Z18) & Y7 & ~(Z19 | Z20) & Y8 & (Y1 ^ Y2 & X1) & (Y3 ^ Y4 & X2) & (Y5 ^ Y6 & X3) & (Y7 ^ Y8 & X4) & ~(M' & C') & W1 & (M' & Y1 & W2) & (M' & C' & Y2 & W3) & (M' & Y3 & W4) & (M' & Y4 & Y1 & W5) & (M' & C' & Y4 & Y2 & W6) & (M' & Y5 & W7) & (M' & Y6 & Y3 & W8) & (M' & Y1 & Y4 & Y6 & W9) & (M' & C' & Y2 & Y6 & Y4 & W10) & ~(W2 | W3) & V1 & ~(W4 | W5 | W6) & V2 & ~(W7 | W8 | W9 | W10) & V3 & (X1 ^ W1 & F0) & (X2 ^ V1 & F1) & (X3 ^ V2 & F2) & (X4 ^ V3 & F3)

2. **Faulty Circuit CNF:** The faulty circuit CNF includes the clauses $\neg A_2'$ and $\neg F_2'$, indicating that A_2 is stuck-at-1 and F_2 is stuck-at-1.

(~fB0 & ~fB0') & (~fB1 & ~fB1') & (~fB2 & ~fB2') & (~fB3 & ~fB3') & (~fM & ~fM') & (fA0 & fA0 & fZ1) & (fB0 & fS0 & fZ2) & (~fB0 & fS1 & fZ3) & (~fB0 & fS2 & fA0 & fZ4) & (fB0 & fA0 & fS3 & fZ5) & (fA1 & fA1 & fZ6) & (fB1 & fS0 & fZ7) & (~fB1 & fS1 & fZ8) & (fA1 & ~fB1 & fS2 & fZ9) & (fA1 & fB1 & fS3 & fZ10) & (fA2 & fA2 & fZ11) & (fB2 & fS0 & fZ12) & (~fB2 & fS1 & fZ13) & (fA2 & ~fB2 & fS2 & fZ14) & (fA2 & fB1 & fS3 & fZ15) & (fA3 & fA3 & fZ16) & (fB3 & fS0 & fZ17) & (~fB3 & fS1 & fZ18) & (fA3 & ~fB3 & fS2 & fZ19) & (fA3 & fB3 & fS3 & fZ20) & ~(fZ1 | fZ2 | fZ3) & fY1 & ~(fZ4 | fZ5) & fY2 & ~(fZ6 | fZ7 | fZ8) & fY3 & ~(fZ9 | fZ10) & fY4 & ~(fZ11 | fZ12 | fZ13) & fY5 & ~(fZ14 | fZ15) & fY6 & ~(fZ16 | fZ17 | fZ18) & fY7 & ~(fZ19 | fZ20) & fY8 & (fY1 ^ fY2 & fX1) & (fY3 ^ fY4 & fX2) & (fY5 ^ fY6 & fX3) & (fY7 ^ fY8 & fX4) & ~(fM' & fC') & fW1 & (fM' & fY1 & fW2) & (fM' & fC' & fY2 & fW3) & (fM' & fY3 & fW4) & (fM' & fY4 & fY1 & fW5) & (fM' & fC' & fY4 & fY2 & fW6) & (fM' & fY5 & fW7) & (fM' & fY6 & fY3 & fW8) & (fM' & fY1 & fY4 & fY6 & fW9) & (fM' & fC' & fY2 & fY6 & fY4 & fW10) & ~(fW2 | fW3) & fV1 & ~(fW4 | fW5 | fW6) & fV2 & ~(fW7 | fW8 | fW9 | fW10) & fV3 & (fX1 ^ fW1 & fF0) & (fX2 ^ fV1 & fF1) & (fX3 ^ fV2 & fF2) & (fX4 ^ fV3 & fF3)

3. **Final CNF:** The final CNF combines the good and faulty CNFs, including the stuck-at conditions for A_2 and F_2 and the condition $F \neq F'$.

(F0 ^ fF0 & alpha) & (F1 ^ fF1 & beta) & (F2 ^ fF2 & gamma) & (F3 ^ fF3 & delta) & (alpha | beta & kk) & (kk | gamma & kkk) & (kkk | delta & root) (~fB0 & ~fB0') & (~fB1 & ~fB1') & (~fB2 & ~fB2') & (~fB3 & ~fB3') & (~fM & ~fM') & (fA0 & fA0 & fZ1) & (fB0 & fS0 & fZ2) & (~fB0 & fS1 & fZ3) & (~fB0 & fS2 & fA0 & fZ4) & (fB0 & fA0 & fS3 & fZ5) & (fA1 & fA1 & fZ6) & (fB1 & fS0 & fZ7) & (~fB1 & fS1 & fZ8) & (fA1 & ~fB1 & fS2 & fZ9) & (fA1 & fB1 & fS3 & fZ10) & (fA2 & fA2 & fZ11) & (fB2 & fS0 & fZ12) & (~fB2 & fS1 & fZ13) & (fA2 & ~fB2 & fS2 & fZ14) & (fA2 & fB1 & fS3 & fZ15) & (fA3 & fA3 & fZ16) & (fB3 & fS0 & fZ17) & (~fB3 & fS1 & fZ18) & (fA3 & ~fB3 & fS2 & fZ19) & (fA3 & fB3 & fS3 & fZ20) & ~(fZ1 | fZ2 | fZ3) & fY1 & ~(fZ4 | fZ5) & fY2 & ~(fZ6 | fZ7 | fZ8) & fY3 & ~(fZ9 | fZ10) & fY4 & ~(fZ11 | fZ12 | fZ13) & fY5 & ~(fZ14 | fZ15) & fY6 & ~(fZ16 | fZ17 | fZ18) & fY7 & ~(fZ19 | fZ20) & fY8 & (fY1 ^ fY2 & fX1) & (fY3 ^ fY4 & fX2) & (fY5 ^ fY6 & fX3) & (fY7 ^ fY8 & fX4) & ~(fM' & fC') & fW1 & (fM' & fY1 & fW2) & (fM' & fC' & fY2 & fW3) & (fM' & fY3 & fW4) & (fM' & fY4 & fY1 & fW5) & (fM' & fC' & fY4 & fY2 & fW6) & (fM' & fY5 & fW7) & (fM' & fY6 & fY3 & fW8) & (fM' & fY1 & fY4 & fY6 & fW9) & (fM' & fC' & fY2 & fY6 & fY4 & fW10) & ~(fW2 | fW3) & fV1 & ~(fW4 | fW5 | fW6) & fV2 & ~(fW7 | fW8 | fW9 | fW10) & fV3 & (fX1 ^ fW1 & fF0) & (fX2 ^ fV1 & fF1) & (fX3 ^ fV2 & fF2) & (fX4 ^ fV3 & fF3)

(~B0 & ~B0') & (~B1 & ~B1') & (~B2 & ~B2') & (~B3 & ~B3') & (~M & ~M') & (A0 & A0 & Z1) & (B0 & S0 & Z2) & (~B0 & S1 & Z3) & (~B0 & S2 & A0 & Z4) & (B0 & A0 & S3 & Z5) & (A1 & A1 & Z6) & (B1 & S0 & Z7) & (~B1 & S1 & Z8) & (A1 & ~B1 & S2 & Z9) & (A1 & B1 & S3 & Z10) & (A2 & A2 & Z11) & (B2 & S0 & Z12) & (~B2 & S1 & Z13) & (A2 & ~B2 & S2 & Z14) & (A2 & B1 & S3 & Z15) & (A3 & A3 & Z16) & (B3 & S0 & Z17) & (~B3 & S1 & Z18) & (A3 & ~B3 & S2 & Z19) & (A3 & B3 & S3 & Z20) & ~(Z1 | Z2 | Z3) & Y1 & ~(Z4 | Z5) & Y2 & ~(Z6 | Z7 | Z8) & Y3 & ~(Z9 | Z10) & Y4 & ~(Z11 | Z12 | Z13) & Y5 & ~(Z14 | Z15) & Y6 & ~(Z16 | Z17 | Z18) & Y7 & ~(Z19 | Z20) & Y8 & (Y1 ^ Y2 & X1) & (Y3 ^ Y4 & X2) & (Y5 ^ Y6 & X3) & (Y7 ^ Y8 & X4) & ~(M' & C') & W1 & (M' & Y1 & W2) & (M' & C' & Y2 & W3) & (M' & Y3 & W4) & (M' & Y4 & Y1 & W5) & (M' & C' & Y4 & Y2 & W6) & (M' & Y5 & W7) & (M' & Y6 & Y3 & W8) & (M' & Y1 & Y4 & Y6 & W9) & (M' & C' & Y2 & Y6 & Y4 & W10) & ~(W2 | W3) & V1 & ~(W4 | W5 | W6) & V2 & ~(W7 | W8 | W9 | W10) & V3 & (X1 ^ W1 & F0) & (X2 ^ V1 & F1) & (X3 ^ V2 & F2) & (X4 ^ V3 & F3)
& (A2) &(F2) & (root)

4. **SAT Solution:** The SAT solver is used to determine the input values for which both A_2 s-a-1 and F_2 s-a-1 faults are detected.
    - **We gave constraints in the final CNF A2=1, F2=0 and Output of XOR(root)=1**
5.
```
============================[ Problem Statistics ]=============================
|                                                                             |
|  Number of variables:           143                                         |
|  Number of clauses:             405                                         |
|  Parse time:                   0.00 s                                       |
|                                                                             |
============================[ Search Statistics ]==============================
| Conflicts |          ORIGINAL         |          LEARNT          | Progress |
|           |    Vars  Clauses Literals |    Limit  Clauses Lit/Cl |          |
==============================================================================
==============================================================================
restarts              : 1
conflicts             : 6              (8345 /sec)
decisions             : 108            (0.00 % random) (150209 /sec)
propagations          : 582            (809458 /sec)
conflict literals     : 7              (0.00 % deleted)
Memory used           : 6.00 MB
CPU time              : 0.000719 s

SATISFIABLE
root@16b24952c6da:/verification_resources/minisat_for_class/test# cat 6.result
SAT
-1 2 3 -4 -5 6 -7 8 9 -10 11 12 -13 -14 15 16 17 18 19 -20 -21 -22 -23 -24 -25 -26 27 28 -29 30 31 32 33 34 -35 36 37 -3
8 -39 -40 -41 -42 -43 44 -45 -46 -47 -48 49 -50 51 52 -53 -54 -55 -56 -57 -58 -59 -60 -61 -62 -63 -64 65 -66 67 -68 -69
70 71 -72 -73 74 -75 76 -77 78 79 80 81 -82 83 84 85 86 87 -88 89 90 91 -92 -93 94 95 96 -97 98 99 100 -101 -102 -103 10
4 -105 -106 -107 -108 -109 -110 -111 112 -113 -114 -115 -116 117 -118 119 -120 -121 -122 -123 -124 -125 -126 -127 -128 -
129 -130 -131 -132 -133 -134 135 -136 137 -138 -139 -140 141 142 143 0
root@16b24952c6da:/verification_resources/minisat_for_class/test#
```
6.

- **Test for F1 s-a-0:**

1. **Good Circuit CNF:** The good circuit is represented by its nets and logic gates, following the datasheet for simplification.

(~B0 & ~B0') & (~B1 & ~B1') & (~B2 & ~B2') & (~B3 & ~B3') & (~M & ~M') & (A0 & A0 & Z1) & (B0 & S0 & Z2) & (~B0 & S1 & Z3) & (~B0 & S2 & A0 & Z4) & (B0 & A0 & S3 & Z5) & (A1 & A1 & Z6) & (B1 & S0 & Z7) & (~B1 & S1 & Z8) & (A1 & ~B1 & S2 & Z9) & (A1 & B1 & S3 & Z10) & (A2 & A2 & Z11) & (B2 & S0 & Z12) & (~B2 & S1 & Z13) & (A2 & ~B2 & S2 & Z14) & (A2 & B1 & S3 & Z15) & (A3 & A3 & Z16) & (B3 & S0 & Z17) & (~B3 & S1 & Z18) & (A3 & ~B3 & S2 & Z19) & (A3 & B3 & S3 & Z20) & ~(Z1 | Z2 | Z3) & Y1 & ~(Z4 | Z5) & Y2 & ~(Z6 | Z7 | Z8) & Y3 & ~(Z9 | Z10) & Y4 & ~(Z11 | Z12 | Z13) & Y5 & ~(Z14 | Z15) & Y6 & ~(Z16 | Z17 | Z18) & Y7 & ~(Z19 | Z20) & Y8 & (Y1 ^ Y2 & X1) & (Y3 ^ Y4 & X2) & (Y5 ^ Y6 & X3) & (Y7 ^ Y8 & X4) & ~(M' & C') & W1 & (M' & Y1 & W2) & (M' & C' & Y2 & W3) & (M' & Y3 & W4) & (M' & Y4 & Y1 & W5) & (M' & C' & Y4 & Y2 & W6) & (M' & Y5 & W7) & (M' & Y6 & Y3 & W8) & (M' & Y1 & Y4 & Y6 & W9) & (M' & C' & Y2 & Y6 & Y4 & W10) & ~(W2 | W3) & V1 & ~(W4 | W5 | W6) & V2 & ~(W7 | W8

| W9 | W10) & V3 & (X1 ^ W1 & F0) & (X2 ^ V1 & F1) & (X3 ^ V2 & F2) & (X4 ^ V3 & F3)

2. **Faulty Circuit CNF:** The faulty circuit CNF includes the clause $\neg F_1^{'}$, indicating that F_1 is stuck-at-0.

(~fB0 & ~fB0') & (~fB1 & ~fB1') & (~fB2 & ~fB2') & (~fB3 & ~fB3') & (~fM & ~fM') & (fA0 & fA0 & fZ1) & (fB0 & fS0 & fZ2) & (~fB0 & fS1 & fZ3) & (~fB0 & fS2 & fA0 & fZ4) & (fB0 & fA0 & fS3 & fZ5) & (fA1 & fA1 & fZ6) & (fB1 & fS0 & fZ7) & (~fB1 & fS1 & fZ8) & (fA1 & ~fB1 & fS2 & fZ9) & (fA1 & fB1 & fS3 & fZ10) & (fA2 & fA2 & fZ11) & (fB2 & fS0 & fZ12) & (~fB2 & fS1 & fZ13) & (fA2 & ~fB2 & fS2 & fZ14) & (fA2 & fB1 & fS3 & fZ15) & (fA3 & fA3 & fZ16) & (fB3 & fS0 & fZ17) & (~fB3 & fS1 & fZ18) & (fA3 & ~fB3 & fS2 & fZ19) & (fA3 & fB3 & fS3 & fZ20) & ~(fZ1 | fZ2 | fZ3) & fY1 & ~(fZ4 | fZ5) & fY2 & ~(fZ6 | fZ7 | fZ8) & fY3 & ~(fZ9 | fZ10) & fY4 & ~(fZ11 | fZ12 | fZ13) & fY5 & ~(fZ14 | fZ15) & fY6 & ~(fZ16 | fZ17 | fZ18) & fY7 & ~(fZ19 | fZ20) & fY8 & (fY1 ^ fY2 & fX1) & (fY3 ^ fY4 & fX2) & (fY5 ^ fY6 & fX3) & (fY7 ^ fY8 & fX4) & ~(fM' & fC') & fW1 & (fM' & fY1 & fW2) & (fM' & fC' & fY2 & fW3) & (fM' & fY3 & fW4) & (fM' & fY4 & fY1 & fW5) & (fM' & fC' & fY4 & fY2 & fW6) & (fM' & fY5 & fW7) & (fM' & fY6 & fY3 & fW8) & (fM' & fY1 & fY4 & fY6 & fW9) & (fM' & fC' & fY2 & fY6 & fY4 & fW10) & ~(fW2 | fW3) & fV1 & ~(fW4 | fW5 | fW6) & fV2 & ~(fW7 | fW8 | fW9 | fW10) & fV3 & (fX1 ^ fW1 & fF0) & (fX2 ^ fV1 & fF1) & (fX3 ^ fV2 & fF2) & (fX4 ^ fV3 & fF3)

3. **Final CNF:** The final CNF combines the good and faulty CNFs, along with the condition $F \not\equiv F^{'}$.

(F0 ^ fF0 & alpha) & (F1 ^ fF1 & beta) & (F2 ^ fF2 & gamma) & (F3 ^ fF3 & delta) & (alpha | beta & kk) & (kk | gamma & kkk) & (kkk | delta & root) (~fB0 & ~fB0') & (~fB1 & ~fB1') & (~fB2 & ~fB2') & (~fB3 & ~fB3') & (~fM & ~fM') & (fA0 & fA0 & fZ1) & (fB0 & fS0 & fZ2) & (~fB0 & fS1 & fZ3) & (~fB0 & fS2 & fA0 & fZ4) & (fB0 & fA0 & fS3 & fZ5) & (fA1 & fA1 & fZ6) & (fB1 & fS0 & fZ7) & (~fB1 & fS1 & fZ8) & (fA1 & ~fB1 & fS2 & fZ9) & (fA1 & fB1 & fS3 & fZ10) & (fA2 & fA2 & fZ11) & (fB2 & fS0 & fZ12) & (~fB2 & fS1 & fZ13) & (fA2 & ~fB2 & fS2 & fZ14) & (fA2 & fB1 & fS3 & fZ15) & (fA3 & fA3 & fZ16) & (fB3 & fS0 & fZ17) & (~fB3 & fS1 & fZ18) & (fA3 & ~fB3 & fS2 & fZ19) & (fA3 & fB3 & fS3 & fZ20) & ~(fZ1 | fZ2 | fZ3) & fY1 & ~(fZ4 | fZ5) & fY2 & ~(fZ6 | fZ7 | fZ8) & fY3 & ~(fZ9 | fZ10) & fY4 & ~(fZ11 | fZ12 | fZ13) & fY5 & ~(fZ14 | fZ15) & fY6 & ~(fZ16 | fZ17 | fZ18) & fY7 & ~(fZ19 | fZ20) & fY8 & (fY1 ^ fY2 & fX1) & (fY3 ^ fY4 & fX2) & (fY5 ^ fY6 & fX3) & (fY7 ^ fY8 & fX4) & ~(fM' & fC') & fW1 & (fM' & fY1 & fW2) & (fM' & fC' & fY2 & fW3) & (fM' & fY3 & fW4) & (fM' & fY4 & fY1 & fW5) & (fM' & fC' & fY4 & fY2 & fW6) & (fM' & fY5 & fW7) & (fM' & fY6 & fY3 & fW8) & (fM' & fY1 & fY4 & fY6 & fW9) & (fM' & fC' & fY2 & fY6 & fY4 & fW10) & ~(fW2 | fW3) & fV1 & ~(fW4 | fW5 | fW6) & fV2 & ~(fW7 | fW8 | fW9 | fW10) & fV3 & (fX1 ^ fW1 & fF0) & (fX2 ^ fV1 & fF1) & (fX3 ^ fV2 & fF2) & (fX4 ^ fV3 & fF3) (~B0 & ~B0') & (~B1 & ~B1') & (~B2 & ~B2') & (~B3 & ~B3') & (~M & ~M') & (A0 & A0 & Z1) & (B0 & S0 & Z2) & (~B0 & S1 & Z3) & (~B0 & S2 & A0 & Z4) & (B0 & A0 & S3 & Z5) & (A1 & A1 & Z6) & (B1 & S0 & Z7) & (~B1 & S1 & Z8) & (A1 & ~B1 & S2 & Z9) & (A1 & B1 & S3 & Z10) & (A2 & A2 & Z11) & (B2 & S0 & Z12) & (~B2 & S1 & Z13) & (A2 & ~B2 & S2 & Z14) & (A2 & B1 & S3 & Z15) & (A3 & A3 & Z16) & (B3 & S0 & Z17) & (~B3 & S1 & Z18) & (A3 & ~B3 & S2 & Z19) & (A3 & B3 & S3 & Z20) & ~(Z1 | Z2 | Z3) & Y1 & ~(Z4 | Z5) & Y2 & ~(Z6 | Z7 | Z8) & Y3 & ~(Z9 | Z10) & Y4 & ~(Z11 | Z12 | Z13) & Y5 & ~(Z14 | Z15) & Y6 & ~(Z16 | Z17 | Z18) & Y7 & ~(Z19 | Z20) & Y8 & (Y1 ^ Y2 & X1) & (Y3 ^ Y4 & X2) & (Y5 ^ Y6 & X3) & (Y7 ^ Y8 & X4) & ~(M' & C') &

W1 & (M' & Y1 & W2) & (M' & C' & Y2 & W3) & (M' & Y3 & W4) & (M' & Y4 & Y1 & W5) & (M' & C' & Y4 & Y2 & W6) & (M' & Y5 & W7) & (M' & Y6 & Y3 & W8) & (M' & Y1 & Y4 & Y6 & W9) & (M' & C' & Y2 & Y6 & Y4 & W10) & ~(W2 | W3) & V1 & ~(W4 | W5 | W6) & V2 & ~(W7 | W8 | W9 | W10) & V3 & (X1 ^ W1 & F0) & (X2 ^ V1 & F1) & (X3 ^ V2 & F2) & (X4 ^ V3 & F3)

&(~F1) &(root)

4. **SAT Solution:** Use a SAT solver to find the input test values that detect the F_1 s-a-0 fault.

5 We gave constraints in the final CNF F1=0 and Output of XOR(root)=1

```
============================[ Problem Statistics ]=============================
|                                                                             |
WARNING! DIMACS header mismatch: wrong number of clauses.
|  Number of variables:           129                                         |
|  Number of clauses:             405                                         |
|  Parse time:                   0.00 s                                       |
|                                                                             |
============================[ Search Statistics ]==============================
| Conflicts |          ORIGINAL         |          LEARNT          | Progress |
|           |    Vars  Clauses Literals |    Limit  Clauses Lit/Cl |          |
===============================================================================
===============================================================================
restarts              : 1
conflicts             : 16             (9496 /sec)
decisions             : 85             (0.00 % random) (50445 /sec)
propagations          : 822            (487834 /sec)
conflict literals     : 39             (4.88 % deleted)
Memory used           : 6.00 MB
CPU time              : 0.001685 s

SATISFIABLE
root@16b24952c6da:/verification_resources/minisat_for_class/test# cat 12.result
SAT
1 -2 3 -4 -5 6 7 -8 9 -10 11 12 13 14 15 -16 17 -18 19 20 21 22 23 -24 -25 26 27 28 -29 30 31 32 -33 -34 35 -36 -37 -38
-39 -40 -41 -42 -43 44 -45 -46 -47 -48 49 -50 51 52 -53 -54 -55 -56 -57 -58 -59 -60 -61 -62 -63 -64 65 -66 67 -68 -69 -7
0 71 -72 -73 74 75 -76 -77 78 79 80 -81 -82 83 84 -85 86 87 -88 -89 90 -91 -92 -93 -94 -95 -96 -97 -98 -99 -100 -101 -10
2 -103 -104 -105 106 -107 -108 -109 -110 -111 -112 -113 -114 -115 -116 -117 -118 119 -120 -121 -122 -123 -124 125 -126 -
127 128 129 0
root@16b24952c6da:/verification_resources/minisat_for_class/test#
```

Conclusions

This assignment demonstrated the use of SAT-solving techniques for fault detection in digital circuits. The methodology provides a systematic approach for generating tests for stuck-at faults, which is crucial for ensuring circuit reliability.

References

1. 74181 ALU Datasheet
2. Madhav P. Desai, Lecture Notes on SAT-based Fault Detection