

Design of Strong Arm Latch Comparator in 180nm

*A capstone project report submitted in partial fulfilment of the requirement for the award of the degree
of*

Bachelor of Engineering
in
Electronics and Communication Engineering

Submitted By
Tanmay Chakravorty (101906107)

Under Supervision of
Dr. Anil Singh (Assistant Professor, ECED)



Department of Electronics and Communication Engineering
THAPAR INSTITUTE OF ENGINEERING & TECHNOLOGY, PATIALA, PUNJAB
May 2023

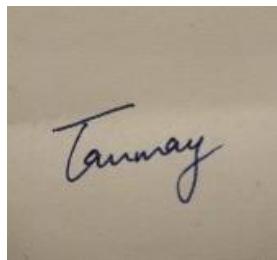
DECLARATION

I hereby declare that the capstone project group report title “Design of Strong Arm Latch Comparator in 180nm “ is authentic record of my own work carried out at “Thapar Institute of Engineering and Technology, Patiala” as a Capstone Project in eighth semester of B.E. (Electronics & Communication Engineering), under the guidance of “**Dr. Anil Singh**”, during January to May 2023.

Date: 16th May,2023

Signature of Students

1. Tanmay Chakravorty



ACKNOWLEDGEMENT

The quest of higher education is a very challenging and demanding process. The process would have been impossible without the encouragement and support of our friends, colleagues and family members. We wish to express sincere gratitude to these individuals.

First and foremost, we would like to express our deep sense of gratitude to our guide Dr. Anil Singh (Assistant Professor), Department of Electronics and Communication Engineering, Thapar Institute of Engineering and Technology, Patiala for their benevolent guidance, suggestions and constant encouragement in undertaking and successfully completing the present study. Their keen interest in the present research work provided us the necessary motivation in carrying out this study. We are also indebted to them for providing creative inspiration in developing ways to analyze the data in this study to arrive at meaningful conclusions.

Last, but not least, we must thank our family members for their patience and cooperation, while we spent extra hours into this study out of their share. And finally, thanks to God who is most beneficent and merciful. This was an incredible opportunity which helped us discover many more unexpected and significant lessons.

Date: 16th May, 2023

Roll No.	Name
101906107	Tanmay Chakravorty

ABSTRACT

This report describes the design and tradeoffs of the Strong Arm Latch Comparator in 180nm process. Different challenges faced while designing a comparator are discussed in this report, mainly the monte carlo simulations which is indeed the most important step needed to be carried out after designing any circuit , it's implementation and most importantly how to carry it out in Mentor Graphics tool step by step is clearly shown in this report.

The circuit is implemented in 180nm CMOS technology with a $\pm 1.8V$ power supply and 2.3 pW of power dissipation. Propogation delays along with their Cumulative distribution function (CDF) and Probabilty Distributive function (PDF) using Mentor Graphics environment to verify the functionality of the circuits is implemented.

TABLE OF CONTENTS

DECLARATION.....	i
ACKNOWLEDGEMENT.....	ii
ABSTRACT	iii
List of Figures	1
Introduction	1
1.1 Project Overview	2
1.1.1 Characterization of the comparator	3
1.2 Motivation	4
1.3 NOVELTY OF WORK	4
CHAPTER 2 – LITERATURE SURVEY	5
2.1 LITERATURE SURVEY.....	5
2.2 PROBLEM DEFINITION AND SCOPE.....	8
2.3 REQUIREMENTS SPECIFICATION	9
2.3.1 INTRODUCTION	9
2.3.1.1 PURPOSE	9
2.3.1.2 INTENDED AUDIENCE AND READING SUGGESTIONS.....	9
2.3.2 OVERALL DESCRIPTION.....	10
2.3.2.1 PRODUCT PERSPECTIVE.....	10
2.4 APPROVED OBJECTIVES.....	11
CHAPTER 3 – FLOW CHART	13
3.1 SYSTEM ARCHITECTURE.....	13
3.2 TOOLS AND TECHNOLOGIES USED.....	16
CHAPTER 4 – PROJECT DESIGN AND DESCRIPTION...	17
4.1 DESCRIPTION	17
4.2 U.G SUBJECTS.....	17
4.3 STANDARDS USED.....	18
4.4 Circuit Description.....	18
CHAPTER 5 – IMPLEMENTATION & EXPERIMENTAL RESULT.....	23
5.1 CIRCUIT STIMULATION.....	24
5.2 Output Waveforms	
5.3 Steps to carry out monte carlo simulations	
5.4 How to use commands	
5.5 Results	
CHAPTER 6 – OUTCOME AND PROSPECTIVE LEARNING.....	39
6.1 SCOPE AND OUTCOMES.....	39
6.2 PROSPECTIVE LEARNINGS.....	39
REFERENCES	40

List of Figures

<i>Figure 1.1</i>	<i>circuit symbol of the comparator</i>
<i>Figure 1.2</i>	<i>Transfer curve of an ideal comparator with infinite gain</i>
<i>Figure 1.3</i>	<i>Transfer curve of the comparator with finite gain</i>
<i>Figure 1.4:</i>	<i>propagation delay definition for a comparator</i>
<i>Figure 1.5</i>	<i>Transfer curve of the comparator including input offset voltage</i>
<i>Figure 2.1:</i>	<i>Pre amplifier based comparator</i>
<i>Figure 2.2</i>	<i>double-tail latch type voltage sense amplifier</i>
<i>Figure 2.3</i>	<i>Dynamic Comparator</i>
<i>Figure 3.1</i>	<i>Flow Chart</i>
<i>Figure 3.1</i>	<i>Flow Chart on how to use the tool</i>
<i>Figure 4.1</i>	<i>Phase 1</i>
<i>Figure 4.2</i>	<i>Phase 1 Capacitor View</i>
<i>Figure 4.3</i>	<i>Phase 2</i>
<i>Figure 4.4</i>	<i>Phase 3</i>
<i>Figure 5.1</i>	<i>Schematic Diagram</i>
<i>Figure 5.2</i>	<i>Propagation delay example</i>
<i>Figure 5.3</i>	<i>TPDUP & TPDDOWN</i>
<i>Figure 5.4</i>	<i>Operation Frequency</i>
<i>Figure 5.5</i>	<i>Power Dissipated</i>
<i>Figure 5.6</i>	<i>Node & voltage parameters</i>
<i>Figure 5.7</i>	<i>Tpd2 & Tpd3</i>
<i>Figure 5.8</i>	<i>Tpd2 & Tpd3 waveforms</i>
<i>Figure 5.9</i>	<i>Probability distribution function of Tpd2 & Tpd3</i>
<i>Figure 5.10</i>	<i>Gauss integral of Tpd2</i>
<i>Figure 5.11</i>	<i>Gauss integral of Tpd3</i>
<i>Figure 5.12</i>	<i>Gaussian Curve</i>

CHAPTER-1 INTRODUCTION

Comparators, as the name suggests compares an analog signal with another analog signal and outputs a Binary signal based on the comparison. The comparator can be thought of as a decision-making circuit. The comparator is widely used in the process of converting analog signals to digital signals. Since comparators are generally used in open loop mode, they can have very high open-loop gain. Comparators are generally classified as open-loop comparators and regenerative comparators. Open-loop comparators are basically operational amplifiers without compensation. Regenerative comparators use positive feedback, similar to sense amplifiers or flip-flops, to accomplish the comparison of the magnitude between two signals. A simple comparator is an op-amp without compensation. Comparators are generally used in open-loop mode and so it is not necessary to compensate the comparator. Since no compensation is needed, it has the largest bandwidth possible which gives a faster response

1.1 PROJECT OVERVIEW

The comparator can be thought of as a decision-making circuit. If the positive input of the comparator is at a greater potential than the negative input, the output of the comparator is at logic 1, whereas if the positive input is at a potential less than the negative input, the output of the comparator is at logic 0. The circuit symbol of the comparator is shown below in figure1.

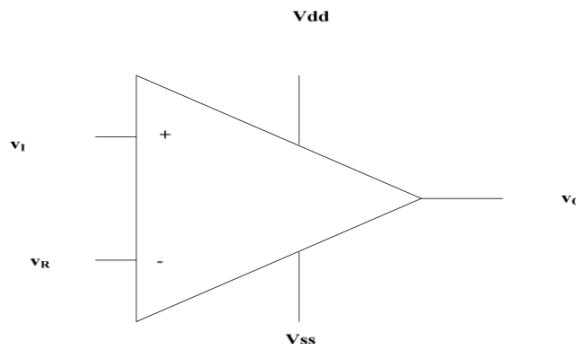


Figure 1.1 circuit symbol of the comparator

Comparators generally are designed to operate more optimally than op-amps in digital applications, in that comparator output voltages will go very close to the power supply voltage rails and their outputs will swing between these rails very fast , that is they have a very high slew rate.

1.1.2 Characterization of the comparator

Gain: The gain of the comparator is the derivative of the dc transfer curve at $v_I \sim v_R$. The transfer curve of an ideal comparator with infinite gain is shown below.

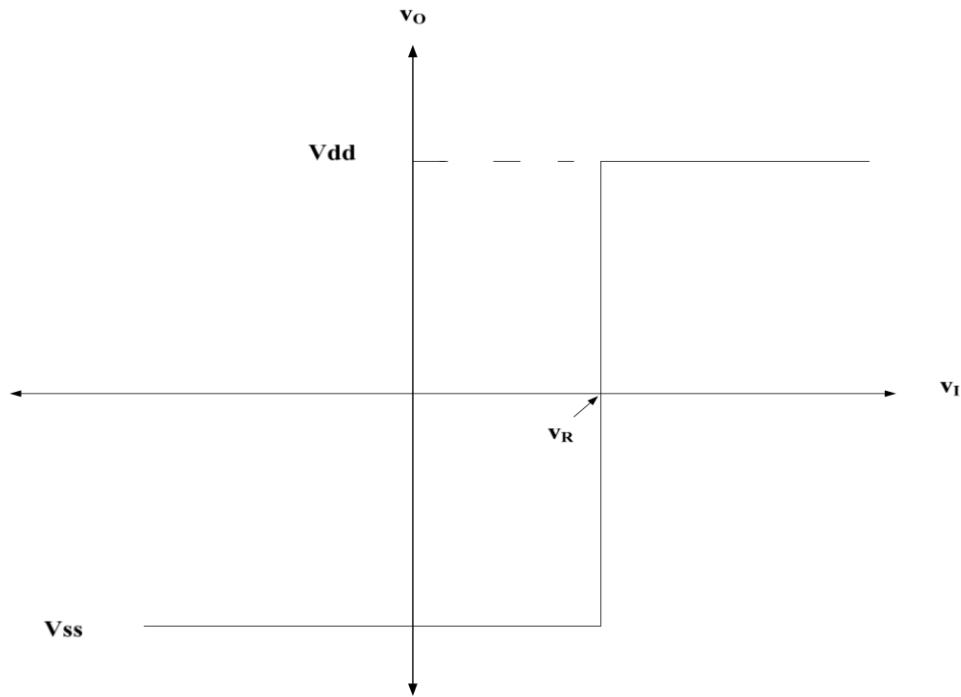


Figure 1.2: Transfer curve of an ideal comparator with infinite gain

The output equations for an ideal comparator can be defined as follows.

$$v_O = V_{dd} \text{ if } v_I > v_R$$

$$= V_{ss} \text{ if } v_I < v_R$$

A comparator with infinite gain is not realizable. Figure 3 shows a more realistic piecewise linear transfer curve of a comparator.

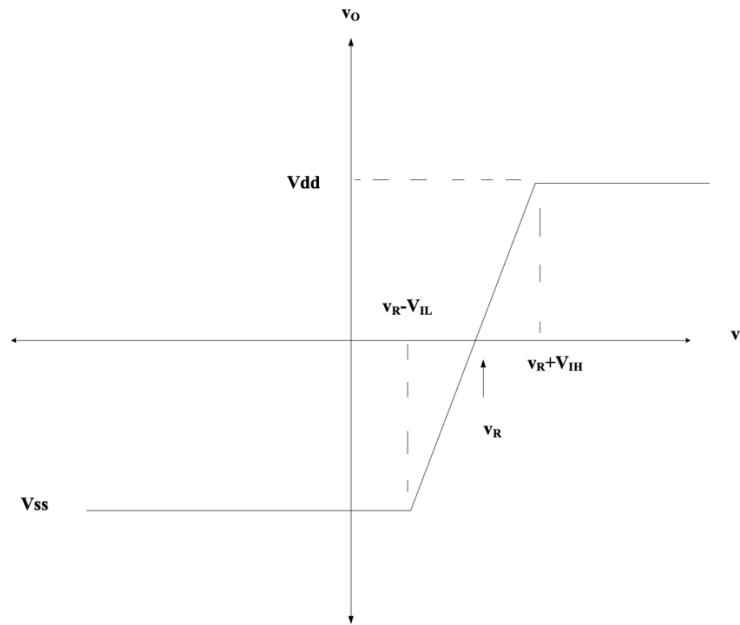


Figure 1.3: Transfer curve of the comparator with finite gain

The output equations can be defined as follows

$$v_O = V_{dd} \text{ if } v_I > v_R + V_{IH}$$

$$= V_{ss} \text{ if } v_I < v_R - V_{IL}$$

$$= A_V v_I \text{ if } V_{IL} < v_I < V_{IH} \text{ Where } A_V \text{ is the non-infinite gain.}$$

Propagation delay: The time difference between the input crossing the reference voltage and the output changing the logic state is defined as the propagation delay. t_{LH} = The delay time between the input crossing v_R i.e., 0V and the output switching the levels i.e., 0V when the output is changing from low to high.

t_{HL} = The delay time between the input crossing zero volts and the output switching the levels i.e., 0V when the output is changing from high to low..

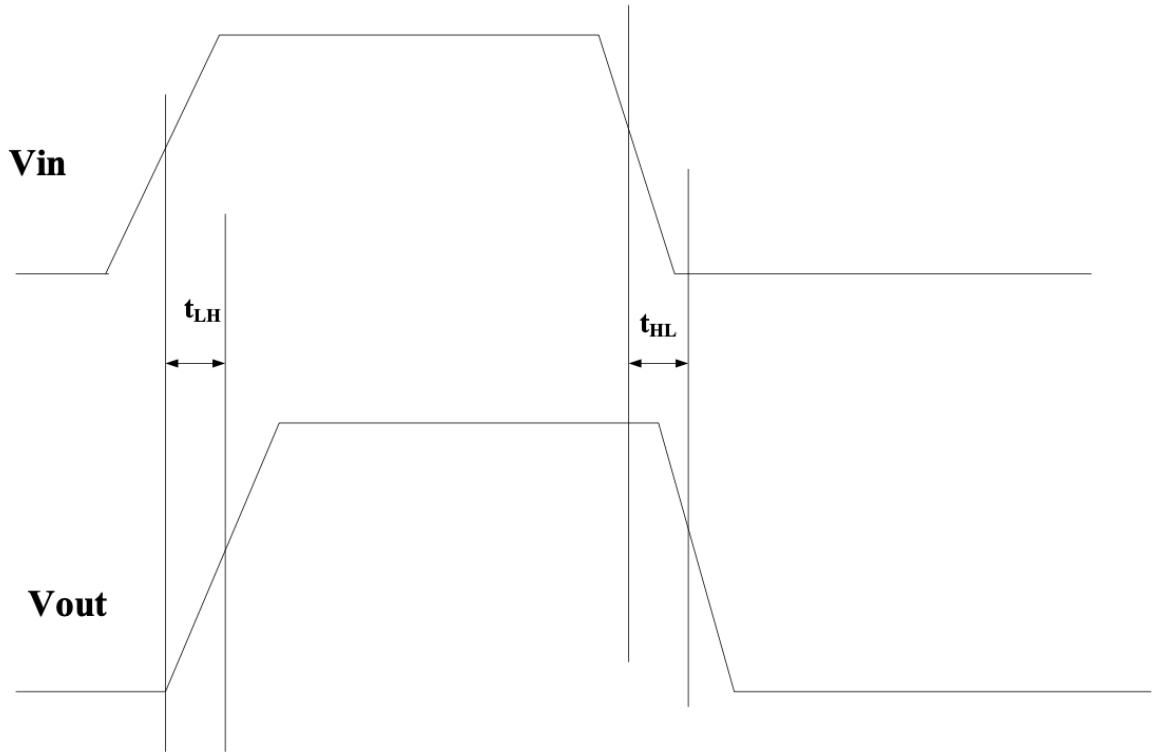


Figure 1.4: propagation delay definition for a comparator

The propagation delay time of the comparators generally varies as a function of the amplitude of the input. A larger input will result in a smaller delay time. Generally, the delay of a comparator is less than that of an op-amp. The delay of the comparator is reduced by cascading several low-gain stages. In other words, the delay of a single high-gain stage is in general longer than the delay of several low-gain stages.

Input offset: Another important characteristic of the practical comparator is the presence of an input offset. The difference between the input voltages $v_I - v_R$, at the instance where output voltage v_O equals zero volts is defined as the input offset voltage. Offset varies from comparator circuit to comparator circuit.

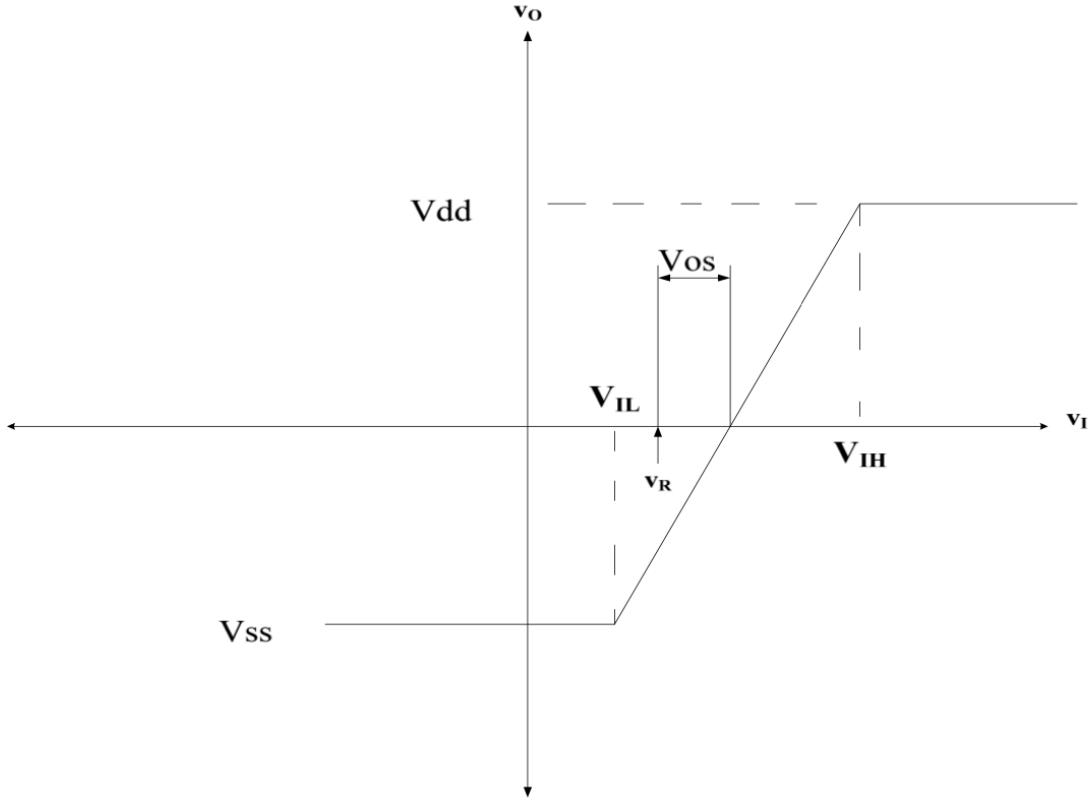


Figure 1.5: Transfer curve of the comparator including input offset voltage

The equation can be defined as follows:

For particular v_R , $V_{os} = v_I - v_R$ such that $v_O = 0 \text{ V}$.

1.2 MOTIVATION

The StrongARM latch topology finds wide usage as a sense amplifier, a comparator, or simply a robust latch with high sensitivity. The term “StrongARM” commemorates the use of this circuit in Digital Equipment Corporation’s StrongARM microprocessor, but the basic structure was originally introduced by Toshiba’s Kobayashi et al. The StrongARM latch has become popular for three reasons:

- 1) it consumes zero static power,
- 2) it directly produces rail-to-rail outputs, and
- 3) its input-referred offset arises from primarily one differential pair.

1.3 NOVELTY OF WORK

This work targets the novel work done on Mentor Graphics tool to figure out how to carry monte carlo simulations, interpreting the data from histograms, calculating propagation delay and making it’s pdf and cdf.

CHAPTER-2 LITERATURE SURVEY

2.1 LITERATURE SURVEY

In this literature review, we will discuss about various type of comparator architecture. The static and dynamic characteristics & advantages and disadvantages of pre-amplifier based comparator are analyzed.

PRE-AMPLIFIER BASED COMPARATOR

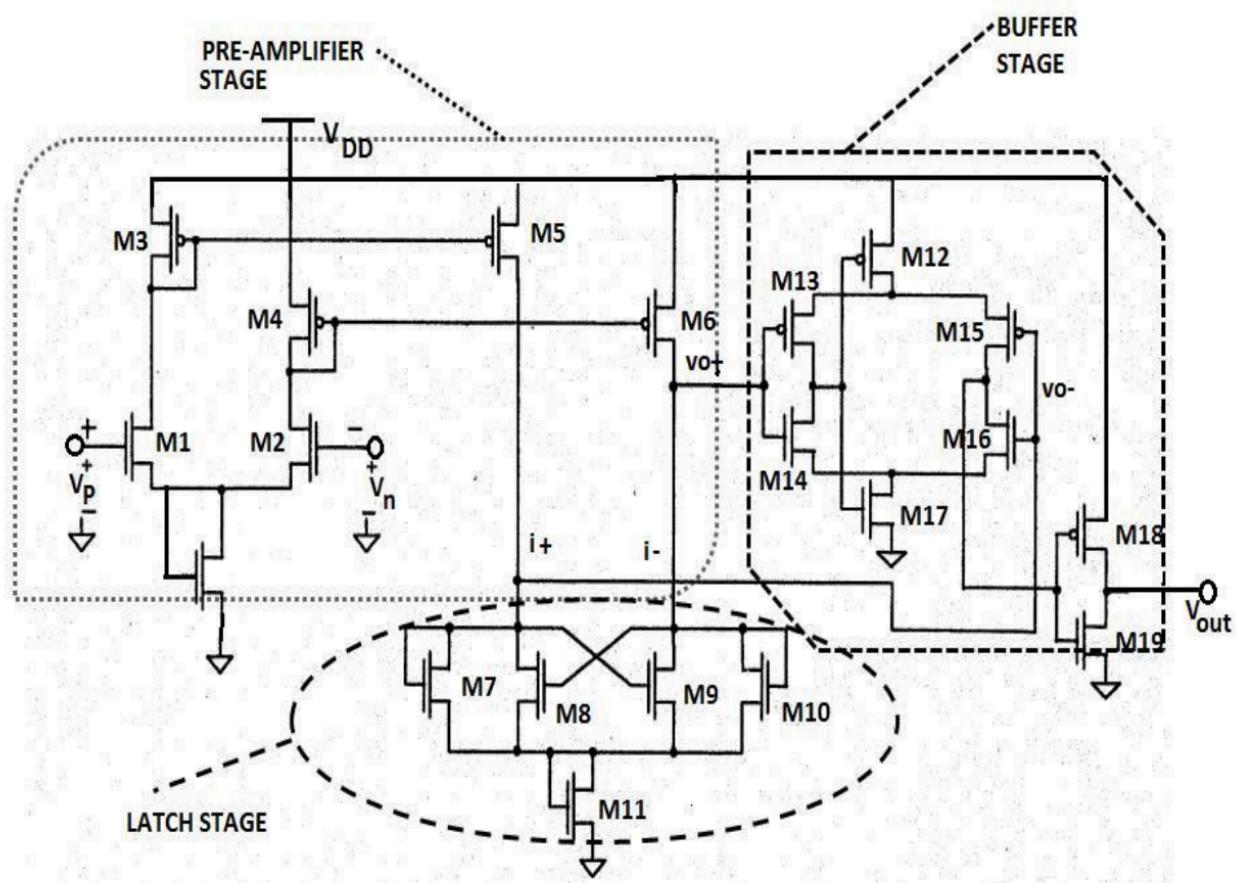


Figure 2.1: Pre amplifier based comparator

The comparator consists of three stages

- i. input preamplifier stage
- ii. latch stage
- iii. output buffer stage

The preamplifier stage consists a differential amplifier with active loads. The preamp stage amplifies the input signal to improve the comparator sensitivity. It increases the minimum input signal with which the comparator can make a decision and isolates the input of the comparator from switching noise (often called kickback noise) coming from the positive feedback stage. It also can reduce the input referred latch offset voltage. The sizes of

M₁ and M₂ are set by taking into consideration the input capacitance and the diff-amp trans-conductance. The transconductance sets the gain of the stage, while the size of M₁ and M₂ mosfets determines the input capacitance of the comparator. Here g_{m1}= g_{m2}.

The positive feedback latch stage is used to determine which of the input signals is larger and amplifies their difference. The output buffer stage consists of a self-biased differential amplifier followed by an inverter which gives the digital output. It converts the output of the latch stage to a full scale digital level output (logic 1 or logic 0). The output buffer stage should accept a differential input signal and not have slew-rate limitations.

DOUBLE-TAIL LATCH TYPE VOLTAGE SENSE AMPLIFIER

Figure 2.2 shows the schematic diagram of the Double-Tail latch type voltage sense amplifier. Double-Tail is derived from the fact that the comparator uses one tail for input stage and another tail for latching stage. It has less stacking and therefore it can operate at lower supply voltages. Large size of the Transistor M₁₄ draws large current at latching stage which is completely independent of common mode voltages at inputs. Also small size of M₁ offers lower supply voltages resulting lower offset.

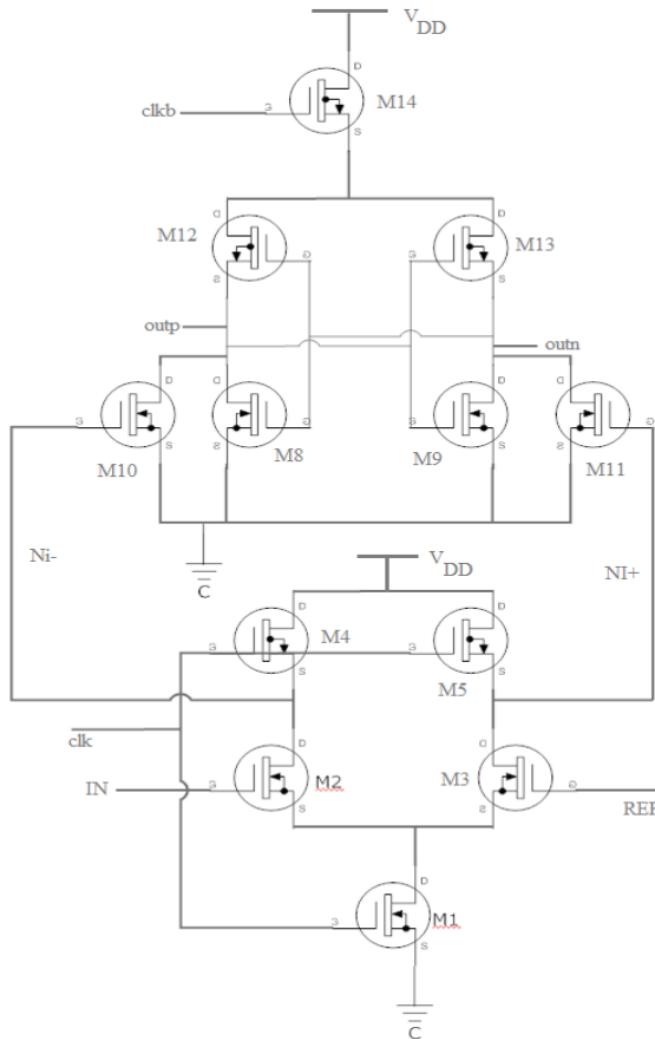


Figure 2.2 : double-tail latch type voltage sense amplifier

OPERATION

During reset phase ($\text{clk}=0\text{V}$), M4 and M5 charges to VDD which in turn charges Ni (regenerative nodes) nodes to VDD. Then M10 and M11 turns on and discharges output nodes to GND. During evaluation phase ($\text{clk}=\text{VDD}$), the transistors M1 and M14 turns ON. So Ni nodes common mode voltage decreases gradually and one input dependent differential mode voltage generates. M10 and M11 pass this differential node voltage to latch stage. The inverters start to regenerate the voltage difference as soon as the common-mode voltage at the Di nodes is no longer high enough for M10 and M11 to clamp the outputs to ground. M10 and M11 also provide additional shielding which reduces kickback noise.

DISADVANTAGES

clk and clkb requires high accuracy timing. The reason is that the latch stage has to regenerate the differential input voltage coming from input stage at very short period of time. Now if we replace the clkb with the inverter whose input is clk signal then clk has to drive heavier load in order to drive largest transistor M14 in a smallest possible delay. Now if clkb leads clk , then comparator will undergo increased power dissipation and if clkb lags clk , it results in increased delay means less speed of operation due to short circuit current path from M14 to M10/M11 through M12/M13.

DYNAMIC COMPARATOR

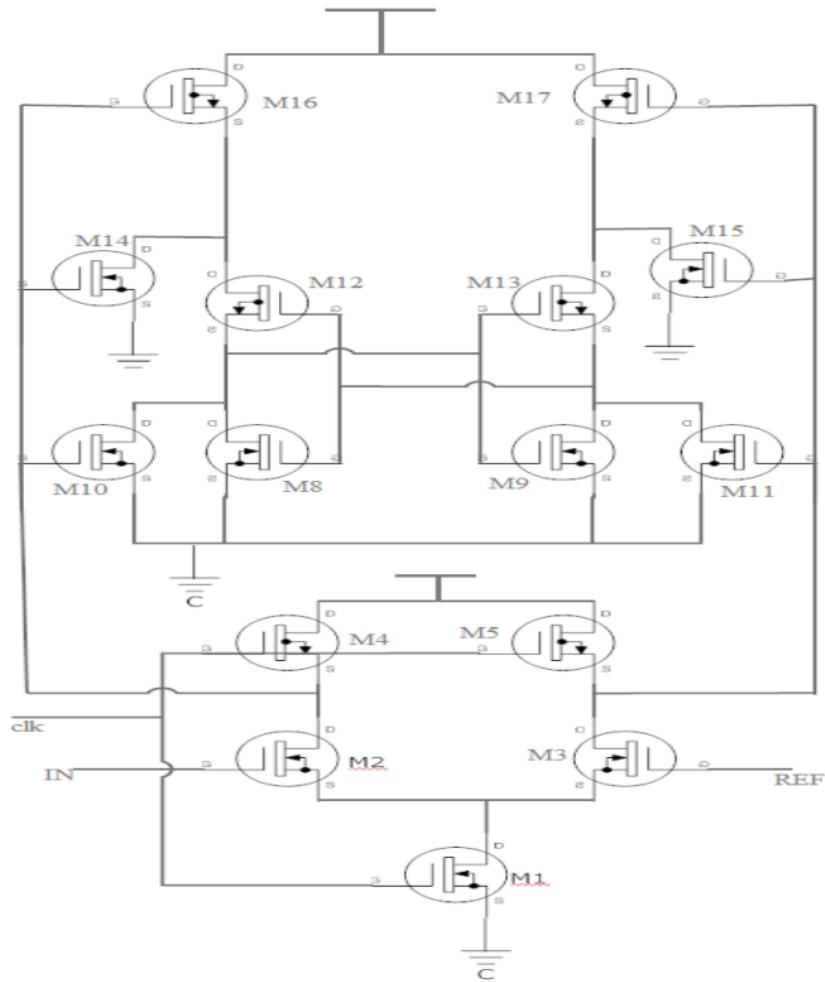


Figure 2.3 : Dynamic Comparator

Figure 2.3 shows the Self-Calibrating Dynamic Comparator. This comparator resolved the high accuracy timing between clk and clkb problem by replacing clkb signal with Ni nodes. But it results in increased delay because the transistor M16 and M17 use Ni node voltages as their input signal. Also due to this, the current drivability of the output node decreases. The input referred latch offset is also reduced in this circuit since the output latch stage takes load from the M10, M11 and M16, M17. Maximum drive current of the output node also decreased to half since the supply voltage VDD has been divided into two transistors.

DOUBLE TAIL DUAL RAIL DYNAMIC LATCHED COMPARATOR

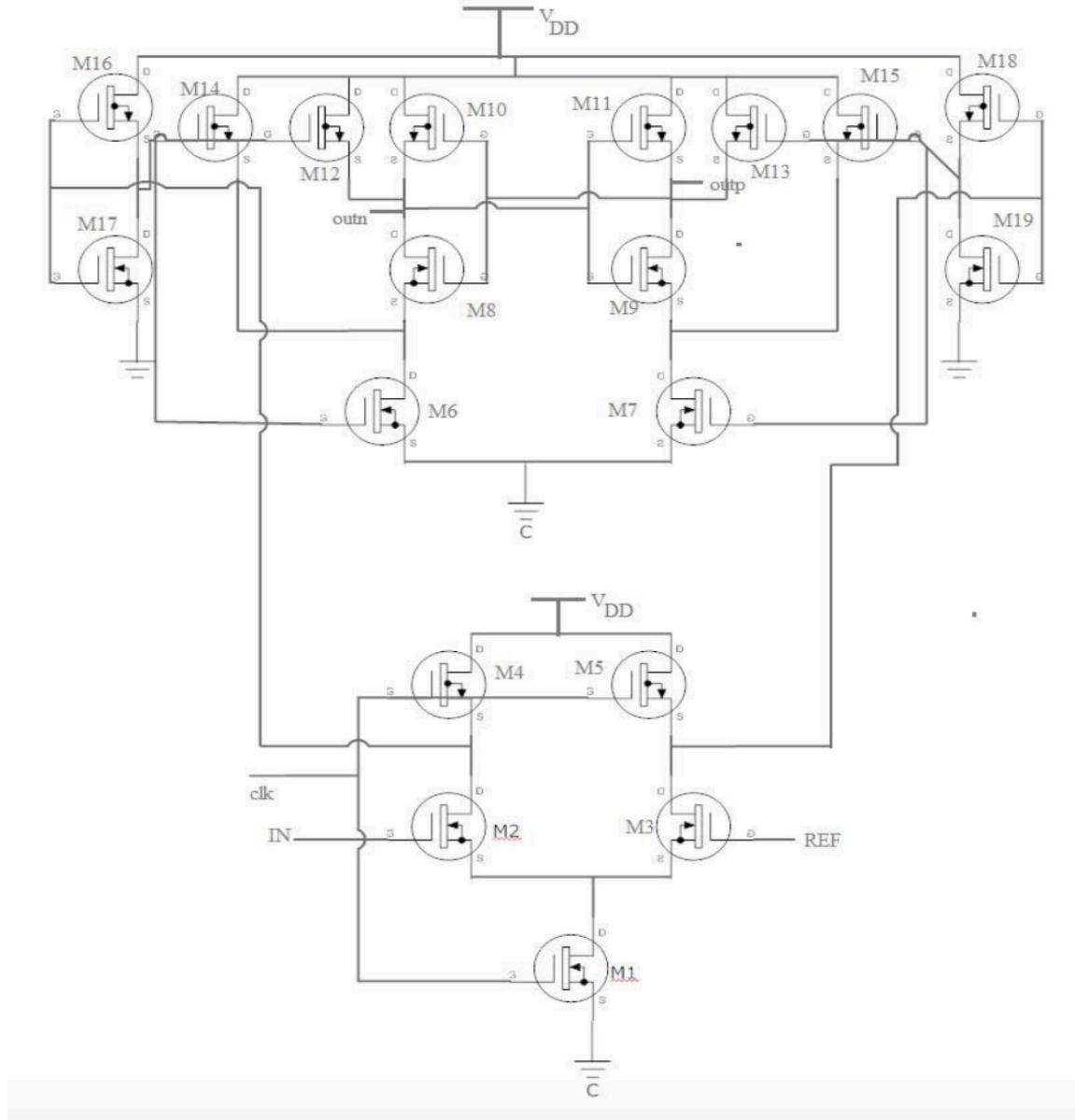


Figure 2.4 Double tail dual rail dynamic latched comparator

Figure 2.4 shows the schematic of the Double-Tail Dual-Rail Dynamic Comparator. This comparator eliminated the weakened regenerating nodes by inserting an inverter between input and output stages. This comparator shows faster operation and lesser power dissipation than the previous comparators.

2.2 PROBLEM DEFINATION & SCOPE

This work targets the novel work done on Mentor Graphics tool to figure out how to carry monte carlo simulations, interpreting the data from histograms, calculating propagation delay and making it's pdf and cdf.

Problems were faced while configuring the mentor graphics tool to carry out monte carlo simulations.

This report now presents step by step guide for mentor graphics tool to do monte carlo, will help students in future to carry out research work and will save their time in configuration of tool.

2.3 REQUIREMENT SPECIFICATIONS

2.3.1 INTRODUCTION

This section explains the necessity of this project to the world.

2.3.1.1 PURPOSE

The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on comparison. A simple comparator is an op-amp without compensation. Comparators are generally used in open-loop mode and so it is not necessary to compensate the comparator. Since no compensation is needed, it has the largest bandwidth possible which gives a faster response.

2.3.1.2 INTENDED AUDIENCE AND READING SUGGESTIONS

The comparator is a commonly used architecture for data acquisition systems that are widely used in medical imaging systems, industrial process control, and optical communication systems. In these applications, we usually need to digitize data generated by a large number of sensors.

2.3.2 OVERALL DESCRIPTION

2.3.2.1 PRODUCT PERSPECTIVE

The comparator is widely used in the process of converting analog signals to digital signals. Since comparators are generally used in open loop mode, they can have very high open-loop gain. Comparators are generally classified as open-loop comparators and regenerative comparators. Open-loop comparators are basically operational amplifiers without compensation.

2.4 APPROVED OBJECTIVES

The following are the objectives while designing the strong arm latch comparator

- . To design the circuit
- . Calculate propagation delay between i/p and o/p
- . Carry out monte carlo simulation
- . designing histogram for mean delay
- . finding out power dissipated by the circuit
- . sweeping the circuit for different i/ps

CHAPTER-3 FLOW CHART

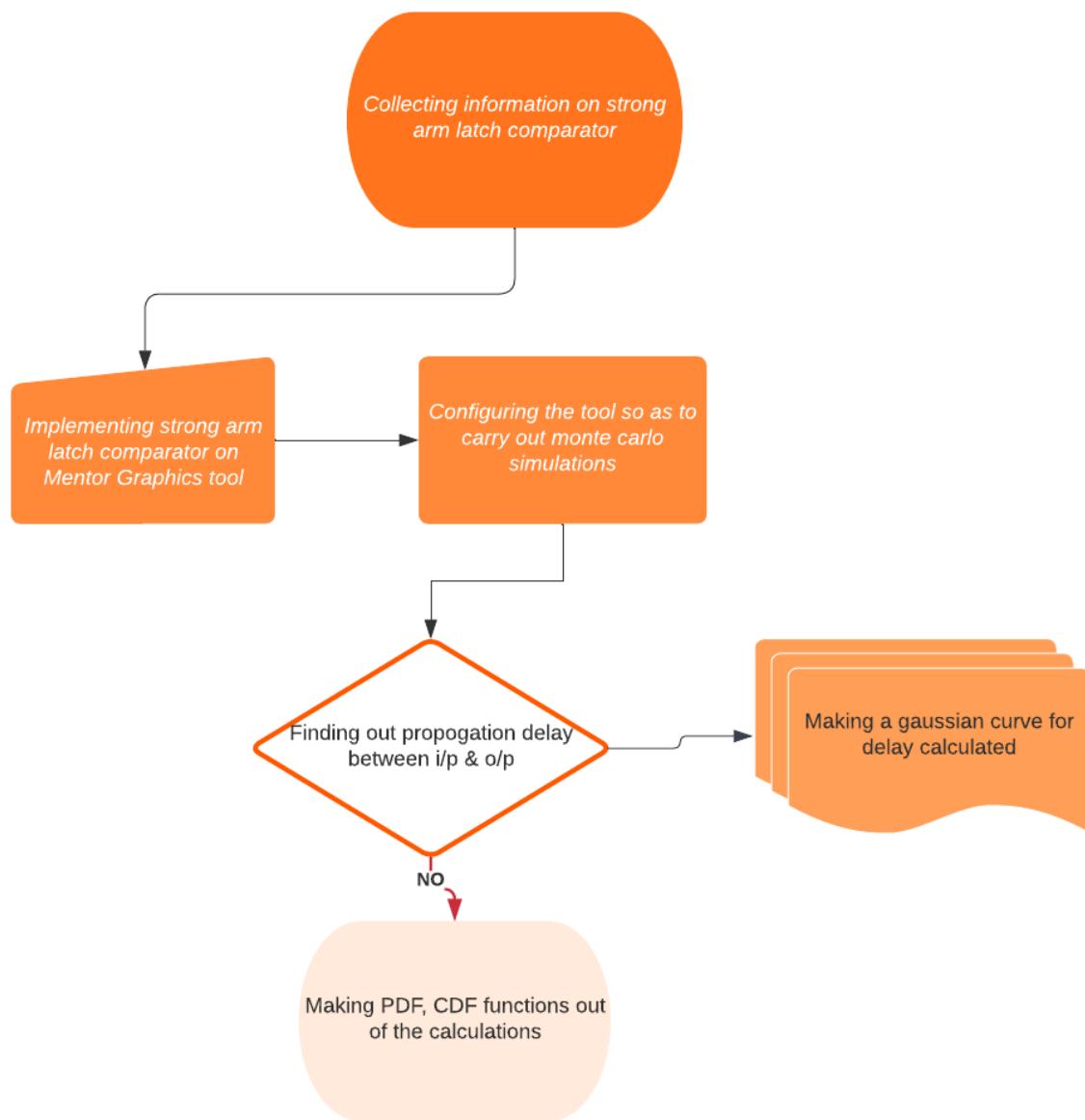


Figure 3.1 Flow Chart

3.1 SYSTEM ARCHITECTURE

Dynamic latched comparators are highly desirable for several applications, including high-speed analog-to-digital converters (SAR-ADCs), memory sense amplifiers (SAs), and data receivers, owing to their high speed, low power consumption, high input impedance, and full-swing output. These days, dynamic comparators are widely being used because of their low-power consumption. Important design parameters for an ADC are fast speed, low offset, low power dissipation, and reduced chip area. A comparator is a fundamental circuit that converts a signal from the analogue domain to the digital domain. It compares two voltage inputs and generates a binary signal indicating which one is greater. The output goes high if the non-inverting (+) input is higher than the inverting (-) input. The output goes low if the inverting input is higher than the non-inverting input. These days, dynamic comparators are widely being used because of their low-power consumption. In conventional dynamic latched comparators, a positive feedback mechanism (regenerative latch) is used which increases the speed of operation by instantly increasing a small-scale voltage difference at the input terminals to a full-scale digital level. In fact, in these comparators, usually there is no constant (current) path from the supply voltage to V_{VSS} , and they are controlled by a clock signal. However, the accuracy of these comparators is restricted by an input-referred latch offset voltage arising from threshold voltage V_{th} , current factor $\beta = \mu C_{ox} \cdot (W/L)$, and parasitic node capacitance and output load capacitance mismatches.

3.2 TOOLS & TECHNOLOGIES USED:

Tanner Tools is a complete flow for Analog, Mixed-Signal, and MEMS IC design including schematic capture, analog simulation, physical layout, verification, synthesis and place & route.

In the Tanner Tools suite, the S-Edit tool is used for schematic capture, and works in conjunction with Siemens EDA simulators and waveform viewers during design simulation.

The flowchart in “[Custom Design Flow](#)” describes the schematic capture and design simulation flow. Click the boxes in the flowchart for descriptions of the corresponding tasks in the documentation.

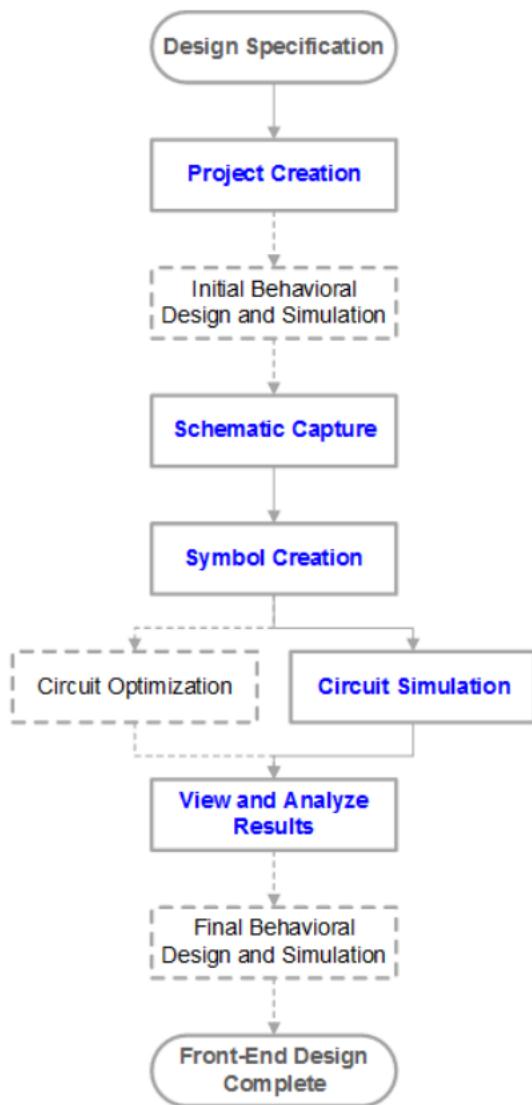


Figure 3.1 Flow Chart on how to use the tool

CHAPTER-4 PROJECT DESIGN AND DESCRIPTION

4.1 DESCRIPTION

Basic Operation: A comparator detects a differential input and produces a logical output based on the input difference's polarity. The "Strong-Arm" comparator is made up of a regenerative latch pair added on top of a input clocked differential pair. As the cross-coupled latch pairs make strong positive feedback, it is able to make decisions quickly. The main advantage of Strong-Arm comparator is

- 1)it consumes zero static power
- 2)it directly produces rail-to rail outputs, and
- 3)its input-referred offset arises from primarily one differential pair, so the offset voltage value is also lower.

4.2 UG SUBJECTS

- 1) MOS Circuit Design (UEC750)
- 2) Analog IC Design (UEC724)
- 3) Linear Integrated Circuits & Applications (UEC512)

4.3 STANDARDS USED

- 1057-2007 - IEEE Standard which describes the testing of waveform recorders. This standard has been used as a guide for many of the techniques described in this standard.
- 746-1984 - IEEE Standard which addresses the testing of analog-to-digital and digital-to-analog converters.
- 1241-2009 - IEEE Standard for analog-to-digital converters is intended to focus specially on terms and definitions as well as test methods for ADCs for wide range of applications.
- 1364-1995 - IEEE Standard was to provide an industry standard based on Verilog Hardware Description Language.

4.4 Circuit Description

Operation of designed comparator

Phase 1: When $CLK=0$, the comparator enters the "Reset" phase, during which S_1 - S_4 switches are activated and P , Q , X , and Y nodes in fig.1. are reset to VDD . The parasitic capacitances of CP , CQ , CX , and CY are therefore charged to VDD during this phase. In Reset mode, M_1 - M_6 and M_7 transistors are cut off

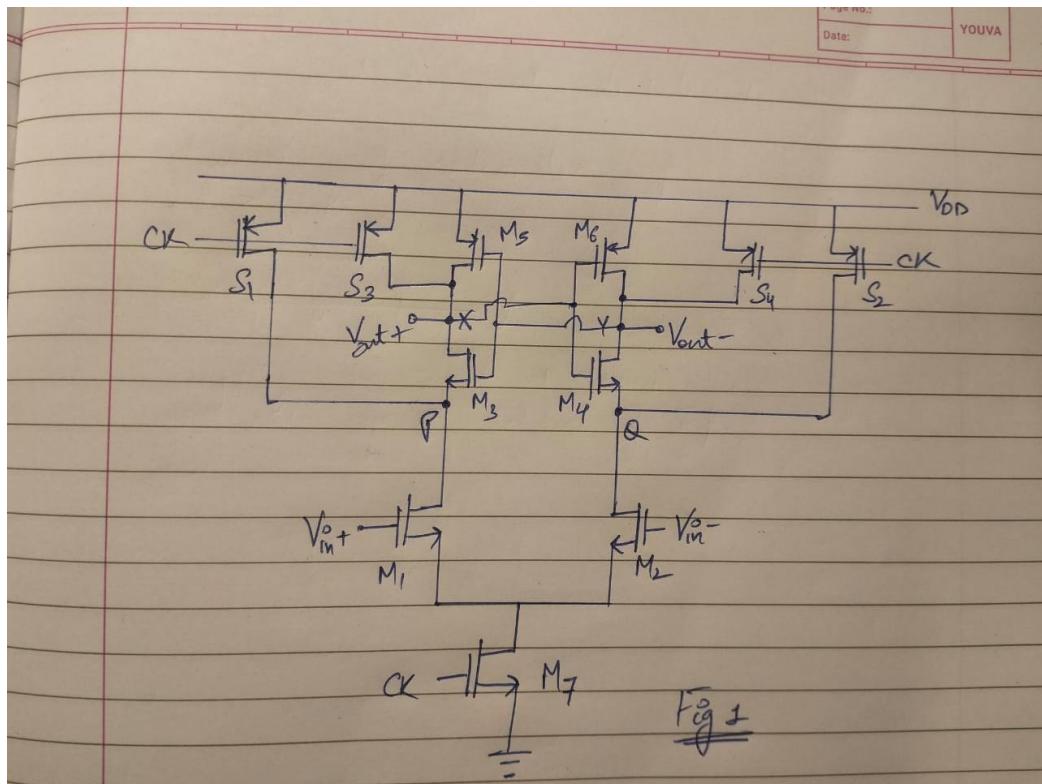


Figure 4.1 Phase 1

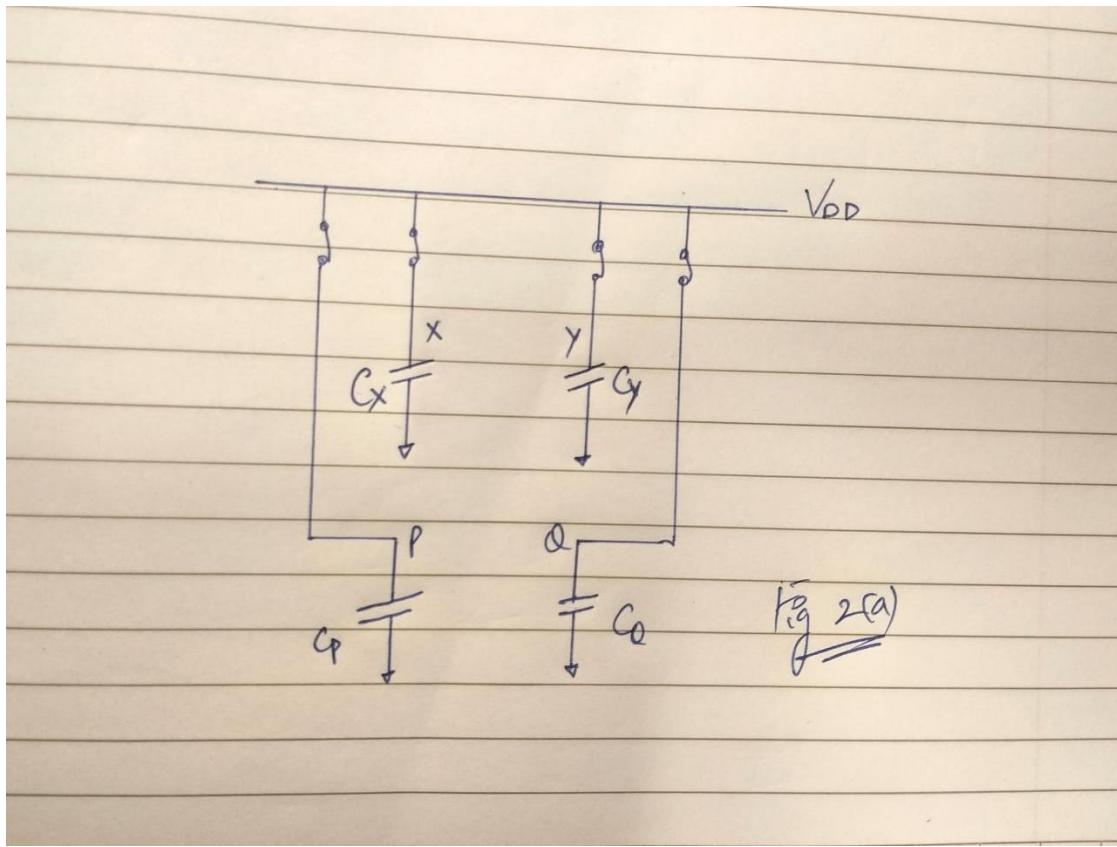


Figure 4.2 Phase 1 Capacitor View

Phase 2: When $CLK = 1$, the comparator enters the Evaluation phase. In this state, switches S1- S4 are deactivated and the tail transistor **M7** is in the triode region. Due to the difference in input voltage between V_{in1} , V_{in2} , the input pair transistors of M1, M2 are in the saturation zone. The pre charged capacitors **CP**, **CQ** are discharging at somewhat different rates. This indicates that the differential input voltage of the comparator is amplified by M1 and M2 and is reflected in the differential drain currents. In other words, this phase might result in voltage gain. This phase is known as the amplification mode, (Fig.2(b)).

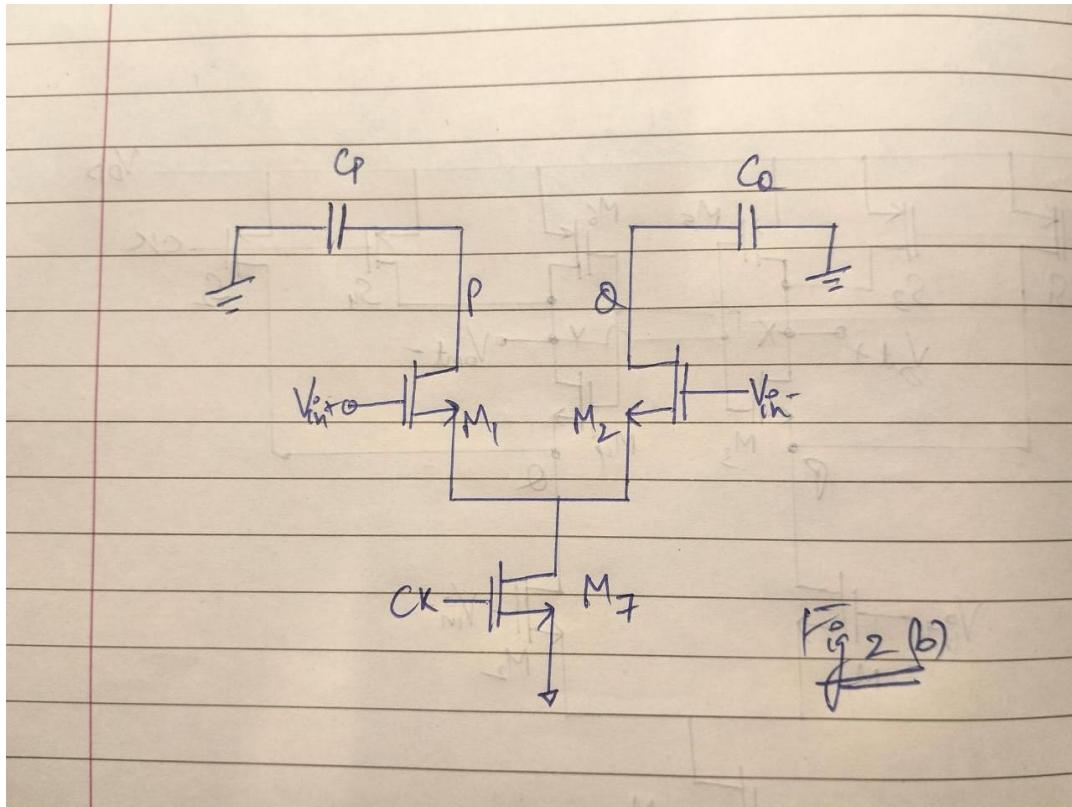


Figure 4.3 Phase 2

Phase 3: When, the voltage on C_p and C_Q fall to $VDD - VTHN$, M_3 and M_4 transistors turn on and C_X and C_Y begin to discharge. When the voltage on C_X , C_Y decreases by a minimum of $VTHP$, cross-coupled latch transistors switch on and regenerate the comparator result; at this point, the lower voltage between X and Y nodes rapidly decreases to 0 and the other node is connected to VDD , (Fig.2(c)). This comparator is completely dynamic and never draws static current due to transistors M_3 and M_4

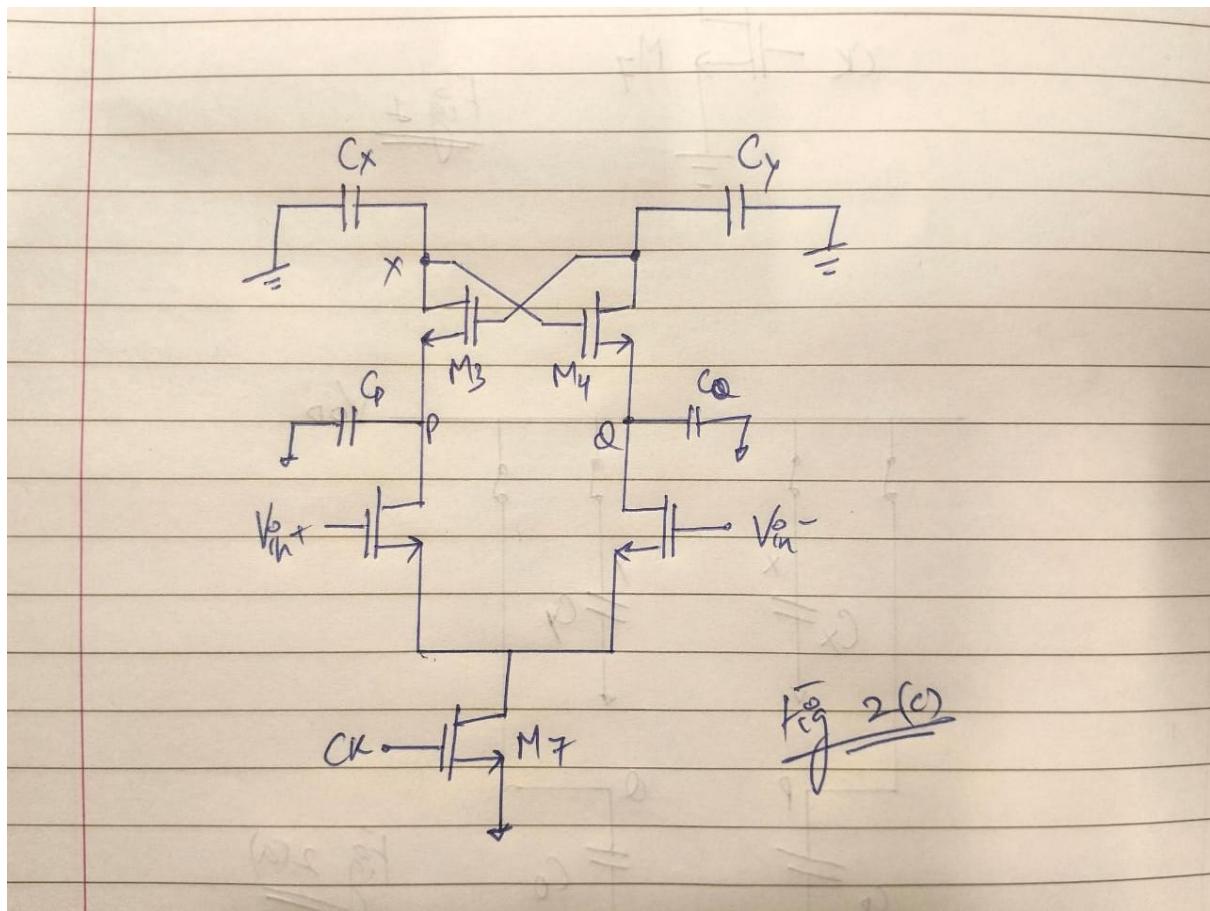


Figure 4.4 Phase 3

Chapter – 5 Implementation & Experimental Results

STRONG ARM LATCH COMPARATOR

5.1 SCHEMATIC DIAGRAM

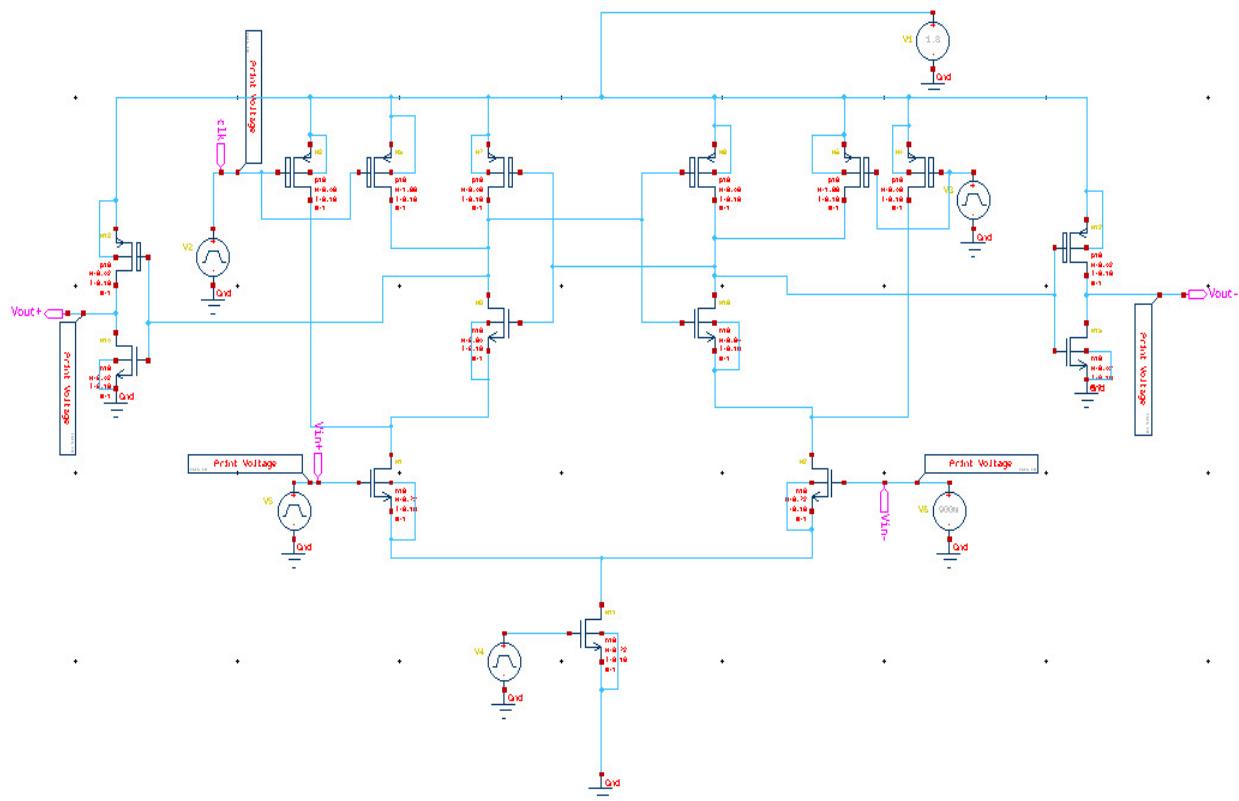
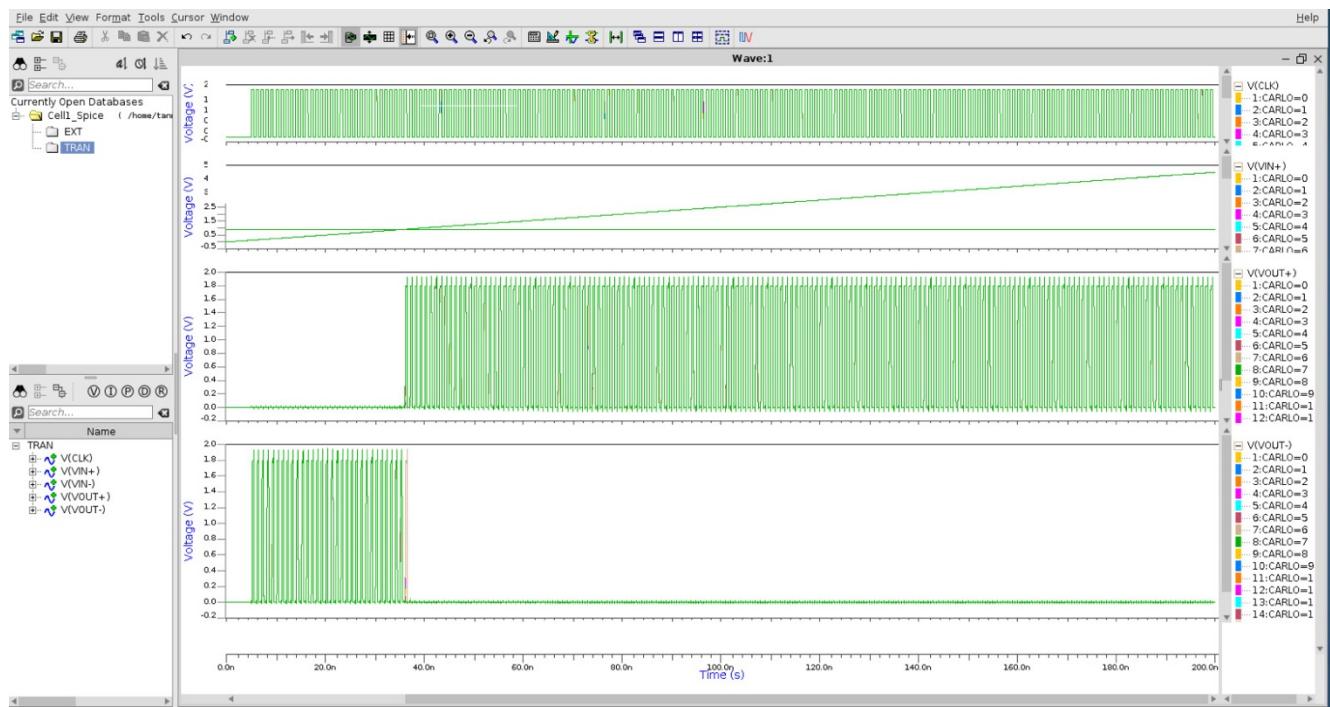
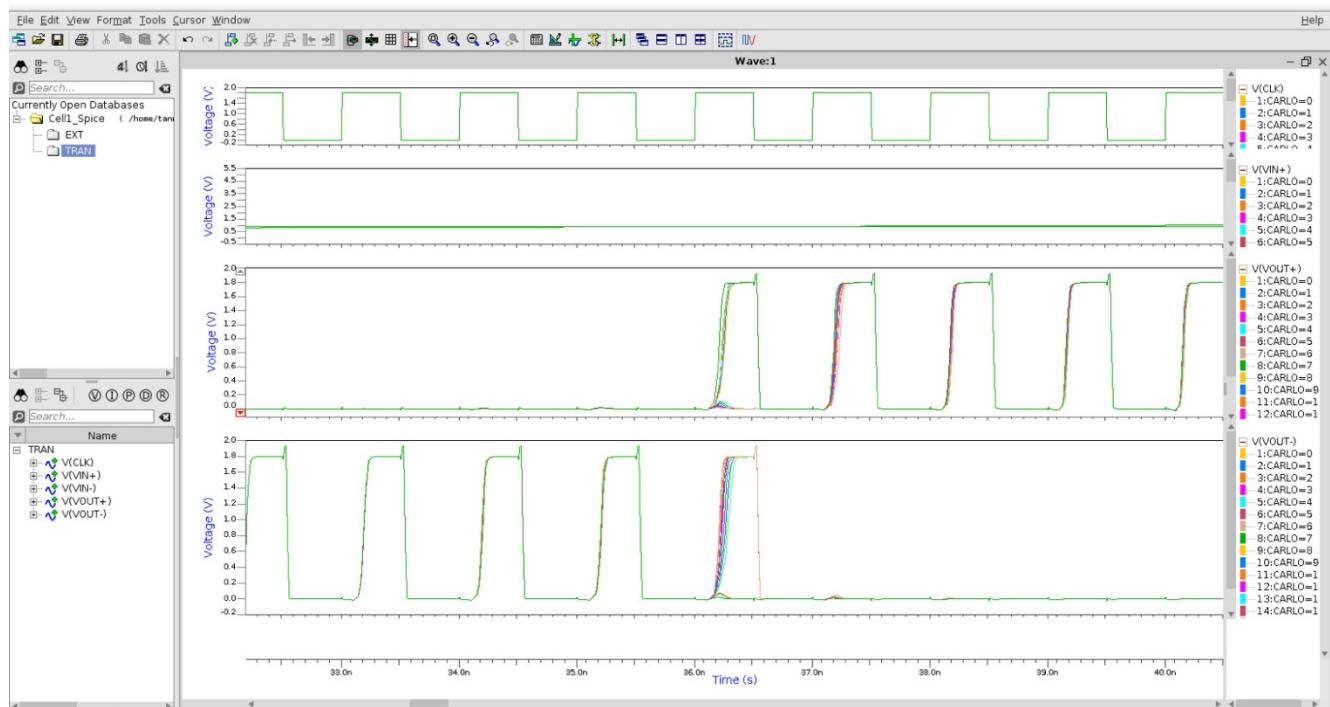


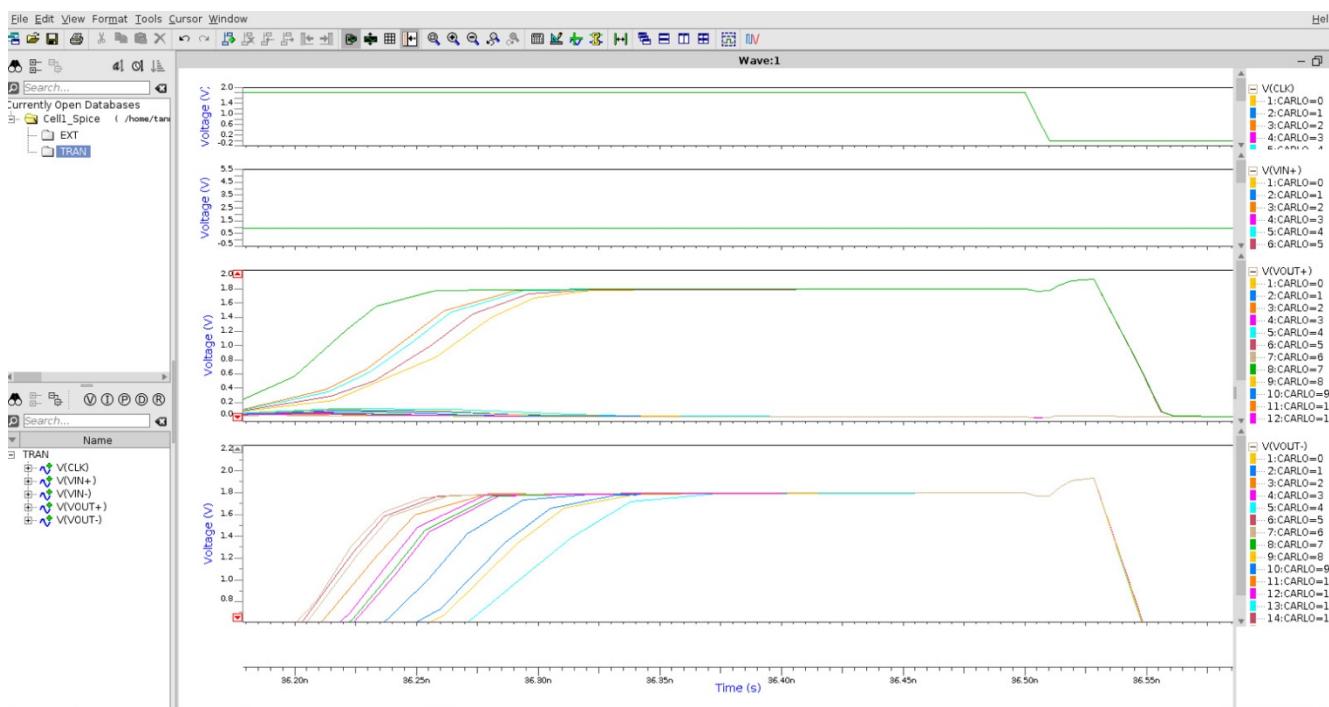
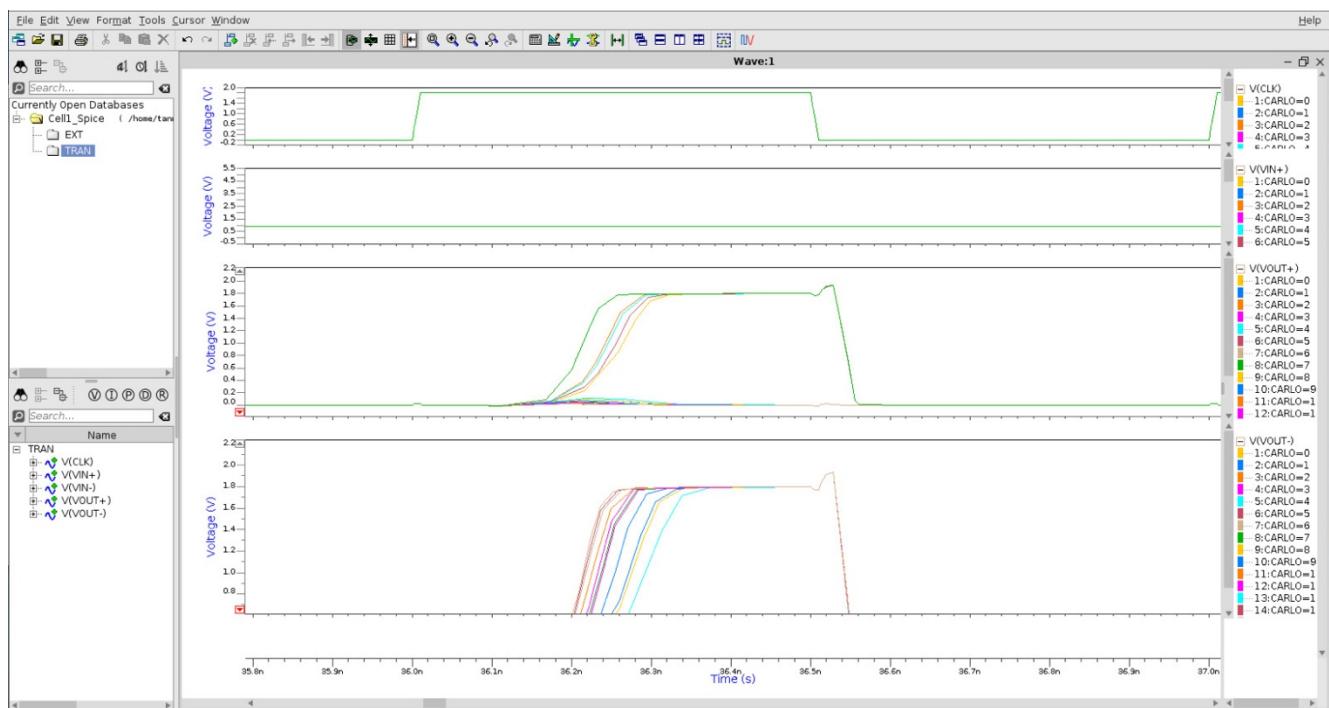
Figure 5.1 Schematic Diagram

5.2 OUTPUT WAVEFORMS :



ZOOMED VIEW :





The above waveforms are monte carlo o/p's of the drawn schematic circuit .

5.3 Steps to carry out the monte carlo simulations

Step 1 : In your desktop go into the folder where your schematic file is saved.

Step 2: Now look out for the cell_spice.sp file, which has the netlist for your circuit

Step 3: Open this file via terminal by giving these commands.

Vim *.sp

Step 4 : .mc command is used to run monte carlo simulations

Given below is the netlist with monte carlo commands and functions called are to calculate the propagation delay of all the monte sims runned.

* SPICE export by: S-Edit 2020.3.3

* Export time: Mon May 1 13:21:49 2023

* Design path: /home/tanmay/strong_arm_latch_comp/lib.defs

* Library: strong_arm_latch_comp

* Cell: Cell1

* Testbench: Spice

* View: schematic

* Export as: top-level cell

* Export mode: hierarchical

* Exclude empty: yes

* Exclude .model: no

* Exclude .hdl: no

* Exclude .end: no
* Expand paths: yes
* Wrap lines: no
* Exclude simulator commands: no
* Exclude global pins: no
* Exclude instance locations: no
* Control property name(s): hspiceD SPICE

*** Simulation Settings - General Section ***

```
.OPTION search="/cad/mentor_tools1/ncsu2/SCL-ts018-CustomPDK-2019-03-29-  
v2_T02/SCL/ts018/Models"
```

```
.LIB 'SCL_ts018_Models.lib' tt
```

```
.LIB 'ts18sl_scl_mat.lib' tt
```

*** Simulation Settings - Options ***

```
.option SCALE = 1e-06
```

** Top Level **

```
.param nwidth=gauss(0.72,0.05,1)
```

```
MM1 N_1 Vin+ N_2 N_2 n18 L=0.18 W=nwidth AD=0.3456 AS=0.3456 PD=2.4 PS=2.4 NRD=0.375  
NRS=0.375 M=1 $ $x=570 $y=590 $w=40 $h=60
```

```
MM2 N_5 Vin- N_2 N_2 n18 L=0.18 W=0.72 AD=0.3456 AS=0.3456 PD=2.4 PS=2.4 NRD=0.375  
NRS=0.375 M=1 $ $x=1130 $y=590 $w=40 $h=60 $m
```

```
MM3 N_1 clk N_6 N_6 p18 L=0.18 W=0.48 AD=0.2304 AS=0.2304 PD=1.92 PS=1.92 NRD=0.5625  
NRS=0.5625 M=1 $ $x=470 $y=920 $w=40 $h=60
```

MM4 N_5 N_7 N_6 N_6 p18 L=0.18 W=0.48 AD=0.2304 AS=0.2304 PD=1.92 PS=1.92 NRD=0.5625
NRS=0.5625 M=1 \$ \$x=1250 \$y=920 \$w=40 \$h=60 \$m

MM5 N_3 clk N_6 N_6 p18 L=0.18 W=1.08 AD=0.5184 AS=0.5184 PD=3.12 PS=3.12 NRD=0.25
NRS=0.25 M=1 \$ \$x=570 \$y=920 \$w=40 \$h=60

MM6 N_4 N_7 N_6 N_6 p18 L=0.18 W=1.08 AD=0.5184 AS=0.5184 PD=3.12 PS=3.12 NRD=0.25
NRS=0.25 M=1 \$ \$x=1170 \$y=920 \$w=40 \$h=60 \$m

MM7 N_3 N_4 N_6 N_6 p18 L=0.18 W=0.48 AD=0.2304 AS=0.2304 PD=1.92 PS=1.92 NRD=0.5625
NRS=0.5625 M=1 \$ \$x=730 \$y=920 \$w=40 \$h=60 \$m

MM8 N_4 N_3 N_6 N_6 p18 L=0.18 W=0.48 AD=0.2304 AS=0.2304 PD=1.92 PS=1.92 NRD=0.5625
NRS=0.5625 M=1 \$ \$x=970 \$y=920 \$w=40 \$h=60

MM9 N_3 N_4 N_1 N_1 n18 L=0.18 W=0.84 AD=0.4032 AS=0.4032 PD=2.64 PS=2.64 NRD=0.321429
NRS=0.321429 M=1 \$ \$x=730 \$y=760 \$w=40 \$h=60 \$m

MM10 N_4 N_3 N_5 N_5 n18 L=0.18 W=0.84 AD=0.4032 AS=0.4032 PD=2.64 PS=2.64 NRD=0.321429
NRS=0.321429 M=1 \$ \$x=970 \$y=760 \$w=40 \$h=60

MM11 N_2 N_8 Gnd Gnd n18 L=0.18 W=0.72 AD=0.3456 AS=0.3456 PD=2.4 PS=2.4 NRD=0.375
NRS=0.375 M=1 \$ \$x=830 \$y=430 \$w=40 \$h=60

MM12 Vout- N_4 N_6 N_6 p18 L=0.18 W=0.42 AD=0.1984 AS=0.1984 PD=1.88 PS=1.88 NRD=1.40909
NRS=1.40909 M=1 \$ \$x=1430 \$y=840 \$w=40 \$h=60

MM13 Vout+ N_3 N_6 N_6 p18 L=0.18 W=0.42 AD=0.1984 AS=0.1984 PD=1.88 PS=1.88 NRD=1.40909
NRS=1.40909 M=1 \$ \$x=270 \$y=830 \$w=40 \$h=60 \$m

MM14 Vout+ N_3 Gnd Gnd n18 L=0.18 W=0.42 AD=0.1984 AS=0.1984 PD=1.88 PS=1.88 NRD=1.40909
NRS=1.40909 M=1 \$ \$x=270 \$y=720 \$w=40 \$h=60 \$m

MM15 Vout- N_4 Gnd Gnd n18 L=0.18 W=0.42 AD=0.1984 AS=0.1984 PD=1.88 PS=1.88 NRD=1.40909
NRS=1.40909 M=1 \$ \$x=1430 \$y=730 \$w=40 \$h=60

VV1 N_6 Gnd DC 1.8 \$ \$x=1260 \$y=1060 \$w=40 \$h=60

VV6 Vin- Gnd DC 900m \$ \$x=1280 \$y=560 \$w=40 \$h=60

VV2 clk Gnd PULSE(0 1.8 5n 10p 10p 490p 1n) \$ \$x=370 \$y=830 \$w=40 \$h=60

VV3 N_7 Gnd PULSE(0 1.8 5n 10p 10p 490p 1n) \$ \$x=1310 \$y=890 \$w=40 \$h=60

```
VV4 N_8 Gnd PULSE(0 1.8 5n 10p 10p 490p 1n) $ $x=730 $y=400 $w=40 $h=60
```

```
VV5 Vin+ Gnd PULSE(0 5 0 200n 0 0 200n) $ $x=470 $y=560 $w=40 $h=60
```

```
.PLOT V(clk) $ $x=415 $y=995 $w=30 $h=150 $r=270
```

```
.PLOT V(Vin+) $ $x=415 $y=605 $w=150 $h=30 $r=180
```

```
.PLOT V(Vin-) $ $x=1315 $y=605 $w=150 $h=30 $r=180 $m
```

```
.PLOT V(Vout+) $ $x=195 $y=695 $w=30 $h=150 $r=90
```

```
.PLOT V(Vout-) $ $x=1525 $y=715 $w=30 $h=150 $r=90
```

*** Simulation Settings - Analysis Section ***

```
.TRAN 0.1ns 200ns 0 0.1ns
```

```
*.STEP MM1 W 0.72 0.74 0.01
```

.mc 15 all

```
.probe tran v(Vout-)
```

```
*.extract tran label=tpd tpdud(v(clk), v(Vout-),vth=0.9, occur=1)
```

```
*.extract tran label=tpd1 tpdud(v(clk), v(Vout-),vth=0.9, occur=2)
```

```
.extract tran label=tpd2 tpduu(v(clk), v(Vout-),vth=0.9, occur=1)
```

```
.extract tran label=tpd3 tpduu(v(clk), v(Vout-),vth=0.9, occur=2)
```

*** Simulation Settings - Additional SPICE Commands ***

.end

5.4 How to use commands?

.EXTRACT COMMAND EXAMPLE :

```
.EXTRACT Extract Waveform Characteristics .EXTRACT [EXTRACT_INFO] [LABEL=NAME]
[FILE=FNAME] [UNIT=UNAME] [VECT] + [CATVECT] $MACRO|FUNCTION [OPTIMIZER_INFO]
[MC_INFO] [TIME=VALUE] +
[INTERP_MODE=LINEAR|QUADRATIC|SAMPHOLD|HISTOGRAM|SPECTRAL]
```

Example: .EXTRACT TRAN label=VMAX MAX(V(out))

.PARAM powersupply=1.2

VDD VDD 0 'powersupply'

.STEP PARAM powersupply list 1.2V 1.3V 1.4V 1.6 2V

.PLOT EXTRACT meas(VMAX) ! this will create a waveform

* showing VMAX(powersupply)

By default, the extraction waveforms, generated by a .EXTRACT combined with a sweep (.TEMP, .STEP, or .ALTER), are saved inside the EXT folder in the main .wdb file, which can be read by EZwave

Using propagation delay commands :

D_WA	DTC	SLEWRATE	TCROSS	TINTEG
TPD	TPDUU	TPDUD	TPDDU	TPDDD
TPERIOD	TRISE	TFALL	VALAT	

TPD Examples

Assume V(IN) crosses VTHIN at 10n 50n and 100n,

assume V(OUT) crosses VTHOUT at 5n 75n and 110n:

TPD(V(IN),V(OUT),OCCUR=1)

would return 65n (75n - 10n), while:

TPD(V(IN),V(OUT),OCCUR=2)

would return 10n (110n - 100n) (second occurrence).

However, TPD(V(IN),V(OUT)) would return 37.5n (average between the first TPD in one direction and the first TPD in the other direction).

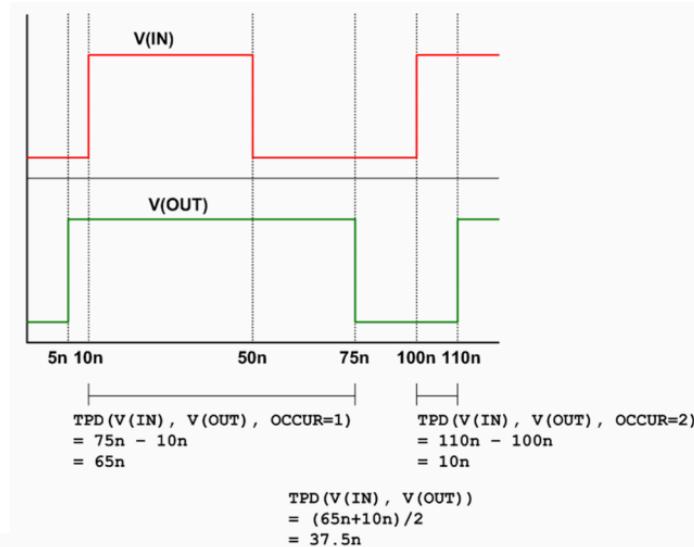


Figure 5.2 Propagation delay example

TPDUU

TPDUU(WAVE1, WAVE2 [, VTH=VAL] [, VTHIN=VAL] [, VTHOUT=VAL] + [, BEFORE=VAL] [, AFTER=VAL] [, OCCUR=VAL])

WAVE1 and WAVE2 are both rising. For example:

```
.extract tran tpduu(v(in),v(out),vth=2.5,occur=3)
```

Eldo returns the propagation delay between v(in) and v(out) for the third occurrence of both waveforms rising above the 2.5 V threshold.

TPDUD

TPDUD((WAVE1, WAVE2 [, VTH=VAL] [, VTHIN=VAL] [, VTHOUT=VAL] + [, BEFORE=VAL] [, AFTER=VAL] [, OCCUR=VAL])

WAVE1 is rising, WAVE2 is falling. For example:

```
.extract tran tpdud(v(in),v(out),vth=2.5,occur=3)
```

Eldo returns the propagation delay between v(in) and v(out) for the third occurrence of waveform v(in) rising above the 2.5 V threshold and waveform v(out) falling below the same threshold.

TPDDU

TPDDU(WAVE1, WAVE2 [, VTH=VAL] [, VTHIN=VAL] [, VTHOUT=VAL] + [, BEFORE=VAL] [, AFTER=VAL] [, OCCUR=VAL])

WAVE1 is falling and WAVE2 is rising. For example:

```
.extract tran tpddu(v(in),v(out),vth=2.5,occur=3)
```

Eldo returns the propagation delay between v(in) and v(out) for the third occurrence of waveform v(in) falling below the 2.5 V threshold and waveform v(out) rising above the same threshold.

TPDDD

```
TPDDD(WAVE1, WAVE2 [, VTH=VAL] [, VTHIN=VAL] [, VTHOUT=VAL] + [, BEFORE=VAL] [, AFTER=VAL] [, OCCUR=VAL])
```

WAVE1 is falling and WAVE2 is falling. For example:

```
.extract tran tpddd(v(in),v(out),vth=2.5,occur=3)
```

Eldo returns the propagation delay between v(in) and v(out) for the third occurrence of both waveforms falling below the 2.5 V threshold.

CROSSING

```
CROSS[ING](WAVE, VALUE[, MIN, MAX[, OCCURENCE]])
```

Returns the x-axis value after the waveform WAVE has crossed OCCURENCE number of times the VALUE in the range MIN to MAX.

The CROSSING() function has two meanings when used inside XYCOND(),

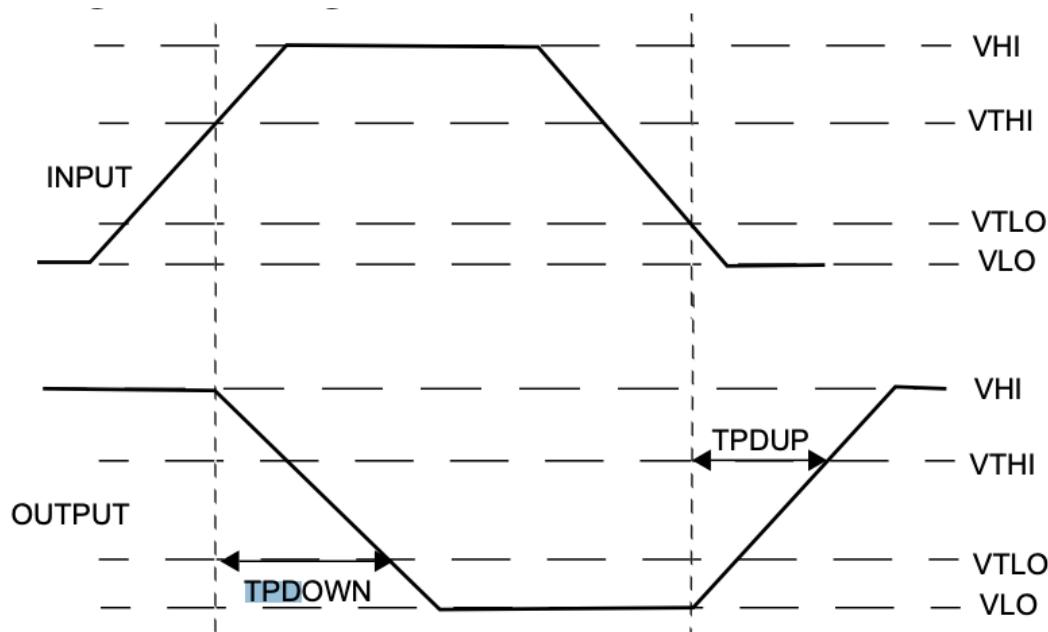


Figure 5.3 TPDUP & TPDDOWN

5.5 RESULTS

1) FREQUENCY AT WHICH ramp is given

Delay	v
ELDO	
FallTime	0
Freq	5M
Period	200n
PulseWidth	0
RiseTime	200n
ROUND	0
spectre	
dc	
delay	
instParameters	val0 val1 period rise fall width
mag	
ORDER	84
OUTPUT	V5 (Vin+ Gnd) vsource type=pulse -
phase	
PRIMITIVE	true
propMapping	val0 VLow val1 VHigh period Period
termOrder	Pos Neg

Figure 5.4 Operation Frequency

2) Power Dissipation in 15th monte carlo runs

```
-----| Simulation Information |-----
***> Memory:
Peak memory usage (MB): 51
Virtual memory usage (MB): 426

***> Design:
Latency: 0.000000%
average number of newton iterations: 2.950511
nb of components: 21
nb of nodes: 13
nb of MOS or BIP calls: 206426
Number of time steps: 7742
-----

Performing 15th Monte Carlo run.

***> 16-May-2023 15:27:26 - DC FOR TRAN completed: TOTAL WALL CLOCK ELAPSED TIME 0s <***
CLK      0.0
N_1     1.8000E+00
N_2     9.7206E-01
N_3     1.8000E+00
N_4     1.8000E+00
N_5     1.8000E+00
N_6     1.8000E+00
N_7     0.0
N_8     0.0
VIN+    0.0
VIN-    9.0000E-01
VOUT+   7.9011E-09
VOUT-   7.9011E-09

TOTAL POWER DISSIPATION: 2.3769E-11 WATTS
```

Figure 5.5 Power Dissipated

3)Node & voltage parameters

```
.....  
          NODE      VOLTAGE      NODE      VOLTAGE      NODE      VOLTAGE  
CLK        0.0       N_1       1.8000E+00  N_2       9.4638E-01  
N_3       1.8000E+00  N_4       1.8000E+00  N_5       1.8000E+00  
N_6       1.8000E+00  N_7       0.0       N_8       0.0  
VIN+      0.0       VIN-      9.0000E-01  VOUT+     7.9011E-09  
VOUT-     7.9011E-09  
  
          VOLTAGE SOURCE CURRENT  
  
NAME      CURRENT      VOLTAGE      POWER  
VV1      -1.3137E-11  1.8000E+00  -2.3646E-11  
VV6       0.0       9.0000E-01   0.0  
VV2       0.0       0.0       0.0  
VV3       0.0       0.0       0.0  
VV4       0.0       0.0       0.0  
VV5       0.0       0.0       0.0  
  
TOTAL POWER DISSIPATION: 2.3646E-11 WATTS  
  
.....  
Eldo NEWTON: VNTOL=1.000000e-06 RELTOL=1.000000e-03  
.....
```

Figure 5.6 Node & voltage parameters

4) Tpd2 & Tpd3 calculated

```
.....  
Simulation progress : 100% (t = 200.0000 N)  
Thread CPU time : 0h 0mn 0s 50 ( 0h 0mn 0s 530)  
CPU Usage : 94% (100%)  
***> 16-May-2023 15:27:26 - TRAN completed: TOTAL WALL CLOCK ELAPSED TIME 0s <***  
  
tpd2 = 1.9176E-10 Sec  
tpd3 = 1.9577E-10 Sec  
  
-----| Simulation Information |-----  
***> Memory:  
Peak memory usage (MB): 51  
Virtual memory usage (MB): 426  
***> Design:  
Latency: 0.000000%  
average number of newton iterations: 2.931435  
nb of components: 21  
nb of nodes: 13  
nb of MOS or BIP calls: 206576  
Number of time steps: 7740  
-----  
***>MESSAGE SUMMARY: 5 warnings, 1 note  
***> 16-May-2023 15:27:30 - GLOBAL CPU TIME 8s 730ms <***  
  
***> 16-May-2023 15:27:30 - GLOBAL WALL CLOCK ELAPSED TIME 19s <***  
-----
```

Figure 5.7 Tpd2 & Tpd3

Tpd2 & Tpd3 waveforms :

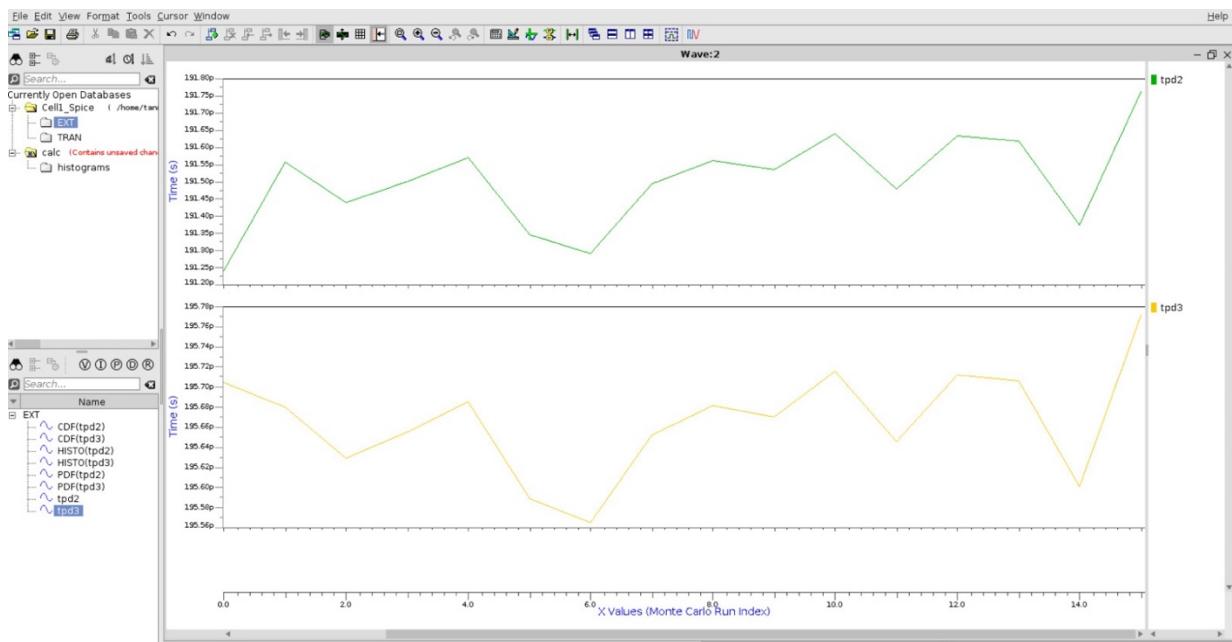


Figure 5.8 Tpd2 & Tpd3 waveforms

PDF function of Tpd2 & Tpd3:

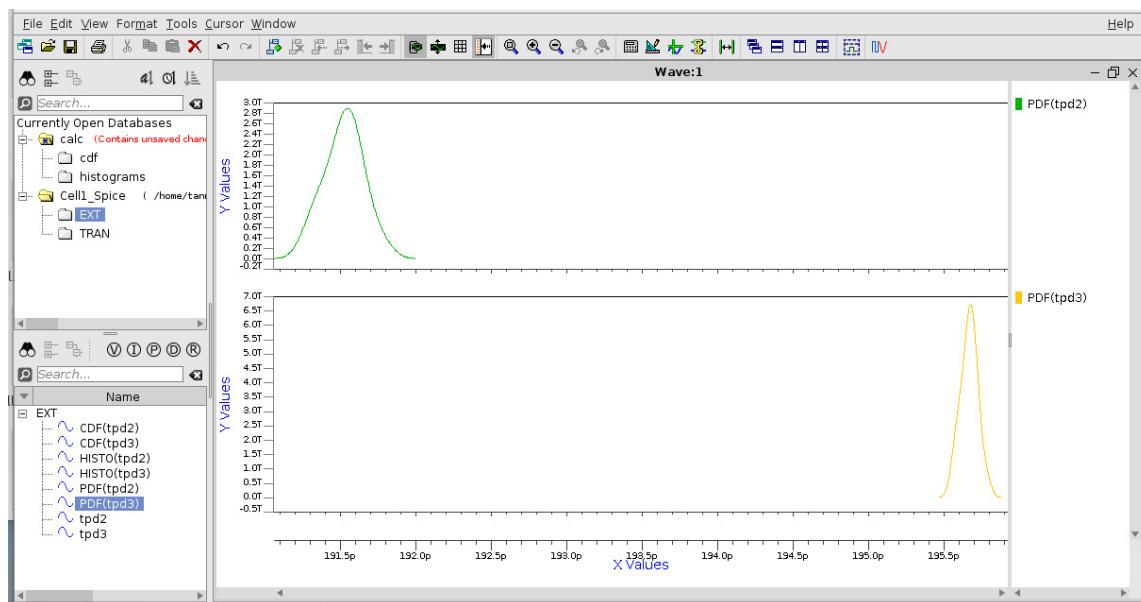


Figure 5.9 Probability distribution function of Tpd2 & Tpd3

Gauss integral of Tpd2:

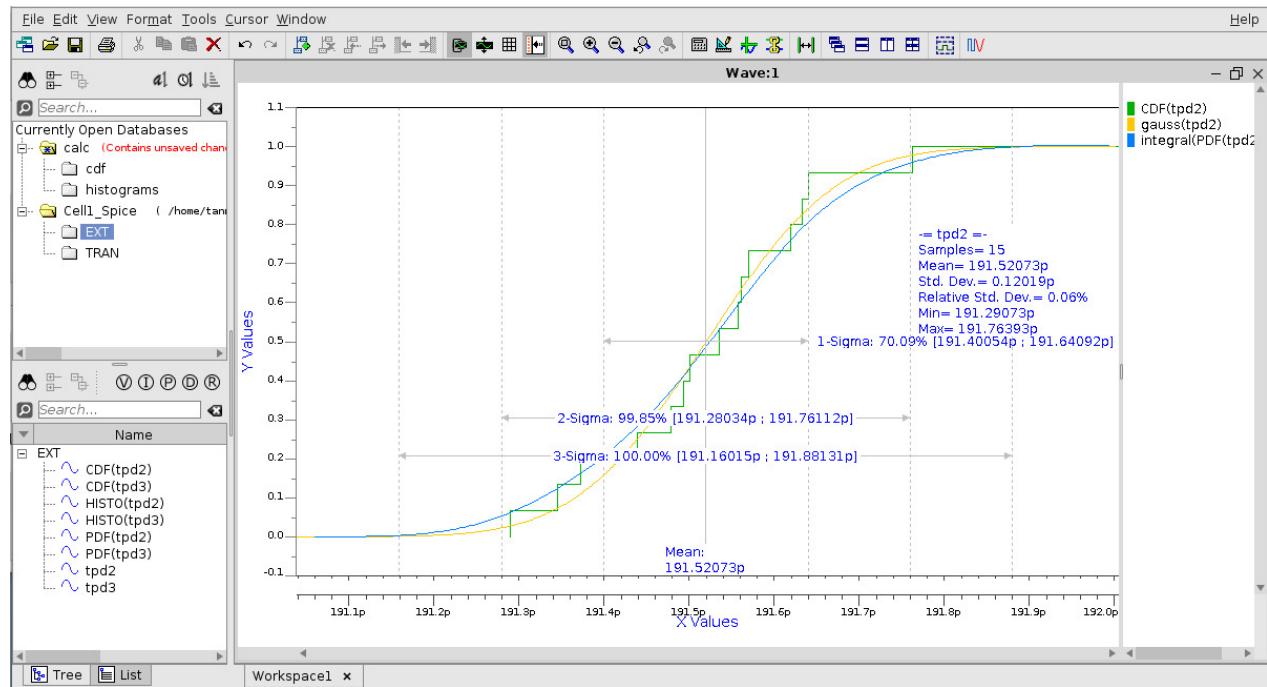


Figure 5.10 Gauss integral of Tpd2

Mean = 191.52073p

Std Dev. = 0.12019p

Gauss integral of Tpd3:

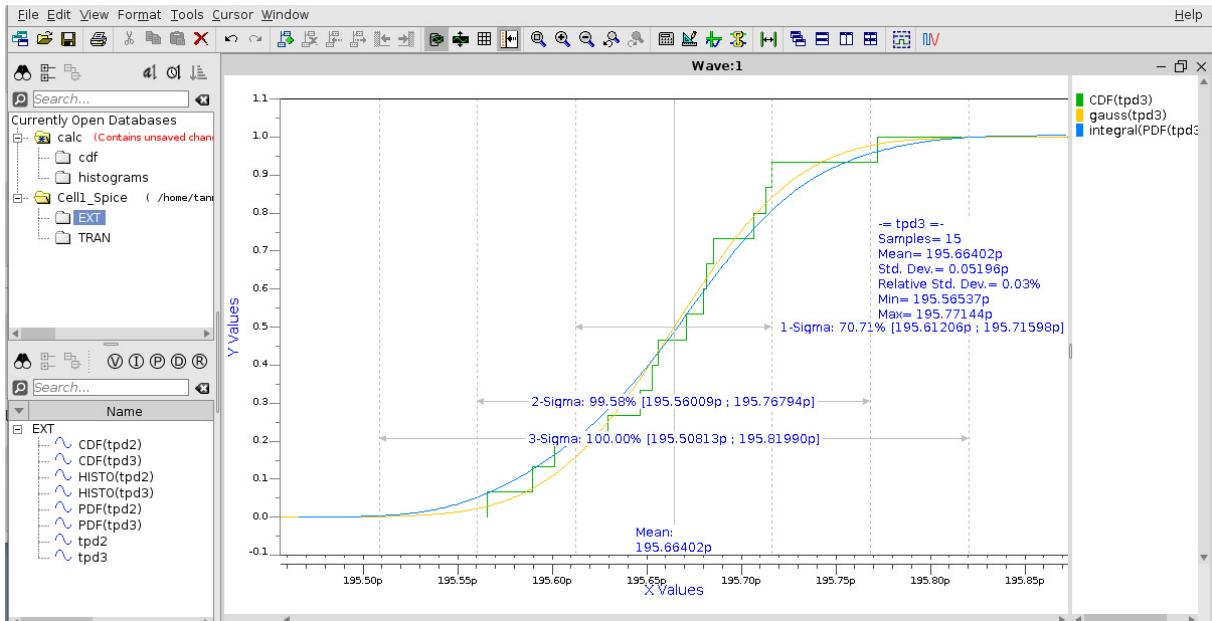


Figure 5.11 Gauss integral of Tpd3

Mean = 195.66402p

Std dev = 0.05196p

Gaussian Curve calculated :

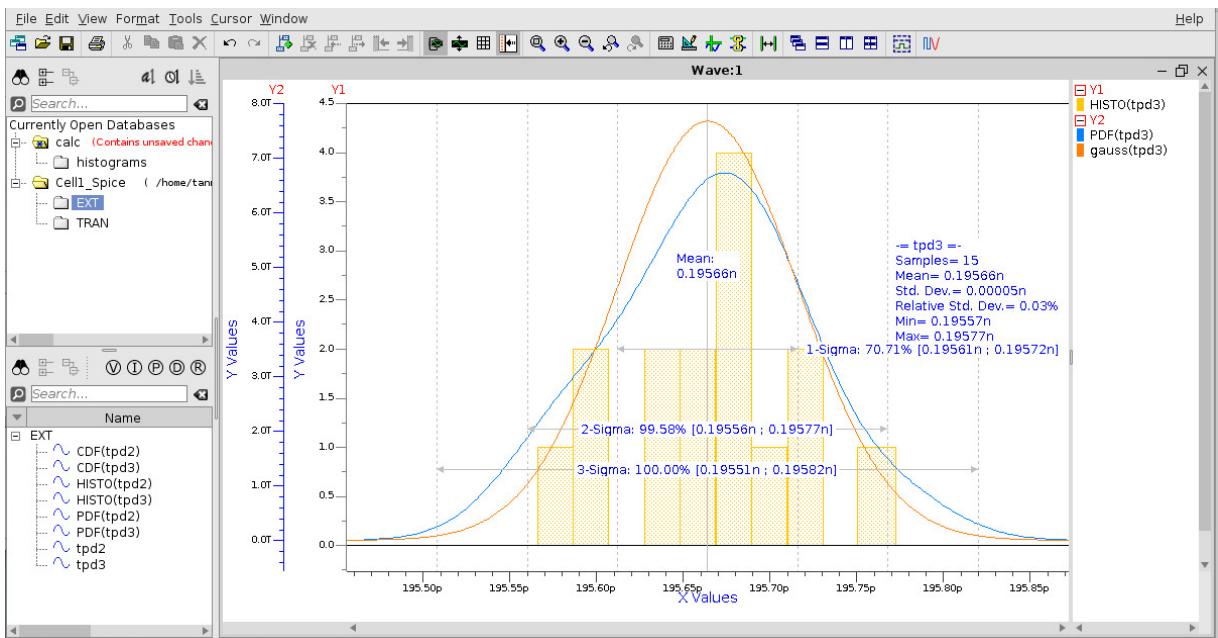


Figure 5.12 Gaussian Curve

Chapter – 6 Prospectives & Outcome Learnings

6.1 SCOPES AND OUTCOMES

In this project, The Strong ARM Latch Comparator was implemented under 180nm SCL technology using Mentor Graphics EDA tool. Monte Carlo simulations were carried out effectively on the tool, propogation delays calculated and verified using tool.

In this project various fields of disciplines were explored:

My project is divided into 6 parts: Understanding of various compartor circuits, Designing strong arm latch comparator, Configuring the tool, Performing monte carlo simulations, Calculating Propogation delays, Finding power dissipated by the circuit

Learning outcomes achieved through this project were:

- Understanding of various electronic tools to implement the precise circuit
- Learning about various models to understand the working of low power battery devices.

6.2 PROSPECTIVE LEARNINGS

- Developed team-working skills and coordination needed for working in such a prestigious and valuable project. Technicalities of this project helped me in brushing up my hardware and software skills and knowledge.
- Research work and detailed analysis of how to use every component is required. Therefore, went through this process of learning, which gave me insights about the technicality of the project.
- Learnt about various components such as comparator, Monte carlo simulations, MOS switches, propogation delays and other components to know whether they were feasible for our project or not.
- Designed a system or process that met the desired needs within realistic constraints such as economical, health, environment, and safety.

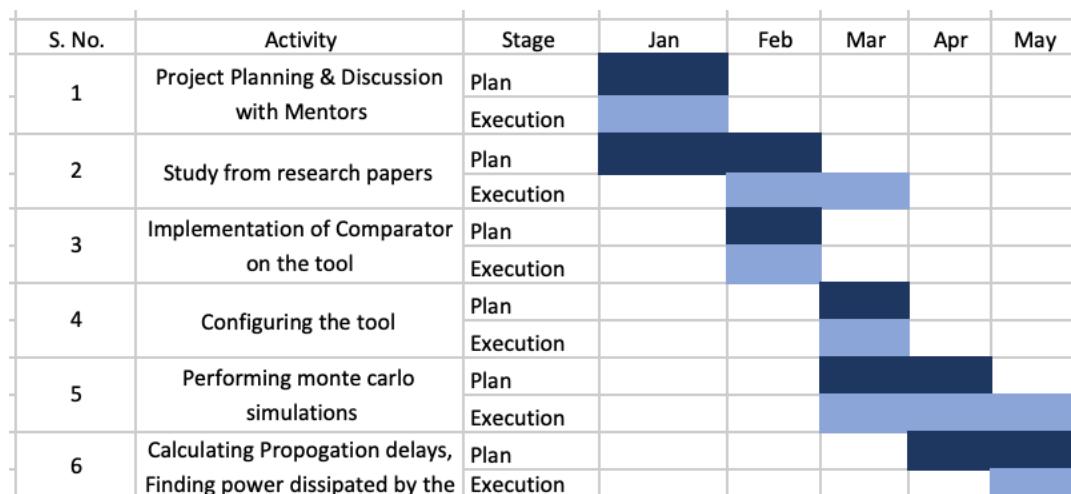
CHAPTER-7 PROJECT TIMELINE

7.1 WORK BREAKDOWN & GANTT CHART

7.1.1 WORK BREAKDOWN

Tanmay Chakravorty	Understanding of various compator circuits, Designing strong arm latch comparator, Configuring the tool, Performing monte carlo simulations, Calculating Propogation delays, Finding power dissipated by the circuit

7.1.2 GANTT CHART



7.2 PROJECT TIMELINE

MONTH	WORK DONE
Jan	Understanding of various comparator circuits
Feb	Designing strong arm latch comparator
Mar	Configuring the Mentor graphics tool for performing Monte Carlo simulations
Apr	Understanding the manual and carrying out experiments on the tool for various commands
May	Performing monte carlo simulations, Calculating Propogation delays, Finding power dissipated by the circuit

NOTE: Which of the following students' outcomes you have achieved till the end of present semester (please answer Yes/No).

For Capstone project the students of undergraduate program in Electronics and Communication Engineering/Electronics and Computer Engineering will have

C. an ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability.

Yes/No

C1. Analyze needs to produce problem definition for electronics and communication systems.	Yes
--------------------------------------------------------------------------------------------	-----

C2. Carries out design process to satisfy project requirement for electronics and communication systems	Yes
---------------------------------------------------------------------------------------------------------	-----

C3. Can work within realistic constraints in realizing systems.	Yes
-----------------------------------------------------------------	-----

C4. Can build prototypes that meet design specifications.	Yes
-----------------------------------------------------------	-----

D. an ability to function on multidisciplinary teams.

D1. Shares responsibility and information schedule with others in team	Yes
------------------------------------------------------------------------	-----

D2. Participates in the development and selection of ideas.	Yes
-------------------------------------------------------------	-----

G. an ability to communicate effectively.

G1. Produce a variety of documents such as laboratory or project reports using appropriate formats and grammar within discipline specific conventions including citations.	Yes
----------------------------------------------------------------------------------------------------------------------------------------------------------------------------	-----

G2. Deliver well organized, logical oral presentation, including good explanations when questioned.	Yes
-----------------------------------------------------------------------------------------------------	-----

H. the broad education necessary to understand the impact of engineering solutions in a global, economic, environmental, and societal context.	
H1. Aware of societal and global changes that engineering innovations may cause.	Yes
H2. Examines economics tradeoffs in engineering systems.	Yes
H3. Evaluates engineering solutions that consider environmental factors.	Yes
I. a recognition of the need for, and an ability to engage in life-long learning.	
I1. Able to use resources to learn new devices and systems, not taught in class.	Yes
I2. Ability to list sources for continuing education opportunities.	Yes
I3. Recognizes the need to accept personal responsibility for learning and of the importance of lifelong learning.	Yes
K. an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.	
K1. Able to operate engineering equipment	Yes
K2. Able to program engineering devices.	Yes
K3. Able to use electronic devices, circuits and systems modeling software for engineering applications	Yes
K4. Able to analyze engineering problems using software tools	Yes

The learning outcomes for project are following. Please rate in accordance to your learnings from capstone.

Course Learning Outcomes	Rate between 1-5 (5: achieved, 1: not achieved)
Developing new/multidisciplinary technical skills.	4
Using professional and technical terminology appropriately.	5
Effectively utilizing and troubleshooting a tool for development of a technical solution.	4
Analyzing or visualizing data to create information.	4
Creating technical report with usage of international standards.	5
Acquiring and evaluating information.	5

REFERENCES

- [1] J. Montanaro, R. Witek, K. Anne, and A. Black, “A 160-MHz 32-b 0.5-W CMOS RISC microprocessor,” IEEE J. SolidState Circuits, vol. 31, pp. 1703–1714, Nov. 1996.
- [2] T. Kobayashi, K. Nogami, T. Shirotori, and Y. Fujimoto, “A current-mode latch sense amplifier and a static power saving input buffer for low-power architecture,” in Proc. VLSI Circuits Symp. Dig. Technical Papers, June 1992, pp. 28–29.
- [3] Y. T. Wang and B. Razavi, “An 8-bit 150-MHz CMOS A/D converter,” IEEE J. Solid-State Circuits, vol. 35, pp. 308–317, Mar. 2000.
- [4] P. Nuzzo, F. De Bernardinis, P. Terreni, and G. Van der Plas, “Noise analysis of regenerative comparators for reconfigurable ADC architectures,” IEEE Trans. Circuits Syst. I, vol. 55, pp. 1441–1454, July 2008.
- [5] M. J. E. Lee, W. J. dally, and P. Chiang, “Low-power area-efficient high-speed I/O circuit techniques,” IEEE J. Solid-State Circuits, vol. 35, pp. 1591–1599, Nov. 2000.
- [6] M. Yoshiyoka, K. Ishikawa, T. Takayama, and S. Tsukomato, “A 10-b 50-MS/s 820- uW SAR ADC with on-chip digital calibration,” IEEE Trans. Biomed. Circuits Syst., vol. 4, pp. 411–418, Dec. 2010.
- [7] S.W. Chiang and B. Razavi, “A 10-bit 800-MHz 19-mW CMOS ADC,” IEEE J. Solid-State Circuits, vol. 49, pp. 935–949, Apr. 2014.
- [8] T. Sepke, P. Holloway, G. Sodini, and H. S. Lee, “Noise analysis of comparator-based circuits,” IEEE Trans. Circuits Syst. I, vol. 56, pp. 541–553, Mar. 2009.
- [9] R. J. Baker, CMOS Circuit Design, Layout, and Simulation. Wiley: Hoboken, NJ: Wiley, 2010