HFE TESTER

Group 12

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Date: 19/04/2021

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User Requirements & Technical Specifications

Design a microprocessor-based transistor h_{FE} tester. The system has to display the h_{FE} value of NPN transistors.

- The base of the TUT is energized with a current I from a device DI. The current I can be controlled by DC supply voltage V.

$$\mathbf{I = V * 10^{-6} A}$$

- Current range is 1-10µA.
- Resolution required is 1µA.
- Emitter of the transistor is grounded.
- Collector is connected to a 1K resistor whose other end is connected to the +5V supply.
- Voltage drop across a 1K resistor is measured and this is related to the h FE by the following relation:

$$\mathbf{h_{FE} * I * 1000 = Voltage\ Drop}$$

- If the h_{FE} value is less than 20, an alarm should be sounded.

Assumptions & Justifications

JUSTIFICATION

1. Code based on design is different from the EMU design, due to implementation support in Proteus. The codebasedondesign.asm file has the code we wish to implement but were not able to as AD7819 was not available on proteus and display had to be changed.
2. NPN transistor always operates in the active region.
3. As the hFE values to be displayed lie between 1 and 500 and resolution is 1, only three seven segment displays are used.
4. The conversion time (for busy to become low) of AD7918 is very low hence we are polling.

NOTE:

To Increase maximum H_{FE} value handled to 500, the given process is used to calculate the value:

Notations:

I	:	Base Current	V	:	Voltage given to DI
VD	:	Voltage Drop	ip	:	Input Voltage

op : Output Voltage

<u>Given:</u>

$I = V * 10^{-6}$

$h_{FE} * I * 1000 = VD$

$h_{FE} = VD/V * 1000$ (1)

$VD = ip * \frac{5}{256}$ (2)

$V = op * \frac{10}{256}$ (3)

Substituting (2) and (3) in (1),

$h_{FE} = \frac{ip}{op} * 500$

For calculation purposes:

$h_{FE} = ((ip * 250) / op) * 2$

ASSUMPTIONS

1. The system is designed for integral values of hFE.
2. The maximum value of hFE is not to exceed 500.

Components used with justification wherever required

- 8086 - 1
- 8284 – to generate clock for 8086
- 2N2369 – NPN Switching Transistor (TUT) (Manual Attached)
- ADC 7819 - 1 Analog inputs with voltage varying from 0 – 5 V with 8-bit resolution (Manual Attached).
- 2N3906 - (3 Nos.) PNP Bipolar Transistor to control simultaneous operation of 7-segment displays (Manual Attached)
- AD558 – 1 Nos. 8-Bit DAC. 0-10V output range. Directly connected to DI which Is connected to base of transistor. (Manual Attached)
- 1K Ohm Resistor - connected to the collector terminal of the TUT to channelize the collector current to measure h_{FE}.
- VCCS - Linear voltage controlled current source (the device DI). Black box given to us.
- Common Anode Seven Segment Display – 3 Nos. As 3 digits are to be displayed.
- 7447 - 1 BCD to Common Anode 7 Segment converter.
- 8255A – 2 nos. Interfacing with various IO devices.
- 2716 – 2 nos. Smallest ROM chip available is 2K and as we need to have even and odd bank and ROM is required at reset address which is at $FFFF0_H$.
- 6116 – 2 nos. Smallest RAM chip available is 2K and we need odd and even bank. We need RAM for stack and temporary storage of data.
- LS 138 – 2 nos. 3:8 decoders (Manual Attached)
- LS 373
- LS 245
- LS 244
- Required Gates
- Zip sockets
- Buzzer
- Switch

Address Map

Memory Map

RAM (2 banks of 2K each) – 00000H – 00FFFH

ROM (2 banks of 2K each) – FF000H – FFFFFH

I/O Map

8255: 00 – 06h

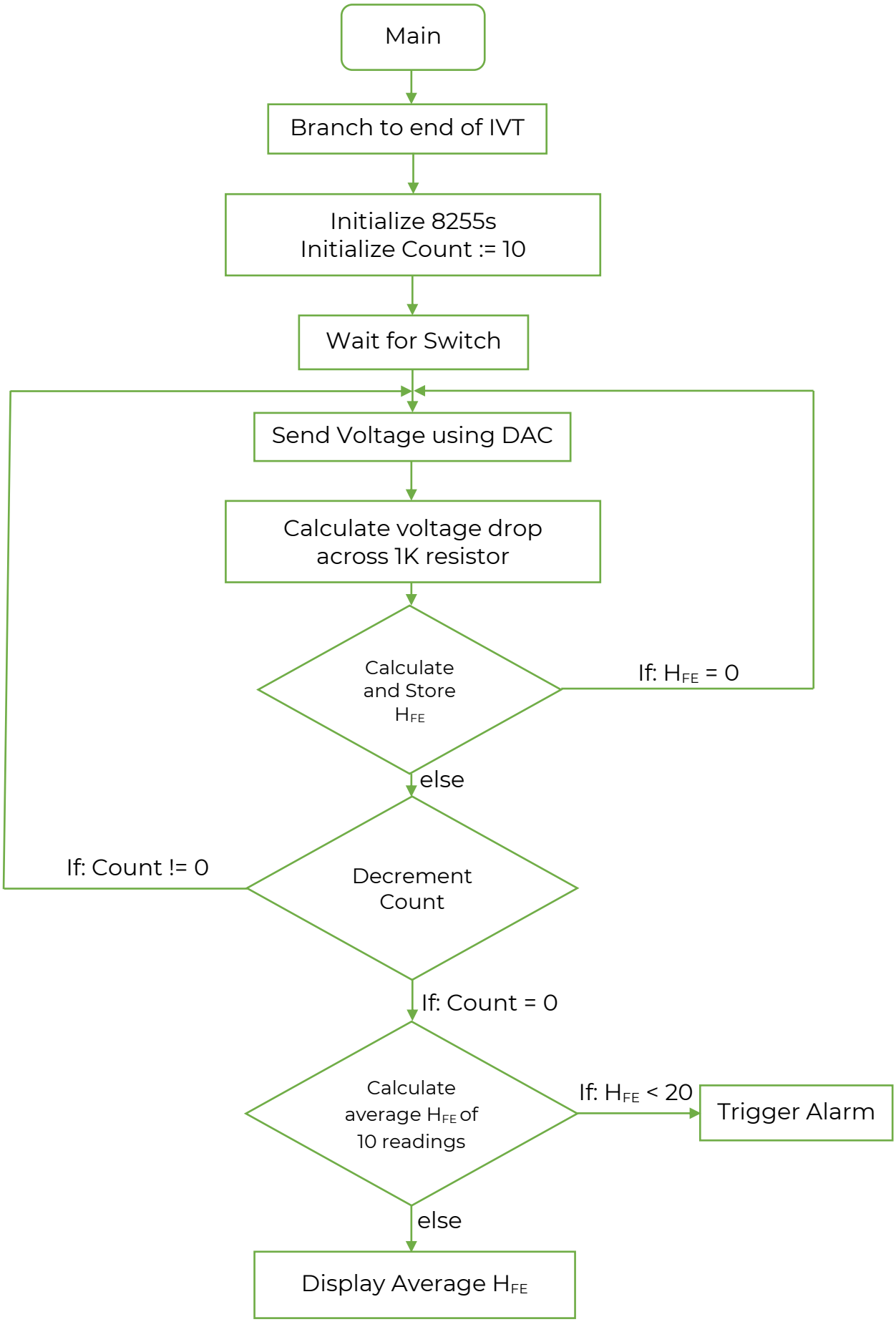
8255: 08 – 0Eh

Design

Complete design shown. (attached)

Flow Chart

Main Program



Variations in Proteus Implementation with Justification

1. ADC used is 0808 as AD7819 is not present in Proteus, hence an IVT had to be introduced, altering the Memory Mapping to:

   RAM- 02000-02FFF

   ROM- 00000-01FFF

2. DAC used is a Primitive DAC as AD558 is not present in proteus.
3. ROM used is 2732 as 2716 are not present in proteus.
4. As more ports were left due to unavailability of used ADC and DAC, we connected 3 7447 and connected them to display.

Firmware

Implemented using emu8086 attached.

List of Attachments

1. Complete Hardware Real World Design
2. Manuals
   a. AD558
   b. AD7819
   c. LS138
   d. 2N2369
3. Proteus File
4. EMU8086 ASM File
5. Binary File after assembly