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Real-Time Switch Fault Diagnosis for Non-Isolated DC-DC Converters

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Real-Time Switch Fault Diagnosis for Non-Isolated DC-DC Converters

***Abstract*— Fault tolerance in dc-dc converters is necessary in embedded and safety critical applications to prevent further damage and to make the continuity of service possible. Fast fault detection is a mandatory step in order to make suitable response to a fault in one of the semiconductor devices. The aim of this study is to present a fast yet robust method for fault diagnosis in non-isolated DC-DC converters. Fault detection is based on time and current criteria which observe the slope of the inductor current over the time. No additional sensors, which increase system cost and reduce reliability, are required for this detection method.**

For validation, computer simulations are first carried out. The proposed detection scheme is validated on a boost converter. Then, experimental tests are performed. A Field Programmable Gate Array digital target is used for the implementation of the proposed method, to perform real-time switch fault detection. Results show the effectiveness of the proposed detection method.

***Index Terms*— Switch fault detection, Fault diagnosis, Field Programmable Gate Array (FPGA), DC-DC converter.**

I. INTRODUCTION

DC-DC power converters are widely used in a variety of applications including aerospace, ships, electric vehicles and renewable energy power systems. In such embedded or safety critical applications, a high level of system reliability is mandatory. However, power electronic converters are sensitive to a sudden failure in their semiconductor devices. In fact, according to [1], power semiconductor devices are the most fragile component of power electronic converters. A sudden switch failure can have undesirable consequences on the system performances. For this reason, switch fault diagnosis and fault tolerant converter topologies have been an interesting topic of research in recent publications [2]-[7]. In order to make an efficient response to a switch fault in power electronics converters, the first step is to perform fast fault diagnosis and to identify the fault location.

Several papers have studied fault detection methods in power electronic converters [7]-[15]. Fault detection in a multilevel converter is studied in [7], [8]. A detection method for faults in IGBT switches based on gate signal monitoring is presented in [9]. Open-circuit faults in matrix converters are studied in [10], [11]. Nonlinear observers are used in [12] to detect open-switch faults in induction motor drives. Another method for the detection of open-switch faults in voltage source inverters feeding AC drives, based on analyzing the load currents, is presented in [13]. Fast FPGA-based fault detection based on a simultaneous "time and voltage criteria" for a two-level converters is presented in [14], [15].

Although most of the previously cited researches deal with ac/dc or ac/ac converters, an increasing number of recent papers are focused on fault diagnosis in dc-dc converters. Fault diagnosis in the power conversion stage of a grid-connected photovoltaic system is studied in [16]. Open circuit fault detection in an isolated full bridge converter is presented in [17]. A fault detection method for three level dc-dc converters is presented in [18]; it is based on the monitoring of the flying capacitor voltage. Application of kalman filter in model based fault diagnosis of a dc-dc boost converter is presented in [19]. Another diagnosis method based on harmonic components of the magnetic near field of a dc-dc converter is presented in [20]. In [21], switch faults are detected in a boost converter by comparing the duty ratio and inductor current sloop. In this method three switching periods are needed to detect the fault.

In this paper, an effective FPGA-based real-time method is presented for fast switch fault diagnosis in non-isolated dc-dc converters operating in Continuous Current Mode (CCM). Both open circuit and short circuit faults are concerned. The approach we propose is based on the monitoring of the inductor current. Fault is detected by using a hybrid structure via coordinated operation of two fault detection subsystems. No additional sensors are used, as the inductor current has to be normally measured for control purpose. By avoiding additional sensors, cost is not increased and overall system reliability is improved.

In order to perform real time fault detection, the proposed algorithm must be implemented on a very fast digital target. On the other hand, fault diagnosis must be executed in parallel with other control tasks. Thanks to its parallel architecture, FPGA can run these tasks very quickly; as a result, it appears to be the most suitable choice for the implementation of such switch fault detection schemes. Moreover, high performance of FPGA for many power electronic and drive applications has been proved [22]. Also, by implementing both fault diagnosis and converter control units on a single FPGA chip, the system cost will be decreased and interfaces will be limited. In this paper, an Altera Stratix family FPGA chip is used to perform the proposed fault-detection method. The FPGA implementation procedure is based on a methodology for rapid prototyping, detailed in [23]. Experimental tests are also carried out to validate the effectiveness of this method.

In the following, the studied dc-dc converter family is reviewed briefly in section II. The proposed fault detection method is presented in section III. Simulation results are presented in section IV. The fully experimental results are provided in section V. The presented results show the effectiveness of the proposed fault detection method. It is shown that using this method, the real time switch fault diagnosis can be performed in only 20µs, while this value is only restricted by the natural delays in the system.

II. SINGLE-ENDED NON-INSOLATED DC_DC CONVERTERS: REVIEW OF APPLICATIONS, OPERATIONS AND TOPOLOGIES

There are various topologies for dc-dc converters used in classical power electronics applications. In this paper, we

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propose a real time switch fault diagnosis, dedicated to one family of dc-dc converters, so called "non-isolated single-ended dc-dc converters". Fig. 1 summarizes this family that consists of buck, boost, buck-boost, Ćuk, SEPIC, and dual SEPIC converters [24], [25].

These converters are increasingly being used in industrial applications. Among their vast range of applications, one can mention electric traction, electric vehicles, renewable dc sources, machine tools, and power factor correction (PFC) applications. Some other applications are in distributed dc systems in ships, airplanes, and computer and telecommunication applications [24]-[28].

Most of the previously cited applications are either embedded or safety critical ones for which switch fault diagnosis and consequently fault tolerant operation is of major interest.

As shown in Fig. 1, in non-isolated single-ended dc-dc converters, the shape of the inductor current (i_L) is the same. Because of this similarity, the proposed fault detection method studied in this paper is only applied to the particular case of a boost converter and can be generalized to the other mentioned topologies.

There are two operation modes for the boost converter (in CCM). Mode 1 starts when the switch S is turned on as illustrated in Fig. 2 (a). In this mode, the diode is reversed biased and is off. During DT_s the input voltage is applied across the inductor, where T_s is the switching period and D is the duty ratio. Consequently, the inductor current i_L ramps up linearly, increasing the energy stored in the inductor. The staying condition in mode 1 is q=1.

Mode 2 begins when the switch S is turned off, as shown in Fig. 2 (b). During $(1\text{-}D)T_s$, the stored energy in the inductor flows to the load and forces the diode to conduct. As a result the inductor current i_L decreases. The staying condition in this mode is q=0.

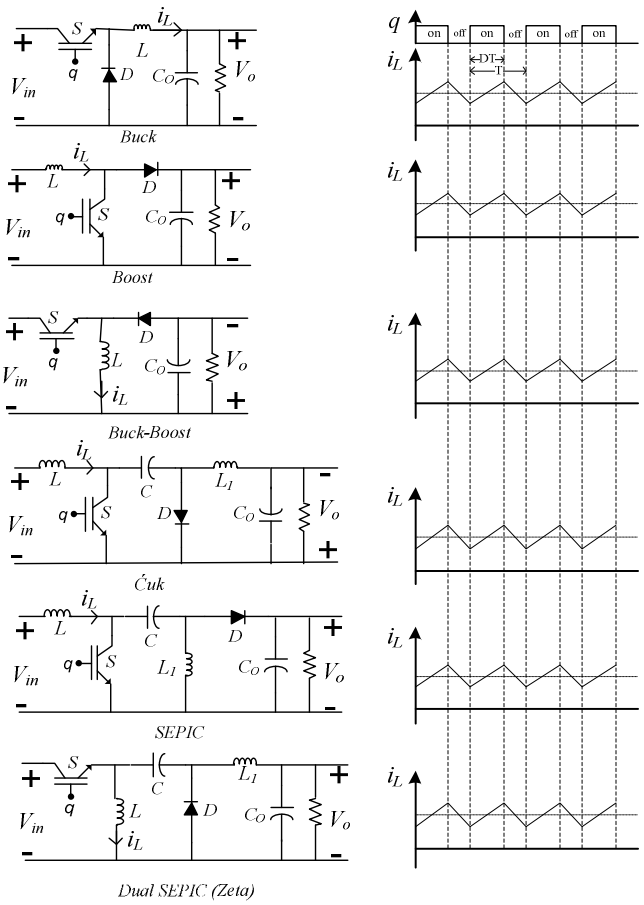

Fig. 1 Single-ended dc–dc non-isolated converters.

This common inductor current shape in single-ended dc-dc converters has been considered in the proposed fault diagnosis.

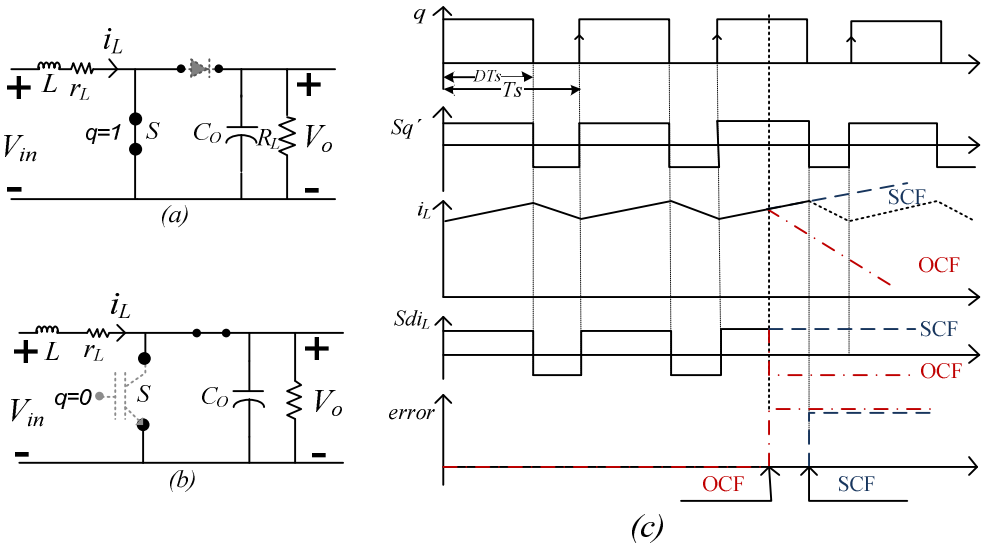

Fig. 2 (a) Boost converter in mode 1 (b) Boost converter in mode 2 (c) Signals for a boost converter in FD1

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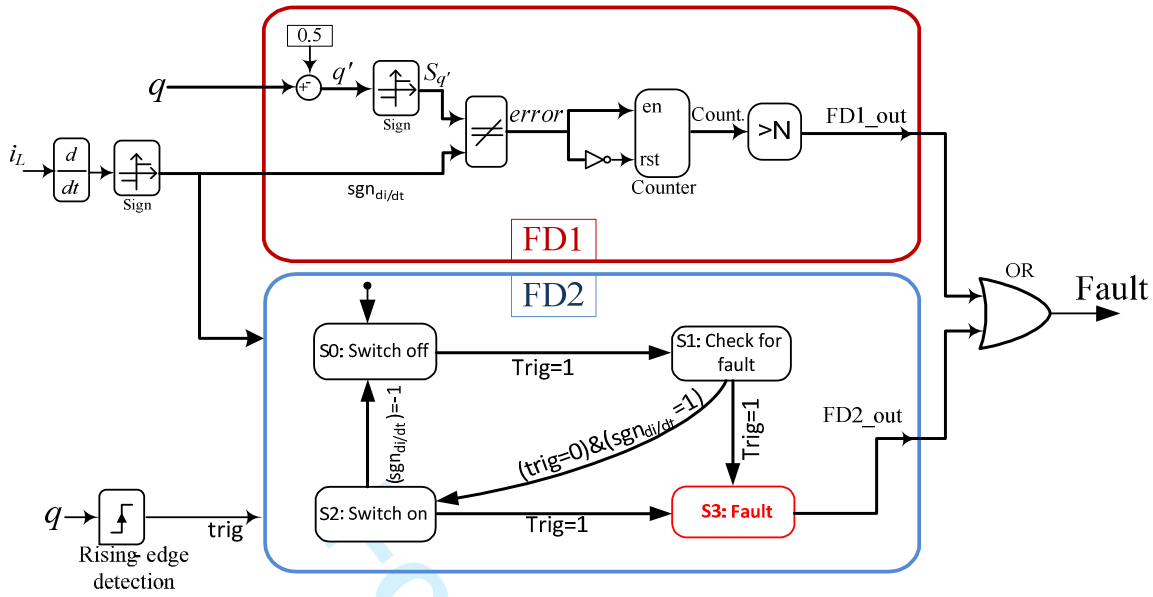

Fig. 3 Switch fault diagnosis based on FD1 and FD2 algorithms.

III. Fault Diagnosis

The proposed switch fault diagnosis is based on two algorithms that consider the shape of the inductor current to detect Open-Circuit Fault (OCF) or Short-Circuit Fault (SCF) in a switch (Fig. 3). The primary algorithm (so called FD1) is faster than the secondary one (FD2) but it is less robust to detect an OCF for small *D* value and to detect SCF for large *D* value or in high frequency switching case. The secondary algorithm is more robust and detects efficiently the faults in any conditions, but it is not as fast as the first one. It can be said that the secondary algorithm acts as backup fault diagnosis. Both algorithms are described in the following.

A. *Primary algorithm (FD1)*

As shown in Fig.2, turning on the switch S increases the inductor current i_L. Consequently, its slop is positive during DT_s thus the sign of the slop of i_L remains positive during this time interval. Fig. 3 presents the general scheme of the proposed fault diagnosis. In subsystem FD1, the inductor current (i_L) passes through a derivation block and then through a sign block which computes *Sgn di/dt*. If i_L increases, *Sgn di/dt* =1 and if i_L decreases *Sgn di/dt* =-1. The calculated error signal is equal to 1 when estimated and measured current slopes are different. If there is no switch failure, the two signals *Sgn di/dt* and *Sq'* have the same values, then the signal "error" is equal to 0, as described in (1).

$$\begin{cases} \begin{cases} sgn_{\frac{di}{dt}} = 1 \\ S_{\acute{q}} = 1 \end{cases} & t \in [0\ , DT_s] \\ \begin{cases} sgn_{\frac{di}{dt}} = -1 \\ S_{\acute{q}} = -1 \end{cases} & t \in [\ DT_s, T_s\ ] \end{cases} \quad (1)$$

As depicted in Fig. 2, in faulty condition, the shape of i_L does not correctly follow the switch command. In OCF, i_L decreases and in SCF i_L increases regardless of the switch command. In any case, the error signal will be set to '1' and then the counter starts to count.

It is noticeable that, as a result of non-ideal behavior of power switches, delays and dead times are inevitable. Therefore, a time criterion is employed to take into account for these delays and dead times.

Here the signal "error" is observed, and if it always remains in state "1" for an enough long time (N observation periods, equal to *NTc*), then it may be concluded that there is a fault. This observation time should be longer than the overall delays caused by the sensors, drivers, controllers and switches; otherwise the inherent but normal delay of the system may be interpreted as a fault. In the studied experimental (mentioned in section V) setup this overall is about 10 delay µs. therefore the observation time (*NTc*) is chosen equal to 20 µs.

FD1 algorithm is very fast and detects a fault in N sampling time after its occurrence. But for an OCF, for small *D* values or in high frequency switching applications, the counter could not reach the predefined value of N because the value of *Sq'* will change after *DTs* and the error will come back to '0'. In other words, for an OCF, during *DTs* the estimated and measured values of the sign of the inductor current's slope will be different. However if this faulty time is lower than the observation time, fault cannot be detected. For a SCF, fault cannot be detected when the faulty portion of the switching period (equal to *(1-D)Ts*) is smaller than the observation time. For this reason, the secondary algorithm FD2 is proposed.

B. *Secondary Algorithm (FD2)*

As described before, there are two operation modes (in CCM) for the conventional boost converter. In Mode 1 the

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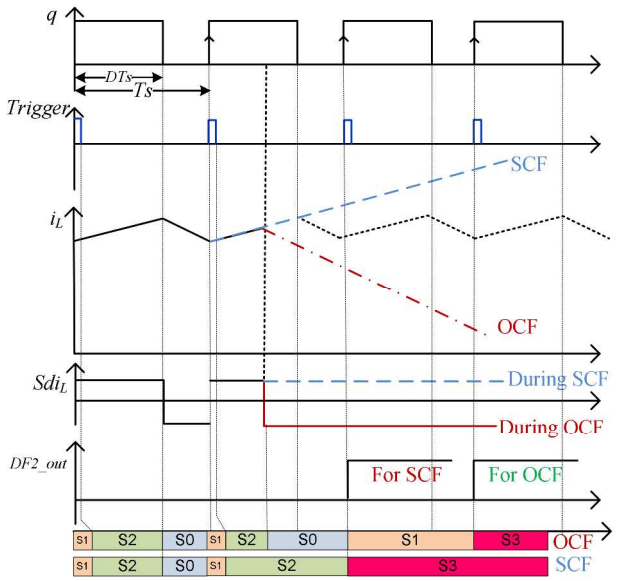

Fig. 4. FD2 algorithm signals and states.

inductor current increases while in mode 2 it decreases. According to Fig. 4 by each pulse of "Trig" the inductor current i_L increases and then decreases, if it only increases or decreases continuously between two "Trig" it can be concluded that a failure has occurred.

As shown in Fig. 3 for fault diagnosis by FD2, a state machine with four states is used. In initial transition (state S0) converter is in mode 2 of operation i.e. q=0, and stays in this state until q=1 and Trig=1; then the transition to state S1 occurs.

In state S1:

- If no failure has occurred, the switch S is turned on, i_L increases and *Sgn di/dt* =1 thus a transition occurs to state S2.
- If an OCF has been occurred, so the switch S is not turned on, i_L decreases and *Sgn di/dt* =-1. The conditions for the transition from S1 to state S2 are not satisfied. The system stays in S1 until the next Trig transition occurs to S3.
- If a SCF has been occurred the switch S is closed, so as in normal condition, i_L increases and *Sgn di/dt* =1, a transition occurs from S1 to S2.

State S2 corresponds to mode 1 of operation i.e. q=1. In normal condition, the system stays in S2, when q=0 a transition occurs to S0. But in SCF condition when q=0 the switch cannot be turned off, so no transition occurs to S0 until the next Trig, then a transition occurs to S3.

When a failure is occurred, the system goes to State S3 and stays in. In this state FD2_out becomes "1" and the fault is detected.

This algorithm is slower than the primary algorithm but it can detect the faults in any conditions, for any D and switching frequency values.

Finally, the general Fault Detection (FD) sets to '1' when one of the algorithms detects a fault (Fig. 3).

As described in this section, the proposed fault detection method can detect OCF as well as SCF very fast, without adding any extra current or voltage sensors in the system. It is interesting because additional sensors affect the system reliability and also increase the cost and weight of the system. Especially in aerospace, electric vehicles and airplane, the weight saving is an important issue.

IV. SIMULATION RESULTS

A Simulink model was developed for verifying the validity of the proposed fault detection method presented above. As mentioned before, because of similarity in the operation of single-ended non-insulated dc-dc converters family, the fault detection method is applied to a boost converter. The parameters used in simulation and experimentation are summarized in TABLE I. A 10 µs delay is considered to stand overall system delay. As mentioned above, the fault observation time is chosen equal to 20 µs. Thus sample time (Tc) is chosen equal to 1 µs, corresponding to the FPGA operation frequency which is used in the experimental setup, as explained in section V. Consequently, N is chosen equal to 20.

TABLE I PARAMETERS OF THE BOOST CONVERTER (FIG. 2)

Vin	40 V
L	3 mH
r_L	0.1 Ω
Co	2200 µF
RL	20 Ω
Switching Frequency	15 KHz

For OCF with D=50% and D=25%, also for SCF with D=50% and D=80% simulation results are presented and discussed in the following.

In Fig. 5, D is equal to 50% and an OCF occurs at t=300 µs. The primary algorithm (FD1) detects the fault after 20 µs and the secondary algorithm (FD2) waits for the next Trig to detect the OCF. Finally the fault is detected very quickly (in 20 µs). For D=25% in OCF condition, the simulation results

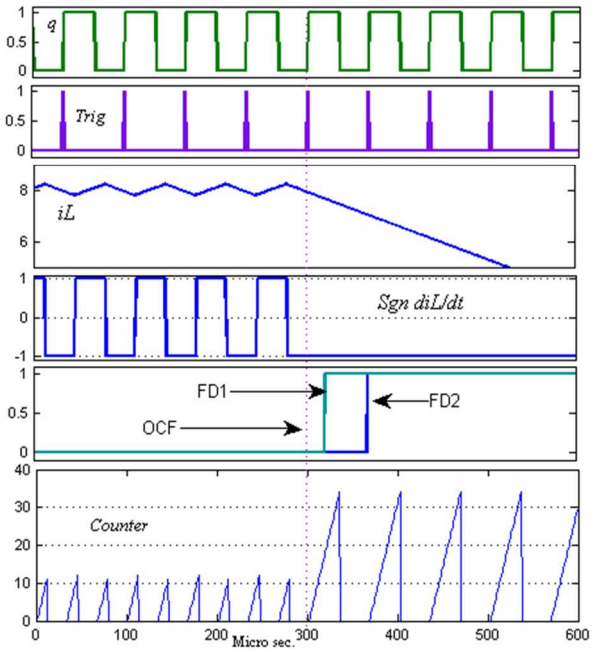

Fig. 5 Open circuit fault case (D=50%).

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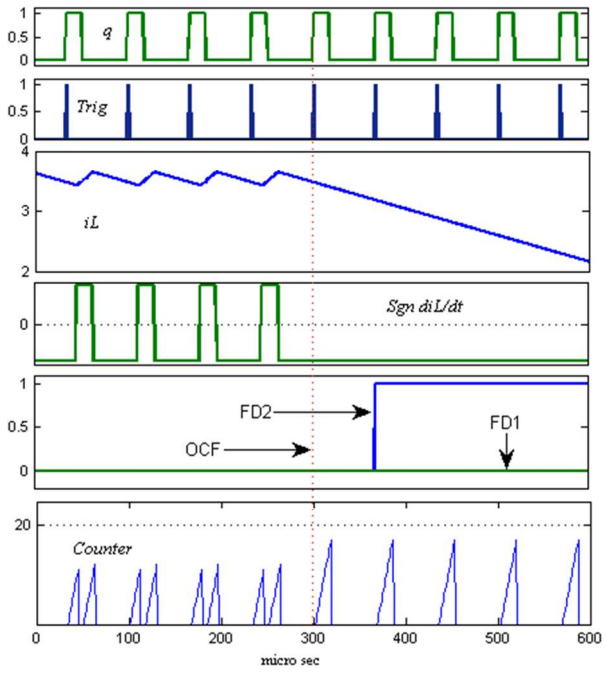


Fig. 6 Open circuit fault case (D=25%).

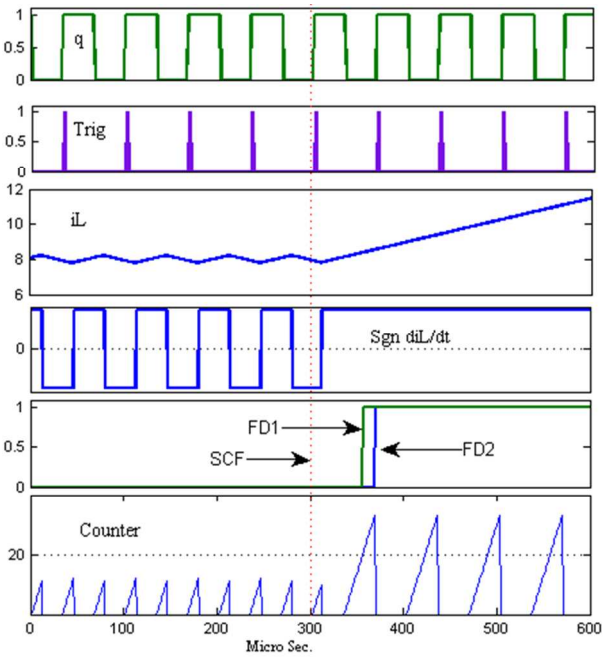


Fig. 7 Short circuit fault (D=50%).

are also presented in Fig. 6. It can be clearly seen that because of the small duty ratio, the counter cannot reach N=20 before the change of the command order *q,* so the FD1 algorithm cannot detect the OCF. However, FD2 detects the fault when the second Trig is applied. The maximum time that is needed to detect the fault is one switching period. It confirms the robustness and the fastness of the proposed method.

Fig. 7 presents the simulation results for SCF with duty ratio D=50%. Both algorithms detect the fault. When D=80%, as for OCF with D=25%, the counter cannot reach N=20, so

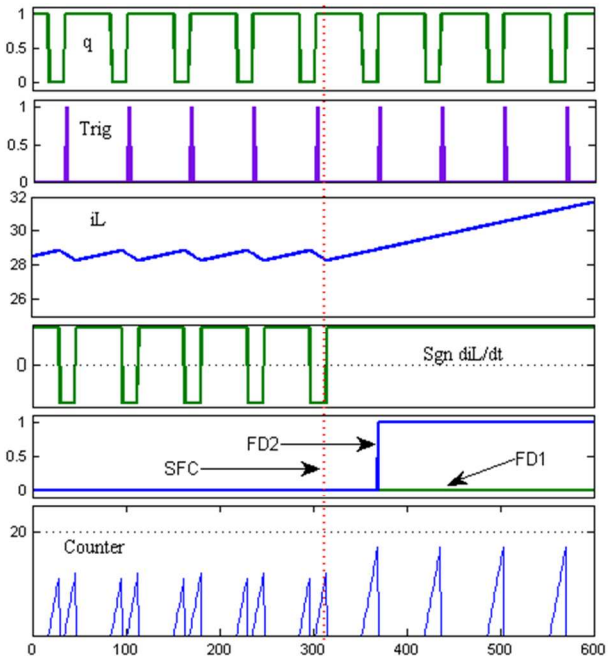


Fig. 8 Short circuit fault case (D=80%).

the fault cannot be detected by FD1 as shown in Fig. 8, but FD2 detects the fault in the following Trig. These simulation results confirm that the proposed method can detect fault as fast as 20μs after its occurrence.

V. Experimental Results

The experimental setup is shown in Fig. 9. It is consisted of a boost converter, an FPGA and interface board, a dc load and a dc source. Parameters are the same as reported in the previous section. The fault detection and the control schemes are implemented on a single FPGA chip. The FPGA implementation is briefly explained in this section; a more detailed flow implementation can be found in [23]. After discrete simulations with Simulink in Matlab environment, simulation with Altera DSP Builder blocks is carried out. Simulink blocks are replaced with DSP Builder ones. For data exchange between DSP Builder and Simulink blocks, proper input/output blocks are used. Using DSP Builder allows us to have visual programming and to translate it to Harware Description Language (HDL) form very easily. An intermediate Hardware In the Loop (HIL) step is used for more realistic evaluation of the control and detection implementation. In this step, the power system is simulated in the Matlab/Simulink environment, while the control and diagnosis parts are both implemented on the single FPGA. The VHDL design is later compiled using Quartus software and uploaded on the Altera FPGA board via a Joint Test Action Group (JTAG) interface. Here, a Stratix DSP S80 development board is used, which includes the Stratix EP1S80B956C6 FPGA chip. This chip contains 79,040 programmable logic elements. For IGBT, SEMIKRON SKM50GB123D devices are used. It is controlled by a

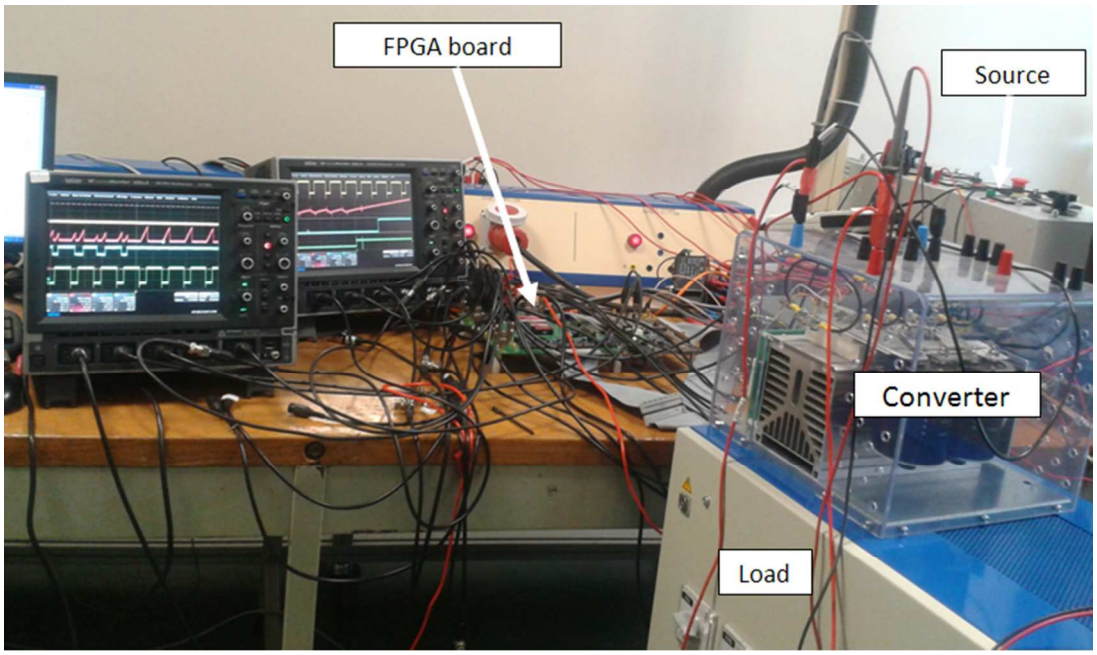


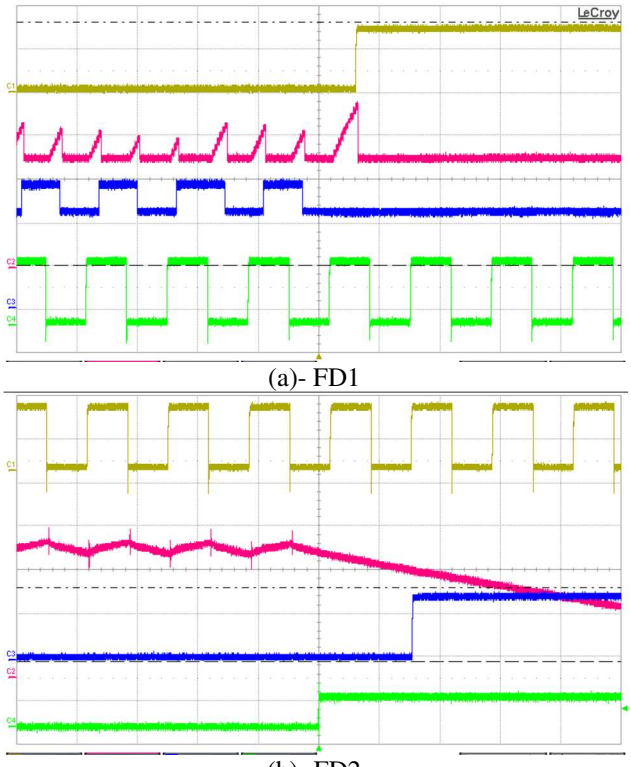
Fig. 9. Experimental setup realized for this study

SKHI22A driver. In this experimental setup, maximum total system delay (delay of IGBT and driver, A/D converter, sensors and interface circuit) is about 10 µs, therefore to avoid false fault detection, observation time (NTc) is chosen equal to 20 µs. Thus FPGA operation frequency is chosen equal to 1MHz, corresponding to a sample time (Tc) equal to 1 µs. Consequently, N is chosen equal to 20. It should be noted that a higher operation frequency for the FPGA will only result to higher sampling rate and a larger N, and the fault cannot be detected any faster. In fact, the detection time is only restricted by the unavoidable natural delays of the system. The switching frequency of the converter is equal to 15 kHz.

First, an open switch fault is studied. The switch is held open by removing its command signal. Fig. 10 shows the results for a duty cycle equal to 50%. Fig. 10-a shows the detection signals in FD1. It can be seen that after fault occurrence, the counter output passes the defined threshold (N), hence the fault is detected in 20µs. Fig 10-b shows the detection signals of FD2. Fault is detected when during a whole switching period, the current slope is negative. In this case, fault is detected in one switching period (67 µs). Both methods have successfully detected the fault, but FD1 is faster.

However for a small duty cycle, the output of the counter cannot reach the threshold N. Fig. 11 shows the open-circuit fault whit D=25%. Clearly, in this case FD1 is unable to detect the fault. However, FD2 will again detect the fault successfully. In other words, fast and robust fault detection is always possible using FD2. If possible, the fault detection will be still more rapid using FD1. It can be noticed that FD1 can detect the faults when faulty operation time in the switching period (DT_s for open-circuit and $(1-D)T_s$ for short circuit) is not smaller than the predefined detection time (NT_c).

Fig. 12 shows the results for a switch short-circuit fault. Both methods have detected the fault, and FD1 has been able to do it more quickly. Results are provided in Fig. 13 for a very large duty cycle (D=80%), and it can be seen that



(a)- FD1

(b)- FD2

Fig. 10. Open circuit fault detection with d=50%. (a) from top to bottom: FD1_out, counter, sgn(di/dt), q (b) from top to bottom: q, i_L (2 A/div), FD2_out, fault. Time scale: 50 µs/div.

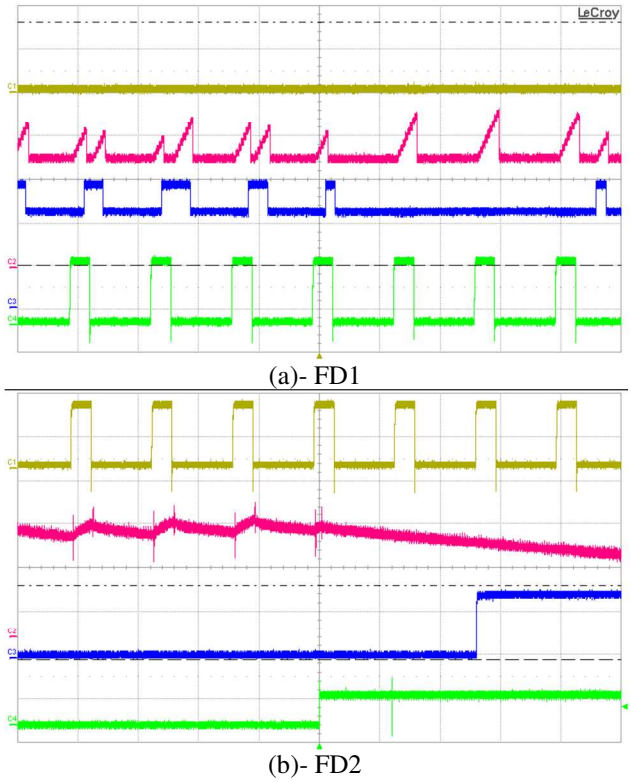


Fig. 11. Open circuit fault detection with d=25%. (a) from top to bottom: FD1_out, counter, sgn(di/dt), q (b) from top to bottom: q, i_L (2 A/div), FD2_out, fault. Time scale: 50 µs/div.

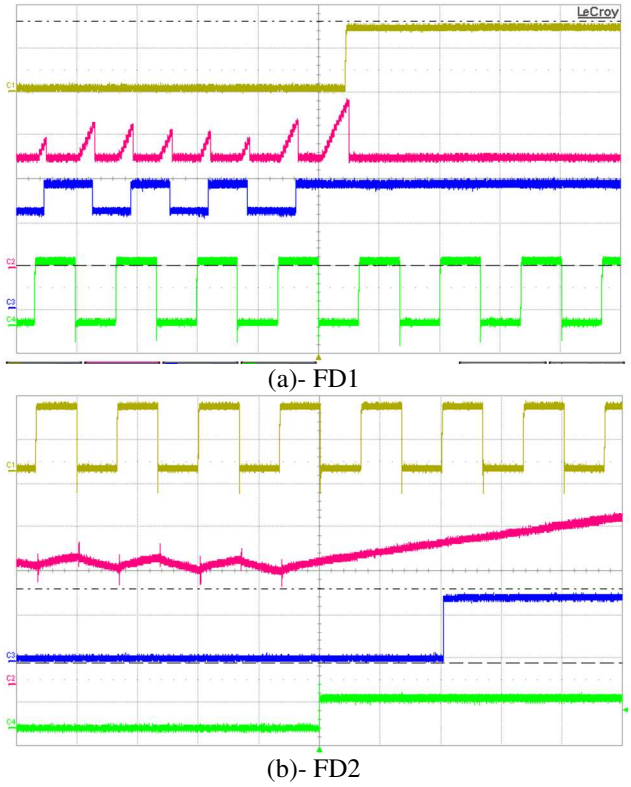


Fig. 12. Short-circuit fault detection with d=50%. (a) from top to bottom: FD1_out, counter, sgn(di/dt), q (b) from top to bottom: q, i_L (2 A/div), FD2_out, fault. Time scale: 50 µs/div.

although it is not possible to detect the fault with FD1, however FD2 has successfully detected the fault again.

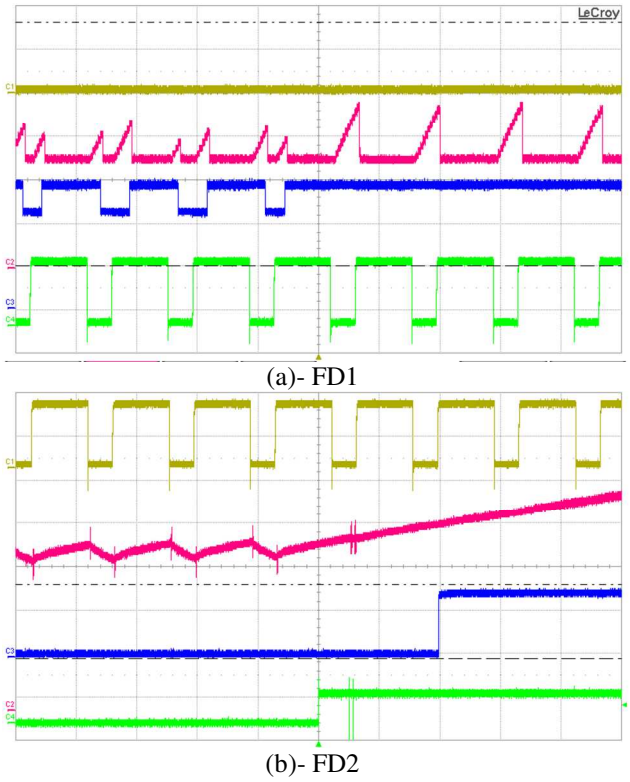


Fig. 13. Short-circuit fault detection with d=80%. (a) from top to bottom: FD1_out, counter, sgn(di/dt), q (b) from top to bottom: q, i_L (2 A/div), FD2_out, fault. Time scale: 50 µs/div.

These results show that the proposed method can always detect both open or short-circuit faults very quickly. The maximum detection time is around one switching period (67 µs in these experiments), but in most cases, it can be decreased to 20µs by using FD1 subsystem. Therefore robust real-time fault detection with this method is possible.

VI. CONCLUSION

Fault tolerant converters have been an interesting subject of research recently. In order to have a suitable response to a semiconductor fault in a dc-dc fault tolerant system, fast fault detection is the first step. Real time fault detection of non-isolated dc-dc converters is studied in this paper. A hybrid method is proposed that is based on two subsystems, one for robust fault detection (FD2) and the other one for fast fault detection, (FD1). Fault detection in FD2 is based on the fact that in normal operation of the converter, during a switching period with restricted duty cycle, the inductor current cannot always increase or decrease. FD1 directly compares the estimated and measured values of the sign of inductor current over the time for fault detection. Simulation and experimental results are carried out in order to evaluate the proposed method. An FPGA is used for experimental implementation of this method to perform real time fault detection. Results show excellent performance of this method for both open and short circuit switch faults. The proposed method is simple enough to

be implemented in a small FPGA target and it is fast, robust and efficient, without requiring any additional sensor.

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