2023 4th IEEE Global Conference for Advancement in Technology (GCAT)
Bangalore, India. Oct 6-8, 2023

VGA Controller Design & Implementation on FPGA

Akshay Chinchanikar
Department of Electronics and Telecommunication Engineering,
G H Raisoni College of Engineering,
Nagpur, India, 440016
akshay.chinchanikar.etc@ghrce.raisoni.net

Dr. Pankaj H. Chandankhede
Department of Electronics and Telecommunication Engineering,
G H Raisoni College of Engineering,
Nagpur, India, 440016
pankaj.chandankhede@raisoni.net

Dr. Abhijit Titarmare
Department of Electronics and Telecommunication Engineering,
G H Raisoni College of Engineering,
Nagpur, India, 440016
abhijit.titarmare@raisoni.net

2023 4th IEEE Global Conference for Advancement in Technology (GCAT) | 979-8-3503-0525-8/23/$31.00 ©2023 IEEE | DOI: 10.1109/GCAT59970.2023.10353298

***Abstract*- The purpose of this work is to understand, design soft VGA Controller on HDL tool which is a display interface, largely used in monitor system. Goal is to how can we distribute this VGA data on larger display in segment format which will be cost effective, So that The controller is designed by using Verilog HDL. It is implemented on FPGAs chip Spartan 6 xc6slx9-3csg324. The system will display colour shades on the monitor screen and test the design & implemented on the FPGA board.**

Index terms—VGA (Vedio Graphics Array) Controller(Hardware description language) , Verilog HDL, FPGA (Field Programmable Gate Array), SRAM(static Random Access memory), CLB(Configurable Logic Blocks), horizontal synchronizer(HS), vertical synchronizer(VS), Joint Test Action Group (JTAG).

I. INTRODUCTION

Early VGA introduced by IBM with resolution of 640x480. Designed specifically for analog displays. Analog displays replaced by LCD displays which allows higher resolution.[1] Which uses digital data. Now VGA is used in multiple systems like Desktops, ATM machines, video calling. VGA displays basic 8-bit RGB combination shades. Last IBM graphics standard was VGA. All IBM computer manufacturers conformed to use VGA graphic standard to all post 1990 computers.

There are some different VGA compatible text modes as shown in table 1.

TABLE I. VGA TEXTS MODE.

Sr no.	Columns	rows	Font size	resolution
1	80	25	9*16	720*400
2	40	25	9*16	350*400
3	80	43	8*8	640*344
4	80	43	8*8	640*400

FPGA is best platform to design unplanned design. FPGA made of registers(memory elements) to store information, flip flops, latches to hold data, logic gates to handle combination logics.[1] Concurrent processing is a feature which improvise the whole processing system which is absent in basic embedded system.

FPGA helps to understand detailed effect of every logic blocks. We have taken top to bottom approach to design VGA. Design code is Verilog HDL.

II. RELATED WORK

A. VGA Introduction

[1]-[15] VGA protocols have been developed on Altera IC s and Xilinx spartan 3, micro blaze processor based platforms. [2] camera interface with FPGA and connected with VGA display. In [15] image processing is done through FPGA to VGA display.

VGA protocol is one of the simplest forms to display images and video data in colour form.[2] VGA displays used where high-definition visual information is not required. standard VGA compatible displays have 640 column & 480 rows of pixel elements. Individual pixels are turned ON & OFF by VGA controller with combination of row and column. Combination of multiple on & off sequence of pixel creates image on display. Monitor scans thought entire screen.

B. Analog display

In old VGA monitor made of CRT (Cathode Ray Tube). Electron beam scans display screen in horizontal lines. Light Video signal turns on light which hits on screen which generate a color phosphor dot on front face of CRT. This process happens all over the screed with very high speed. Whole scanning and illumination light of a screen happened 1/60 of second. That means it can be called as 60 frames per second.

C. FPGA (Field Programmable Gate Array)

It is a semiconductor chip which consist of array of interconnected transistor level subcircuits which acts as on off switch to process the data. This offers high level of flexibility. They are inexpensive and highly versatile. Microcontrollers become increasingly powerful, but microcontroller is built around a processor & peripherals which brings hardware limitation like sequential processing.

FPGAs has JTAG programmable Configurable logic gates also possible to program through nonvolatile memory. FPGA has volatile memory architecture. HDL code gets erased after FPGA gets power off. To store the HDL code External memory EEPROM used. Due to parallel processing capabilities FPGA dominates microcontroller in information processing. FPGA has flexibility due interconnect subcircuits.[18]

In System On Chip (SOC) FPGA can be used. Due to reprogrammable hardware capability FPGA advantageous over microprocessor. Now a days variety of dedicated function blocks, memory blocks , multiplexer comes in current new FPGAs .

To handle the precise function of each block. the logic blocks have configuration memory. Following logic blocks used to implement HDL logic on FPGA.

1. Multiplexers
2. combinational gates like basic NAND gates or XOR gates
3. n-input Lookup tables
4. Wide fan-in And-OR structure
5. Transistor pairs

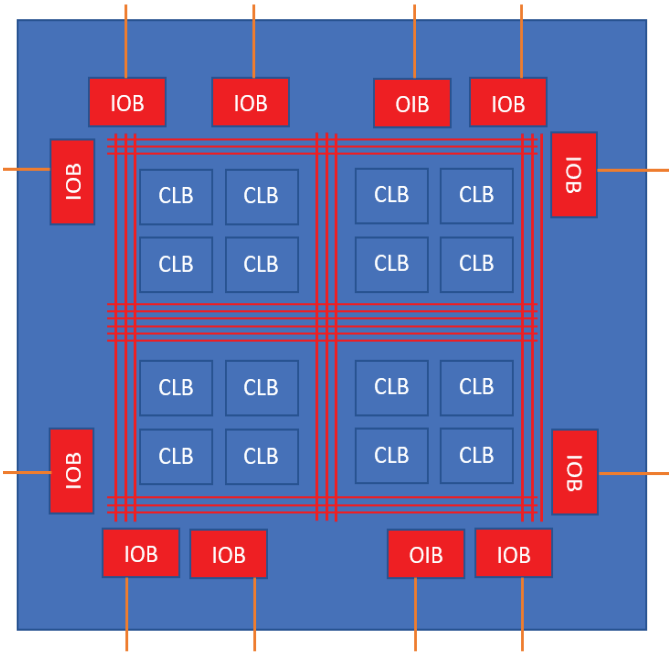

Fig. 1. Architecture of FPGA

III. Application of FPGAs

In Defence, aerospace application FPGAs are widely used due to high frequency processing.

FPGA use has increased in biomedical fields like CT scan, X rays, 3D imaging, medical data analysis, image processing through scanning.

In medical domain vision system works on very high resolution and high data processing capacity. FPGA helps them to handle these high-density data in real time. Concurrent processing capability of FPGA is responsible to fulfil this medical system requirement.

Large scale, Ultra large scale data system can get benefits of FPGA performance. Pin to pin latency in very low in FPGA hardware which is in few nano seconds. Good fan in fan out. This helps in big data storages and data mining.

IV. Proposed Methedology : Hardware Design and Synthesisr

VGA controller is mainly controlled by clock signal, red, green, blue, horizontal synchronizer (HS) & vertical synchronizer (VS).as shown in below black box figure 2.

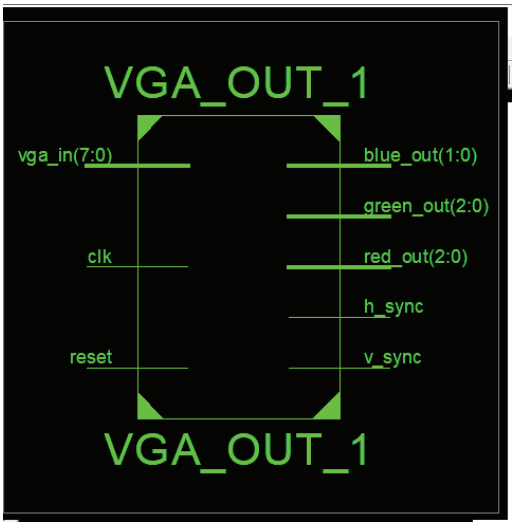

Fig. 2. VGA block diagram

HS and VS signals used to video/image data delivery on screen. HS indicates number of horizontal lines and VS defines refresh rate. Pixel clock defines available time to turn on and off single pixel process. Figure 2 is actual RTL schematic view from Xilinx 14.7 ISE tool.

25.175Mhz clock frequency is used to obtain 640*480 screen resolution. Higher frequency used to display higher resolution. Figure 3 shows VGA synchronization signal. It's a basic protocol of VGA communication.

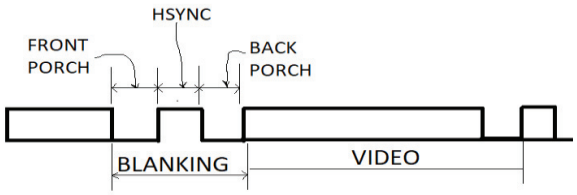

Fig. 3. Sync Signal waveform

V. Horizontal & Vertical Timings[]

A. Horizontal

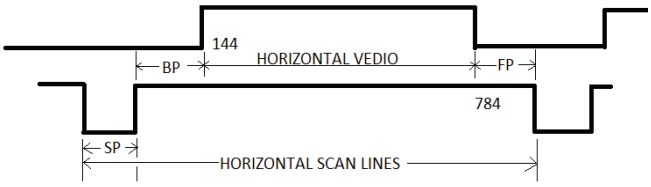

Fig. 4. Horizontal timing

Pixel clock = 25 Mhz timing 0.04 us
Horizontal video (HV) = 640 pixel x 0.04us = 25.6 us
Back porch (BP) = 16-pixel x0.04us = 0.64us
Front porch (FP) = 16-pixel X0.04us = 0.64us
Sync pulse (SP) = 128-pixel x 0.04us = 5.12us
Horizontal scan line = SP+BP+HV+FP

= 120+16+640+16 = 800 Pixels x0.04us = 32us
1/60Hz = 16.67ms/32us = 521 horizontal scan line per frame.

B. Vertical timing

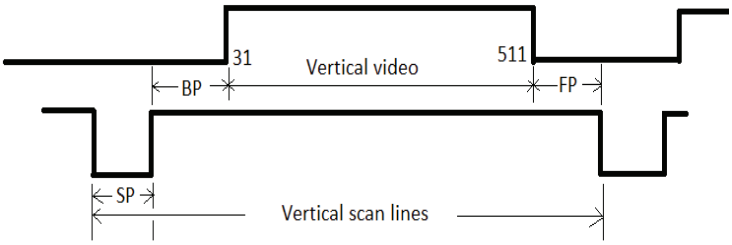

Fig. 5. Vertical timing

pixel clk = 25Mhz Horizontal scan line = 32us
Vertical video (VV) = 480 lines x32us = 15.360ms
Back porch (BP) = 29 lines x32us = 0.928ms
Front porch (FP) = 2 lines x 32us = 0.064ms
Vertical scan lines = SP+BP+VV+FP
= 2+26+480+10 = 512 lines x32us = 16.672ms.

VI. HARDWARE INTERFACING

A. VGA connector

TABLE II. VGA HARDWARE PORT PIN POSITION FUNCTION

Pin position	function
1	Red
2	Green
3	Blue
13	Horizontal sync
14	Vertical sync
6,7,8,9,10.11	Ground
4,5,9,12	Unused

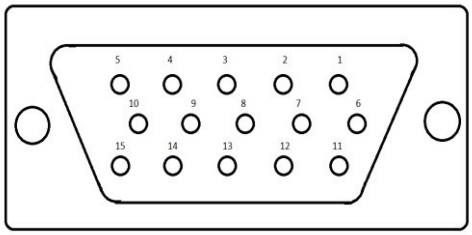

Fig. 6. VGA port front view

Figure 6. shows VGA port has total 15 pins each pin function has mention in table no. 1 above . RGB Color code of VGA are mentioned in table no. 2. At pin 1 ,pin 2 ,pin 3 are analog pins. It comes from resistive circuit from VGA female connector as a output. VGA color code is 3 bits combination data. Which generate 8 different colors as mention in table no 2. FPGA IC spartan 6 give 8 bits lor configuration. Each color has allotted 2 bits. As shown in

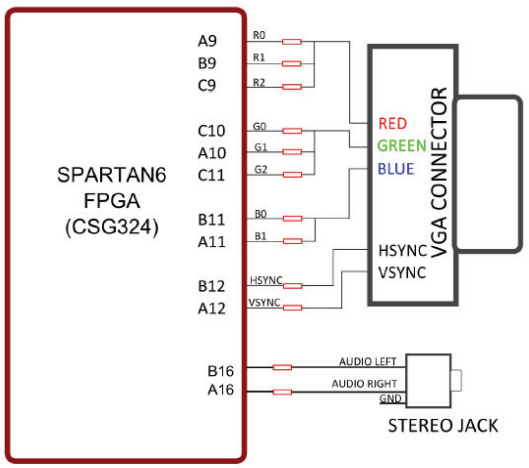

Fig. 7. spartan 6 VGA connection
Numato labs Nimas V2 board connection

TABLE III. VGA 3-BIT COLOR CODES [2]

Red	Green	Blue	Resulting color
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	While

VII. PROTOTYPE IMPLEMENTATION

VGA controller is designed on Xilinx 14.7 ISE web pack tool. Controller is designed in Verilog HDL. The Spartan 6 xc6slx9-3csg324 IC can work up to 200MHz.

Spartan 6 board Nemas V2 as shown in figure 8 which we used to test out prototype has 100 Mhz crystal clock Working voltage is 3.3v.

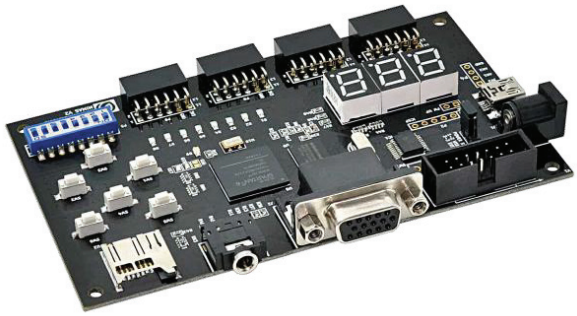

Fig. 8. Numalo Labs Nemas V2 board

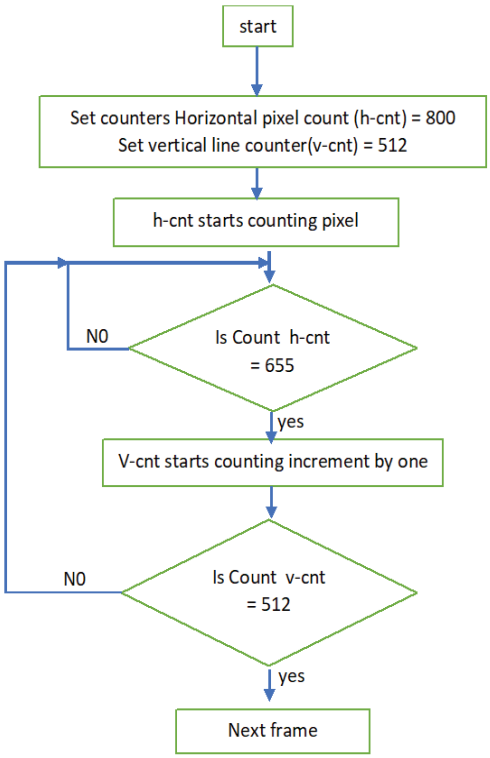

Fig. 9. flow chart on frame scanning

VGA's RTL code we used two major counters to scan pixel position. Every pixel counter vga data is being updates. After completing single horizontal row H-sync signal generate a flag that indicates one line has scanned. After 480 scanned line Vertical synchronized pulse v-sysnc indicate one frame is over. This whole process happens 60 time in a single second. If frame size is 680x480 then as shown in figure 9. H-count is 800, which includes front, back porch, display time & blanking area.

Figure 10 shows standard process of VGA communication for single frame. Which gives clarity of vertical and horizontal line synchronization and writing pixel data on each position of VGA display.

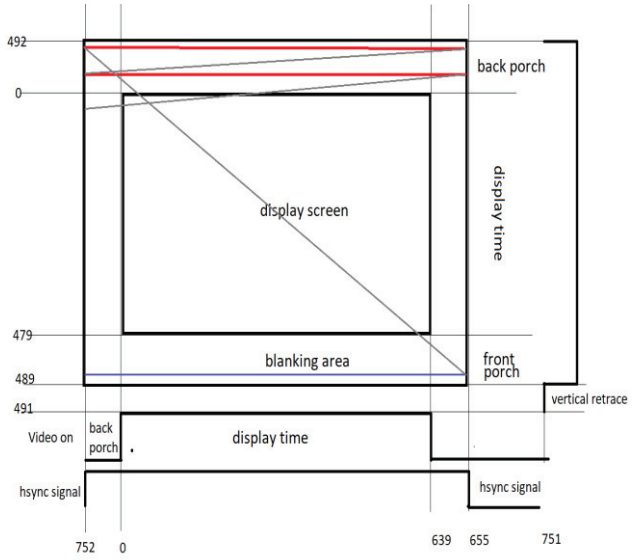

Fig. 10. VGA pixel count within single frame [7]

VIII. RESULT:

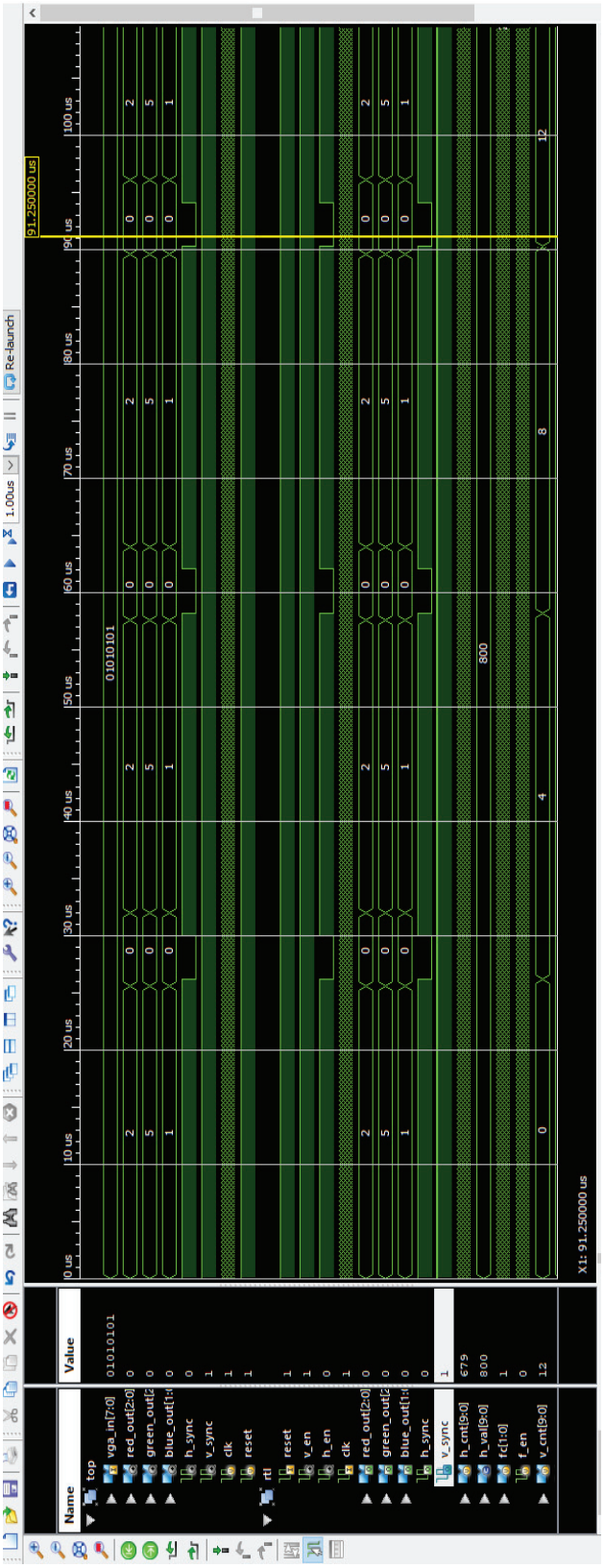

Fig. 11. VGA Simulation waveform Xilinx 14.7

Figure 11 shows waveform of VGA data transaction after applying color shade input. In waveform two horizontal line signals have trigged based internal counter "h_cnt" mentioned in waveform, Also color input data can be observed.

TABLE IV. SUMMARY REPORT

IC: spartan 6 xc6slx9-3csg324

Logic utilization	used	available	%
Slice registers	35	11440	3
Slice LUTs	77	5720	16
Fully used LUT-FF pairs	34	78	43
Bonded IOBs	20	200	19
BUFG/BUFGCTRLs	1	16	6

Table no, 4 shows hardware utilization of used fpga ic.

IX. CODE:

```
module VGA_OUT_1(
    input clk,reset,
        input [7:0] vga_in,
    output reg [2:0] red_out,green_out,
    output reg [1:0] blue_out,
    output reg h_sync,v_sync
    );

parameter [9:0] v_val = 9'h1f4,                          //---480
                frnt_prch_v = 9'h1df,   //...479
                back_prch_v = 9'h1ec,   //....492
                v_retrace =     9'h1e9,    //....489  back to top
                h_val = 10'h320,                         //...800
                frnt_prch_h = 10'h27f,  //....639
                h_retrace = 10'h28f, //.......655
                back_prch_h = 10'h2f0;  //....752

reg [9:0] v_cnt = 0,h_cnt = 0;
reg [1:0] fc = 0;
reg f_en = 0;
wire v_en,h_en;
//...................frequecy step down------------------------------

always@(posedge clk)
        begin
                if((!reset) || (fc == 2'b11))
                        begin
                                fc <= 2'b0;
                                f_en <= 1'b1;
                        end
                else
                        begin
                        fc <= fc + 11'b1;
                        f_en <= 1'b0;
                        end
       end
```

Fig. 12. Start of code

In figure 12 frequency step down logic is used to maintain frame rate of image. Divide by four logic is used for source clock.

```
//...................horizontal control.....................................
always@(negedge clk)
        begin
                if(!reset)
                h_cnt <= 0;
                else if(f_en)
                        begin
                                if(h_cnt == h_val)
                                        h_cnt <= 0;
                                else if(h_cnt < h_val)
                                        h_cnt <= h_cnt + 1'b1;
                        end
        end

assign h_en = (!reset | ((h_cnt > h_retrace) && (h_cnt < back_prch_h)))? 1'b0 : 1'b1;


always@(negedge clk)
        begin
                if(!reset)
                        h_sync <= 0;
                else
                        h_sync <= h_en;
        end
//.....................vertical control.....................................
always@(negedge clk)
        begin
                if((!reset) || (v_cnt == v_val))
                                        v_cnt <= 0;
                                else if((h_cnt == h_retrace) && (v_cnt < v_val))
                                        v_cnt <=  v_cnt + 1'b1;
                        end


assign v_en = (!reset | ((v_cnt <= back_prch_v) && (v_cnt > v_retrace)))? 1'b0 : 1'b1
```

Fig. 13. horizontal vertical sync line logic

Horizontal and vertical synchronization process is being done in code shown in figure 13.

```
//..................... VGA output.....................................

always@(posedge clk)
                        begin
                                if(!reset)
                                {red_out,green_out,blue_out}  <= 8'b0;
                                else if(h_cnt <= frnt_prch_h)
                                        {red_out,green_out,blue_out} <= vga_in;
                                else
                                        {red_out,green_out,blue_out} <= 8'b0;
                end



endmodule
```

Fig. 14. VGA output logic

8 bits Color data input has sent to output port with the help of Vertical and Horizontal sync pulse signals.

X. CONCLUSION

VGA is old protocol but we wanted to improve its application range. Because VGA is mainly used for single display output. To further improvisation, we need to understand gate level design process on spartan 6 series FPGA at 100 MHZ clock source on VGA. Which we have done for Future scope of this work which is to how can we split the VGA data into multiple VGA ports to project broader image or picture. This work can be expanded by increasing multi-port VGA functionality system.

REFERENCES.

[1] Syed, Zaheeruddin, and Munwar Shaik. "Fpga implementation of vga controller." In International Conference on Electronics and Communication Engineering, pp. 46-51. 2012.

[2] Nagarjuna, Ila, and Pillem Ramesh. "An FSM Based VGA Controller with 640□ 480 Resolution." International Journal of Engineering Yunxiang Zhang and Advanced Technology (IJEAT) 2, no. 4 (2013): 881-885.

[3] Finley, Gary P. "A VGA tachistoscope." Behavior Research Methods, Instruments, & Computers 23 (1991): 546-547.

[4] Andersen, Leif, Daniel Blakemore, and Jon Parker. "VGA Controller." (2012).

[5] Aftab, Khan Huma, and Monauwer Alam. "Design of VGA Controller using VHDL for LCD Display using FPGA."

[6] Jaya, Hang Tuah. "The Design and Implementation of VGA Controller on FPGA."

[7] Wasu, Renuka, and Vijay R. Wadhankar. "Review on Design of VGA Controller Using FPGA."

[8] Ekanayake, E. M. S. L. B., and W. A. S. Wijesinghe. "Hardware implementation of VGA controller on FPGA." (2015).

[9] Bakar, Mohamad Sharif Abu. "Keyboard Controller VGA Controller Online." PhD diss., UMP, 2010.

[10] Hanna, Darrin M., and Richard E. Haskell. "VGA graphics in a VHDL/FPGA digital design course." In Proc. ASEE 2010 NCS Spring Conference, pp. 26-27. 2010.

[11] Yadav, Niveditha, M. YaseenBasha, S. Rohith, and H. Venkateshkumar. "Algorithm to Design VGA Controller on FPGA Board." IOSR Journal of VLSI and Signal Processing 6, no. 6 (2016): 82-86.

[12] Ying, Fangqin, and Xiaoqing Feng. "Design and implementation of VGA controller using FPGA." International Journal of Advancements in Computing Technology 4, no. 17 (2012).

[13] Thakar, D.A., Nayak, R.J., Chavda, J.B., Patel, J.R. and Patel, M.P., 2018. Design of Image Display Controller Component for VGA Interfaced Monitor using ZedBoard. In 2nd International Conference on Current Research Trends in Engineering and Technology (pp. 2395-1990).

[14] Swetha, V., Kumar, D.S. and Krishnudu, P.M., FPGA Based IP Core Initialization for Ps2-Vga Peripherals Using Microblaze Processor.

[15] Raj, R., Aggarwal, M. and Mittal, G., Review on HDL Implementation of Digital Image Display on VGA. International Journal of Computer Applications, 975, p.8887.f

[16] Chandel, Prachi, Harshal Sao, and Pankaj Chandankhede. "Transformer Real Time Health Monitoring System." In 2022 IEEE Delhi Section Conference (DELCON), pp. 1-4. IEEE, 2022.

[17] Gogte, Purva, Shravankumar Purve, Roshni Bhave, Dipali Pethe, Pankaj H. Chandankhede, and Bhakti P. Thakre. "Survey: An IOT Based Approach for Hybrid Security Management in Health Care for Secure Cloud Storage." In 2023 11th International Conference on Emerging Trends in Engineering & Technology-Signal and Information Processing (ICETET-SIP), pp. 1-4. IEEE, 2023.

[18] Chinchanikar, Akshay, Pankaj H. Chandankhede, and Abhijit Titarmare. "Design of Binary Neural Network Soft System for Pattern Detection using HDL Tool." In 2023 7th International Conference on Computing Methodologies and Communication (ICCMC), pp. 393-398. IEEE, 2023.

[19] Titarmare, Vedant, Pankaj H. Chandankhede, and Minakshi Wanjari. "Interactive Zira Voice Assistant-A Personalized Desktop Application." In 2023 2nd International Conference on Paradigm Shifts in Communications Embedded Systems, Machine Learning and Signal Processing (PCEMS), pp. 1-6. IEEE, 2023.

[20] Jaiswal, P.,Dhakite, M., Dhule, C.,Wazalwar, S.,Deshmukh, A.R. "Smart AI based Eye Gesture Control System"7th International Conference on Intelligent Computing and Control Systems, ICICCS 2023, 2023, pp. 1873–1876

[21] Bhoware, A., Jajulwar, K., Deshmukh, A., ...Ghodmare, S., Gulghane, A."Performance Analysis of Network Security System Using Bioinspired-Blockchain Technique for IP Networks" International Conference on Emerging Trends in Engineering and Technology, ICETET, 2023, 2023-April

[22] Bhoware, A., Jajulwar, K., Deshmukh, A., ...Ghodmare, S., Gulghane, A."Performance Analysis of Network Security System Using Bioinspired-Blockchain Technique for IP Networks" International Conference on Emerging Trends in Engineering and Technology, ICETET, 2023, 2023-April

[23] Deshmukh, A.R., Dhawale, S.A., Dorle, S.S. "Analysis of Cluster Based Routing Protocol (CBRP) for Vehicular Adhoc Network (VANet) in Real Geographic Scenario" Proceedings of CONECCT 2020 - 6th IEEE International Conference on Electronics, Computing and Communication Technologies, 2020, 9198669

[24] Sharma, H.L., Deshmukh, A.R., Bawane, N.G. "Spread spectrum pattern & PN sequence retrieval in wireless ad hoc network: Design approach"Proceedings - 2nd International Conference on Emerging Applications of Information Technology, EAIT 2011, 2011, pp. 391–394, 5734966

[25] Choudhary, Swapna and Dorle, Sanjay, Secured SDN Based Blockchain: An Architecture to Improve the Security of VANET,in International Journal of Electrical and Computer Engineering System Published 2022 , Volume13, Issue 2, Page 145-153.