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System-on-Chip FPGA Devices for Complex Electrical Energy Systems Control

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Digital electronics has become a standard for controlling electrical systems. This is due to the constant improvement of the digital devices, whether in terms of density, performance, flexibility of use, or cost reduction [1]. This article looks into system-on-chip (SoC) field-programmable gate array (FPGA) for controlling complex electrical energy systems. These devices encompass multicore floating-point microprocessors embedded with standard peripherals and an FPGA fabric that allows the design of custom peripherals and specific hardware (HW) accelerators. Thus, SoC FPGA devices

One of them is the opportunity to enlarge significantly the size of the electrical energy systems to manage.

can be regarded as a good compromise between "super" microcontrollers (very fast in terms of computation but with a fixed microarchitecture) and pure FPGAs (ideal for specific concurrent microarchitectures but limited in terms of density).

SoC FPGA architectures are discussed and compared with state-of-the-art digital signal processor (DSP) controllers, since they can also be qualified as SoC devices as they are integrating floating-point microprocessor cores and substantial peripherals. The main differences between these two groups of devices lies in the opportunity offered to the designer by the SoC FPGAs to customize the SoC device via its internal FPGA fabric. Two case studies demonstrate that with SoC FPGAs one can go beyond standard control by introducing new auxiliary functions that enhance market competitiveness. The first application concerns a fuel cell (FC) hybrid electric system controlled by passivity-based power management associated with an aging prognosis algorithm. For this application, it is shown that the time and cost constraints justify the use of a soft processor core to implement the controller.

The second application concerns the maximization of the electrical power production of a photovoltaic (PV) field operating in mismatched conditions through the dynamic reconfiguration of the PV modules. This application allows us to illustrate the ability of SoC FPGA to solve a complex optimization problem in a time that is so short that the PV field operating conditions can be considered as constant. Second, it shows the benefits of implementing C/C++ high-level synthesis (HLS)-based HW accelerators by significantly simplifying the design space exploration phase.

Finally, to generalize the lessons learned from these case studies, we present an analysis of recent and inspiring controllers for complex electrical energy systems from which key principles for designing the next generation of SoC FPGA-based smart controllers are derived.

Embedded Digital Controllers and SoC: Evolution and Trends

Due to their ability to execute control algorithms of ever increasing complexity in a very short time, using cheap components, digital controllers took preference over the analog ones. Microcontrollers and DSPs are used [2], however, FPGA-based controllers also have some advantages [3]. DSPs and microcontrollers are flexible (C-based programming), low cost, and with a highly performing floating-point arithmetic logic unit. DSP controllers integrate a high number of peripherals, all well-fitting with the control of power electronics and drives. The main disadvantage of such devices is that they are based on a fixed microarchitecture that prevents the concurrent execution of tasks that could be executed in parallel. This significantly limits their timing performance, leading to the introduction in the controller of one sampling period delay that reduces the control system's bandwidth and introduces more chattering into direct control of power converters.

Initially designed as a simple fabric of lookup tables and flip-flops, FPGAs then integrated DSP units and memory banks and lately the end user has been able to easily synthesize 32-b reduced-instruction-set computer (RISC) processors within the FPGA fabric [4]. FPGAs are attractive for controlling industrial systems mainly because they allow the design of dedicated controllers that are the "hardware copies" of the source control algorithms, thus including the entire potential parallelism of these algorithms and, as a consequence, accelerating significantly their real-time executions. FPGAs can also handle the control of systems with a high number of inputs–outputs (I/Os), such as multilevel converters. Indeed, the parallelism can be inside the control algorithm and it can be intrinsic to the system to be controlled, like for multiphase motors. As no additional delay is introduced, the FPGA-based controller increases the bandwidth of the designed control loops, thus they are ideal for the direct control of power converters [3], including power electronics using the recently introduced wideband-gap power switches that are commonly driven with a switching frequency above 100 kHz [5]. Computational demanding algorithms like model predictive control are also good candidates for FPGA-based implementations because of their parallelized and highly pipelined architecture [6]. The main drawbacks of FPGAs are the lack of performing internal analog-to-digital converters (ADCs) and limited size, which make floating-point arithmetic architecture design problematic. However, Intel has introduced an FPGA with 32-b floating-point DSP units [7].

SoC devices were introduced around a decade ago, mainly due to the benefits brought to mobile phones and, more recently, to the Internet of Things (IoT) [8]. They also impacted control applications because of their impressive computational power; the parallelism of the computing tasks can also be obtained by running several tasks simultaneously on different processor cores, with the possibility to also embed a real-time Linux operating system (OS). Thus, SoC can help expand the domain of traditional control algorithms (Figure 1) and brings convergence between the worlds of DSP controllers and FPGAs.

The Texas instrument dual Delfino device [9] [see Figure 2(a)] represents a natural SoC evolution of traditional DSP controllers. It is based on dual 32-b floating-point DSP cores, with always more peripherals and dedicated arithmetic units like a Viterbi complex math unit and a trigonometric math

unit (TMU), which can be regarded as specific HW accelerators [Figure 2(a)]. With the TMU, a Park's transformation can be executed in about 100 ns, comparable to what can be achieved with an FPGA. Also, parallel computing is now possible since four tasks can be executed simultaneously, one on each DSP core and one in each of the two control law accelerators (CLA) cores. So, its clock frequency is 200 MHz but, because it is a multicore architecture, it can reach up to 800 million instructions per second. CLAs alleviate the DSP cores of low level but very time-constrained tasks, like an FPGA current/voltage controller would do. Most insulated-gate bipolar transistor-based inverter switching control functions in the 10-kHz frequency range can, therefore, be achieved.

SoC FPGAs (Xilinx Zynq, Intel FPGA Arria 10, or Intel FPGA Cyclone V devices [7]) include a dual-core ARM A9, along with powerful coprocessors like the single instruction, multiple data NEON, a set of peripherals to communicate with other boards, and highly performing FPGA fabric [Figure 2(b)]. The latter offers the designer the possibility to add custom peripheral and/or specific HW accelerators adapted to a given application. The 32-b ARM A9 microprocessors are intended to run a powerful OS-like embedded Linux. However, these processors can also be used for bare metal applications that are more adapted to standard control solutions for electrical systems. Running at 667 MHz, they feature high computing power and high-quality internal buses used for controlling either a simple peripheral via its internal registers or for exchanging a stream of data at high rate with an FPGA-based HW accelerator [10]. SoC FPGA components can easily implement 32-b RISC processor cores within the FPGA fabric (MicroBlaze for Xilinx, NIOS II for Intel/Altera, and ARM Cortex-M1 or -M3 [11]). These features offer huge flexibility to the designer who can, thanks to the FPGA fabric, integrate specific peripherals and/or HW accelerators plus additional 32-b RISC processor cores into the SoC architecture. Table 1 summarizes

SoC FPGA can make significant contributions to the key developments in complex electrical energy systems, especially those including renewable generators and those employing hydrogen technology.

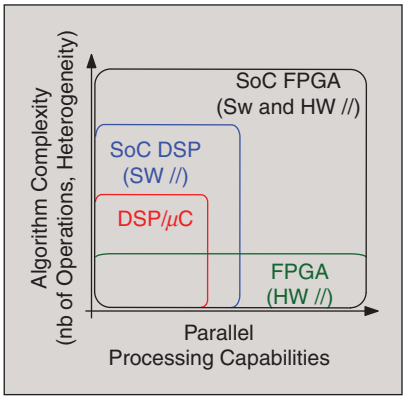

FIGURE 1 – A schematic showing the ability of each device technology to handle an algorithm's complexity and concurrency. nb: number.

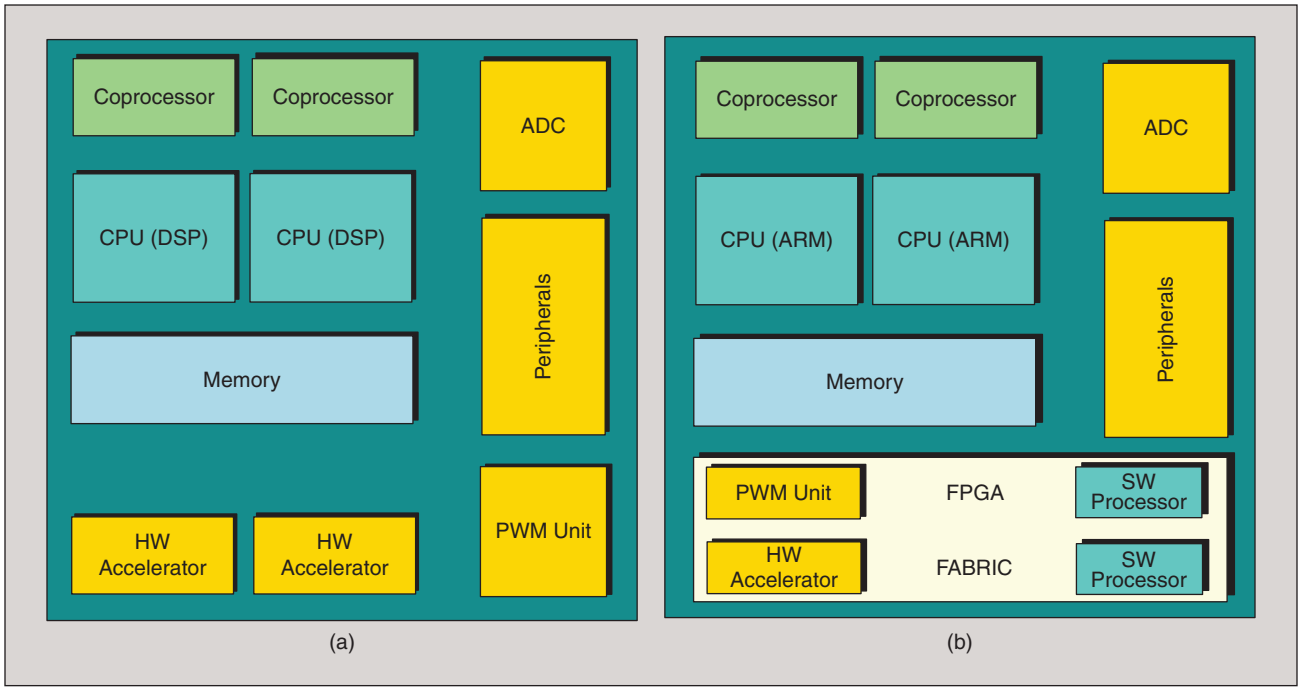

FIGURE 2 – The digital control architectures: (a) SoC DSP-based controllers and (b) SoC FPGA controllers.

Despite a number of limitations, SoC FPGA is one of the most promising digital technologies for implementing smart controllers.

pros and cons of the different types of SoC devices.

Case Studies

Control, Estimation, and Prognosis of a Hybrid FC System

Because of their large number of components like proton-exchange membrane FCs (PEMFCs), electrolyzers associated with hydrogen tanks for long-term storage [12], PV arrays, and power converters, and because of emerging possibilities in terms reinforcement of reliability offered by multistack FCs and interleaved converters [13], modern FC hybrid power systems can be considered very complex. To cope with this complexity, controllers are rapidly evolving by including always more new functionalities such as power sharing [14], impedance spectroscopy for data-based diagnosis [15], prognosis and fault system control [16], as well as weather and power consumption forecasting.

With SoC FPGAs, the HW processor cores and the FPGA fabric are tightly coupled for such control of complex electrical systems, so that the data communication is achieved with low latency. Therefore, one critical point that needs attention is the priority interrupt management. A vectored interrupt controller (VIC) integrated in the soft-core processor NIOS II (Intel/Altera) or hard-core processors ARM Cortex-R and M is mandatory to ensure the lowest interrupt latency and constant low jitters for real-time applications, compared with general ARM Cortex-A [17]. Thanks to the VIC unit of the Cortex-R5 of Xilinx Zynq UltraScale+, this powerful component is ready to handle critical real-time applications and, due to the integration a quad-core Cortex-A53, it is also highly adapted to high computing applications. However, considering the reduction of the costs, a soft-core processor solution, such as the NIOS II, may sometimes be a better option than using an oversized SoC FPGA due to its interesting properties: low interrupt latency and HW adaptability to the system to be controlled.

A proof of concept system, shown in Figure 3, was implemented to validate the performance of an SoC FPGA-based smart controller for a hybrid FC system composed of a FC stack and supercapacitors. It is worth mentioning that this plant is emulated in the DS1006 and DS5203 dSPACE boards [14]. All the corresponding blocks in Figure 3 are in solid blue lines. The modules related to the SoC FPGA-based controller are shown in solid red lines in Figure 3. Among them, the FC control and prognosis algorithms have been implemented in a NIOS II on a low-cost Cyclone V board (DE1-SoC Intel/Altera). Finally, all the modules shown in dashed lines, both within the plant or within the SoC FPGA-based controller, are not present in the current study but can be included in future developments, thus demonstrating the high level of scalability of the SoC FPGA-based control framework presented.

The complete HW/software (SW) system represents a hardware-in-the-loop (HIL) platform to validate the algorithms in real time [14]. The SoC FPGA architecture is composed of two pulsewidth modulation (PWM) units, an acquisition unit of six ADCs, and a soft-core base on a NIOS II. The algorithms are executed in three interrupt service routines (ISR) based on three synchronized timer events configured with a sampling time equal to 50 μs for the current loops and PWMs, 500 μs for the power management, and 1 s for a prognosis and health management (PHM) algorithms. The three ISRs use vectorized interrupts with a highest priority (0) for the current controllers (ISR0) and then priority 1 for the power management module (ISR1). The computation times are equal to 7.20 μs, 9.84 μs, and 117 μs, respectively [14].

Figure 4 shows all the main data computed in the emulated system

TABLE 1 – THE ADVANTAGES AND DISADVANTAGES OF THE DIFFERENT DIGITAL TECHNOLOGIES.

CRITERIA	DSP/μC	FPGA	SoC DSP	SoC FPGA
Algorithmic perspective	●○○	●○○	●●○	●●●
Algorithm complexity management	●○○	●○○	●●○	●●●
Rapidity, possibility of parallelism	●○○	●●○ (HW parallelism: concurrency & pipeline)	●●○ (Multicores SW parallelism)	●●● (both HW & SW parallelism)
Accuracy (floating-point capability)	●●●	●●○	●●●	SW: ●●● HW: ●●○
Connectivity	●○○	●○○	●●○	●●○
Analog interface (ADC, DAC)	●●○	●○○	●●○	●○○
Digital interface (number of I/Os)	●●○	●●●	●●○	●●●
Embedded peripherals	●●○	●●○	●●●	●●●
Embedded OS (Internet access,...)	●○○	●○○	●○○	●●●
Flexibility of use	●●○	●●○	●●○	●●○
Coding facilities	●●●	●●○	●●●	●●○
Microarchitecture adaptation, SW processor core implementation, obsolescence risk reduction	○○○	●●●	●○○	●●●
Learning curve	●●●	●●○	●●○	●○○
Cost	€○○	€€○	€○○	€€○

Score: ○○○ bad, ●○○ medium, ●●○ good, ●●● very good. DAC: digital–analog converter.

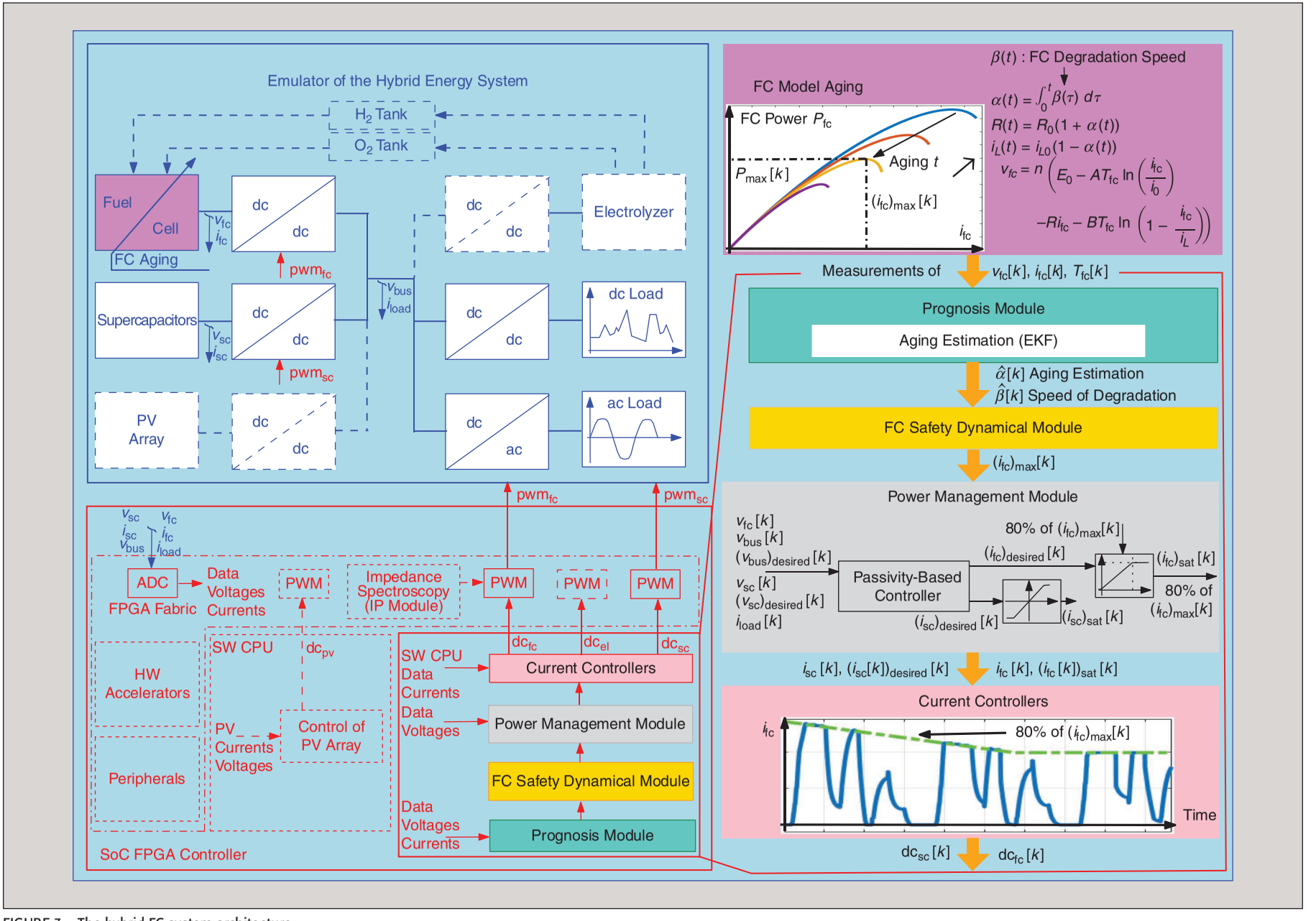

FIGURE 3 – The hybrid FC system architecture.

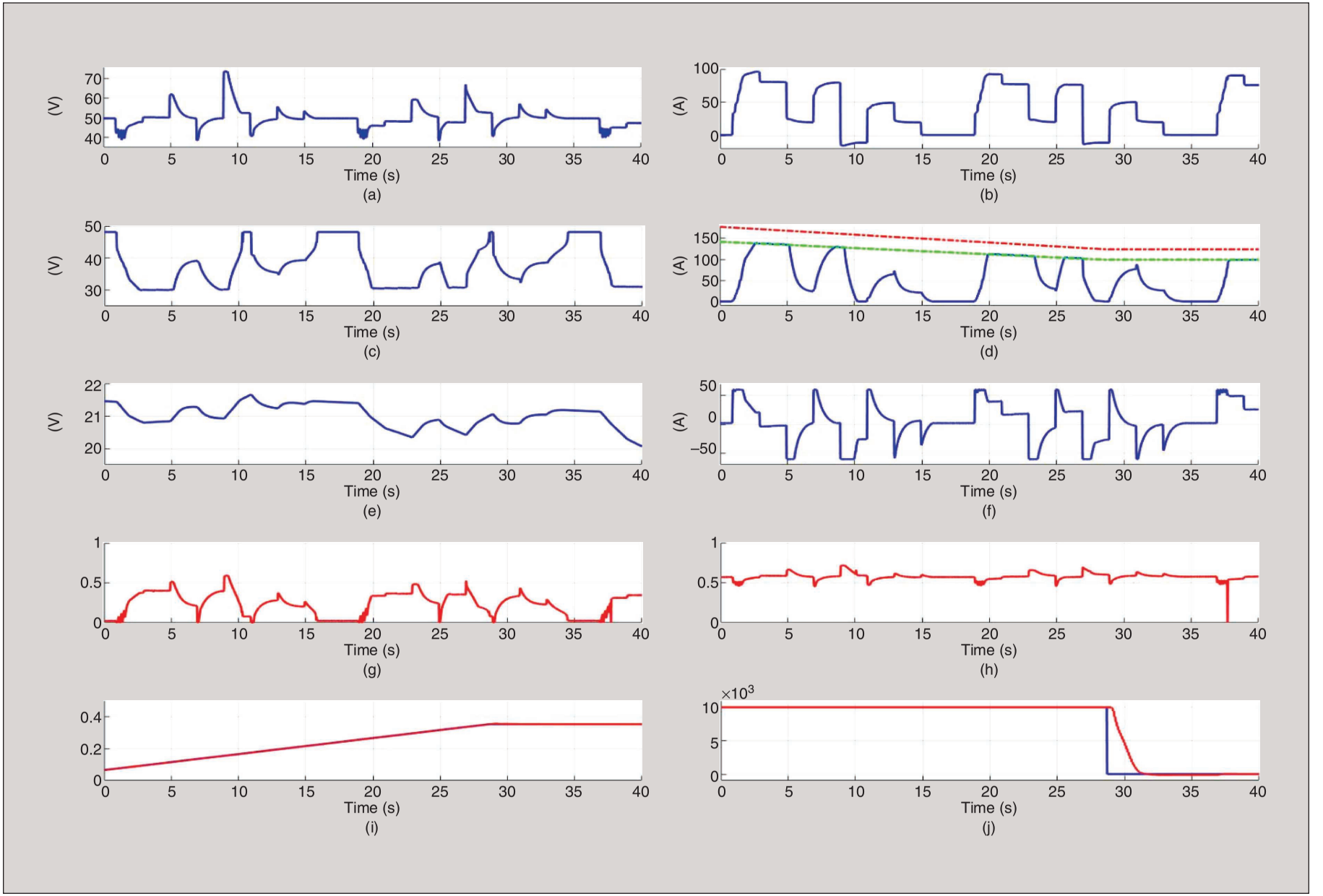

FIGURE 4 – The hybrid FC system HIL results: (a) dc bus voltage v_{bus}, (b) load current i_{load}, (c) FC voltage v_{fc}, (d) FC current i_{fc}, (e) SCs voltage v_{sc}, (f) SCs current i_{sc}, (g) duty cycle dc_{fc}, (h) duty cycle dc_{sc}, (i) FC SoH $\alpha(t)$ and $\hat{\alpha}[k]$, and (j) speed of degradation $\beta(t)$ and $(\hat{\beta}[k])$. SC: supercapacitor; SoH: state of health.

(blue curves) and in the NIOS II processor (red curves); these colors correspond to those chosen in Figure 3. Aging $\alpha(t)$ of the PEMFC, which has been emulated in the FC model, is estimated online ($\hat{\alpha}[k]$) by the PHM algorithm (here an extended Kalman filter) [14], [18]. The FC safety dynamic module computes the maximum FC current $(i_{fc})_{max}[k]$ value that must not be exceeded. Notice that the FC current i_{fc} is well controlled by the SoC FPGA-based controller since it does not exceed the defined maximum current fixed to 80% of $(i_{fc})_{max}[k]$ [see Figure 4(d)]. This means that both the speed of degradation $\beta(t)$ [see Figure 4(j)] and the aging $\alpha(t)$ [see Figure 4(i)] are well estimated by the observer implemented within the NIOS II soft-core processor [14].

Moreover, as the current controllers and peripherals implemented within the FPGA fabric (PWM, ADC) need to be tightly coupled, it appears that the soft-core processor is a valuable option to provide deterministic interrupt, minimum jitters, many possibilities of evolution, and it reduces the risk of obsolescence.

Dynamic Reconfiguration of PV Modules

Shadowing significantly affects PV arrays electrical power production and may lead to the conduction of the modules bypass diodes. Consequently, more than one maximum power point appears in the string power versus voltage (P-V) and current versus voltage (I-V) curves [19]. Depending on the actual shadowing pattern, the adoption of a system permitting change in the electrical connections among the PV modules through a suitable switching matrix [20] is useful. The reconfiguration has to be performed dynamically, because the shading pattern changes during the day, and in a short time interval during which the irradiance level received by the PV cells does not change significantly.

In [21], a theoretical analysis of the problem was proposed, and in [22], an evolutionary algorithm (EA) aimed at dynamically determining the best electrical configuration of the PV modules in a plant formed by more strings was presented.

SoC FPGA devices are not only able to manage complex algorithm online processing, but they can also help to accelerate their execution.

Figure 5 shows a fixed shadow affecting the PV array and two EA individuals, each corresponding to a specific electrical connection of modules, to form the two parallel connected strings. The green P-V curve corresponds to the static connection, showing a peak power lower than the one the EA determines and corresponding to the configuration with blue P-V curve.

The conjoint HW/SW SoC FPGA-based implementation [23] (Figure 6) consists of the core of the EA, implemented in SW on a bare metal ARM A9 core, and of the fitness function instances that are executed in a couple of dedicated intellectual property (IP) modules within the FPGA fabric. The 12-b fixed-point representation ensures a good tradeoff between the FPGA fabric-consumed area and the loss of accuracy, which is less than 1% than the reference case based on a 32-b floating-point representation. The fitness function IP module is written in C++ and the architectural design space is explored by using the HLS approach [24]. HLS allows to design the HW accelerator through high-level languages, for example, C/C++, by generating production-quality register transfer level (RTL) code that is optimized for the targeted FPGA. The synthesis process transforms automatically a C/C++ source code in an HW description language such as VHDL or SystemVerilog. HLS accelerates verification time over RTL by raising the abstraction level for FPGA HW design. HLS designs are typically verified at a speed that is orders of magnitude faster than RTL ones. The algorithm is preliminary optimized to put into evidence the subroutines to be run in parallel and, by using a counting sort algorithm, permits saving up to 80% of computation time with respect to the use of a standard bubble sort algorithm. The reduction in the size of the fixed-point divider leads to a 20% reduction in the latency of the fitness function.

Two practical cases, with 100 and 25 samples per module I-V curve, respectively, were implemented on the low-end, Zynq-based board (Zybo from Digilent) at an FPGA clock frequency of 125 MHz. The PV field has 24 modules divided in two parallel connected strings. The EA runs on a population of 48 individuals, for a maximum of 100 generations. The experiments revealed that, if 100 samples per curve are used, two fitness function HW accelerators can be integrated in parallel in the FPGA fabric. For the 25 samples per curve case, three IPs modules can be embedded. The acceleration rate for the 100 sample case is of 2.46 compared to an optimized full SW implementation based on a bare metal ARM A9 core running at 667 MHz, thus leading to a total execution time of 13.218 s. By comparison, the acceleration rate for the 25 sample case is of 2.80, with a total execution time of 2.374 s.

The Next Generation of Smart Controllers for Electrical Energy Systems

The electrical energy sector in Europe will be pushed by the European Union (EU) Green Deal [25] and the EU Recovery Plan [26], also in view of its integration with other energy sectors [27], [28] and with digital technologies for achieving the decarbonization goal.

We now discuss the significant contributions SoC FPGA can bring to the key future developments of renewable generators and hydrogen technology using the two applications presented in the previous section. SoC FPGA will facilitate meeting the EU expectations and targets in other fields, such as

battery management and diagnostic systems (see, for example, [29], [30]).

Monitoring and diagnostic functions will benefit from the decentralized high computational potential SoC FPGAs offer, enabled by the use of the model-based approach for PV systems [31] and even by running data-driven approaches (for example, [32] for FC applications and [33] for PV systems).

The smart power management area will also profit from SoC FPGAs, especially by introducing the controller digital twins (DTs) of the used static power converters. DTs have several benefits such as the possibility to make online diagnosis [34] or to study in detail the power losses of a complex

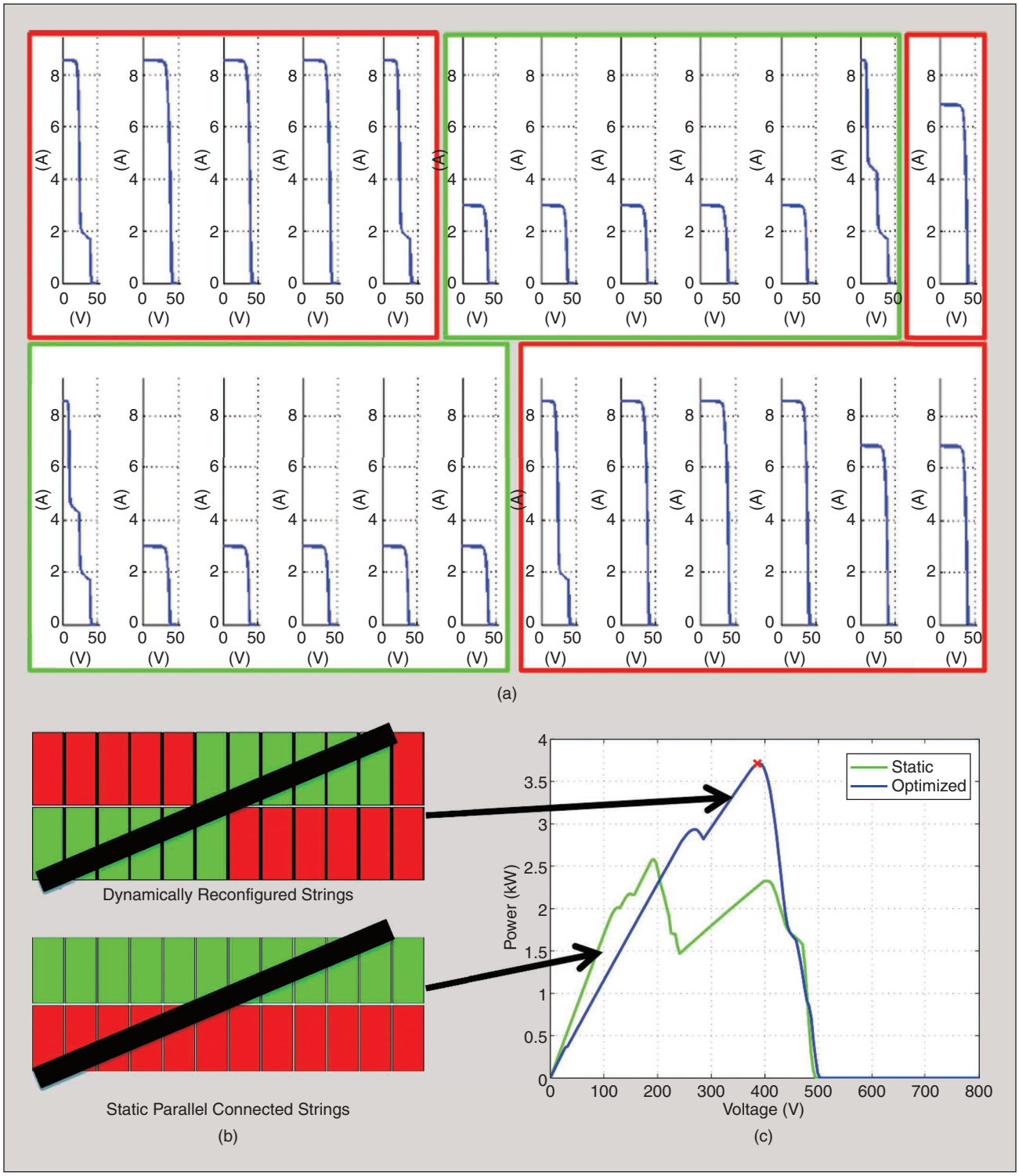

FIGURE 5 – The dynamic reconfiguration of a PV array of two parallel connected strings of 12 modules each. (a) The modules' I-V curves. (b) The strings affected by an oblique shadow. The green and red modules are series connected. (c) The P-V curves corresponding to the static and the reconfigured PV fields.

structure like a modular multilevel converter (MMC) [35]. Finally, the optimized economic dispatching of a microgrid is a good example of the ongoing mutation in terms of control algorithmic needs for modern complex electrical energy systems [36].

These recent works are good illustrations of what could be the next generation of smart controllers for complex electrical energy systems. Beyond the standard control functions (still implemented), these smart controllers will also include additional tasks like diagnosis, fault tolerant capabilities, optimization of the energy flow, and/or economical dispatching. These new functionalities can be gathered under the generic name of *smart monitoring*, and it is worth analyzing their impact on the architecture of smart controllers.

SoC FPGAs also offer a high level of flexibility in terms of microarchitecture.

In complex electrical energy systems, the first task for smart controllers is to collect and aggregate the measurements coming from all internal subelements. An analysis of references shows that three approaches are possible to cope with this problem. A typical approach is to use a standard serial communication like controller area network bus [29] between the low-end microcontroller that is in charge of the monitoring of a given cell and the centralized SoC FPGA-based smart controller. A second solution

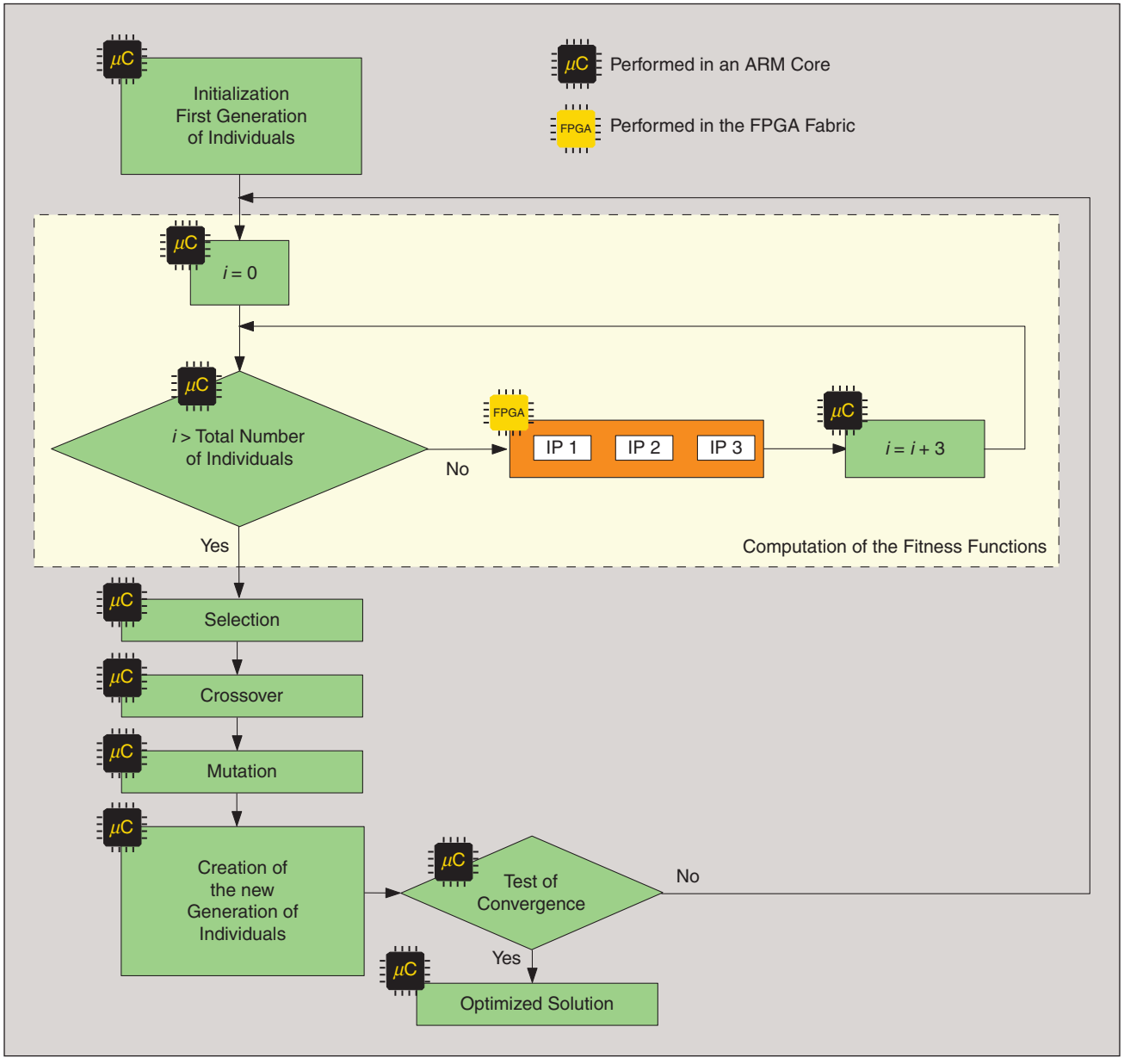

FIGURE 6 – The HW/SW implementation of the PV dynamic reconfiguration algorithm.

is to use a wireless connection (Wi-Fi or Bluetooth) [30], [31], since it offers more flexibility and scalability than a classical serial wired communication. Finally, a more radical approach is to integrate all the necessary front-end analog resources needed to measure and collect the data coming from the cells in an application-specified integrated circuit like that in [32], which also integrates the SoC FPGA-based smart controller. This solution is highly integrated but very specific and costly to design. However, and if, as expected, the market of the industrial IoT will be booming, one should expect SoC FPGA manufacturers to propose that future new devices include more analog capabilities than today. We are already seeing this with the Xilinx RF-SoC device, which is devoted to the 5G SW radio market [37].

The main tasks to be performed by the smart controller are diagnosis [31], [33], health monitoring [18], and energy management [23], [36]. Sometimes higher integration is the key objective [30], where the smart controller performs in parallel both battery management system and charger functionalities.

Depending on the time scale of these smart monitoring tasks, the controller has to apply hard real-time operating conditions (from microseconds to millisecond, with a full timing determinism, achieved by timer interruptions and with a bare metal configuration of the processor to minimize the latency) [18], [35], or soft real-time operating conditions (from seconds to hours when timing determinism is less critical). In this case, it is of great importance to execute the smart monitoring tasks as processes of a real-time OS like an embedded Linux [29], thus profiting from its communication facilities. Even when hard real-time operating conditions are mandatory, it is still possible to dedicate one core processor of the SoC FPGA to run a Linux OS, while the other one is bare metal and devoted only to the critical control tasks [38] ("asymmetric multiprocessing").

Regarding the nature of smart monitoring strategies, most are based on the simulation of a plant model [29]. Some of these approaches require an optimization problem that has to be solved online [23], [31], [36]. The rest of these studies, like those integrating a DT [34], [35], are based on estimators or observers [18]. However, whatever the smart controller has to execute, a stochastic optimization problem or an embedded DT, the computing load is high. Therefore, it is interesting to analyze how the HW/SW partitioning, which consists of choosing which parts of the control algorithm are implemented in a processor and which are implemented in an HW accelerator, is conducted; for the EA-based optimization, the main body of the EA is implemented in SW and the fitness function instances are implemented as HW accelerators [23], [31]. As for estimators and observers, the HW/SW partitioning is usually based on the dynamics of the model to emulate; a slow temperature estimator is naturally implemented in SW, while the battery state-of-charge estimator is done in HW [29]. In [35], because the submodule estimators of the MMCs are prone to parallelization, they are placed in the FPGA fabric. But in [34], a full FPGA implementation is performed, which results as the only choice due to the conjoint short dynamics of the emulated power converters and the complexity of the stochastic models used.

With the progress in machine learning methods, data-driven approaches are increasingly popular for the diagnosis of complex electrical energy systems. They concern classification [32] or regression techniques [33], both requiring a complex offline training process, but the online inference process may be relatively simple. However, in many neural network (NN) classification or regression problems, the trained NN is fed by new incoming data from the plant. This means that, unlike [33], the local smart controller has to implement an inferred NN. An inferred NN, as a simplified version of an optimally trained deep NN, has a reduced power and latency for meeting edge applications requirements. The deep NN is trained offline; then, through pruning and quantization methods, the groups of artificial neurons that rarely or never fire are removed and the numeric precision of the weights is reduced, so that a reduced model size and a faster computation are achieved at the cost of minimal reductions in predictive accuracy [39]. Based on the parallel characteristics inherent in such algorithms, an FPGA-based or GPU-based implementation is highly recommended [40].

The preceding overview reveals that most smart monitoring applications are implemented in an SoC FPGA device since these heterogeneous computing platforms reached very good computing performance and enable architecture customization thanks to the FPGA fabric. With the help of a real-time OS like embedded Linux, these devices are easily connectable to Internet so they are good candidates to handle one of the biggest mutations currently experienced in digital controllers—the transformation of the "local embedded controllers" into edge computing platforms (ECPs). So the aforementioned "smart controllers" are not only able to handle locally complex control functions and smart monitoring tasks, but they can also be part of a larger control system that distributes some tasks to a remote cloud computing platform (CCP). This transformation is directly derived from the industrial IoT concept [41]. The distribution of the tasks between the ECP and the CCP can be seen as an evolution of the embedded control concept, with smart monitoring tasks processed locally. However, in [33] and [36], a different philosophy has been proposed: all the prediction tasks are achieved in advance on an hourly/daily basis and the ECP only has to compare the information received from the plant with these predictions. Thus, the computing load is clearly moved remotely into a CCP and, as consequence, the ECP can remain very light, as in [36], where a single DSP chip is sufficient to implement a decision maker based on simple tests.

To conclude, the fact that SoC FPGA-based ECPs are able to collect

data from the cell unit controllers, use it locally to execute smart monitoring tasks, and interact with a CCP where hourly/daily training of NN is achieved or where other slow supervising and storage tasks are being performed, opens new interesting lines of research. One of them is the opportunity to enlarge significantly the size of the electrical energy systems to manage [36], where the same CCP can handle the economic dispatching forecasts for several microgrids. The next step will be to integrate the possibilities for cooperation between different electrical energy systems, but reinforcing the security and the privacy of the connections between the ECP and the CCP will be a concern. Finally, any complex electrical energy system can be monitored over its entire lifespan by sending and storing on a daily basis relevant data from an ECP to a CCP. A lot of effort has to be dedicated to this topic as part of the energy IoT future research.

Conclusion

SoC FPGA can make significant contributions to the key developments in complex electrical energy systems, especially those including renewable generators and those employing hydrogen technology. We detailed some advantages and limitations through the two specific applications presented in the case studies. One concerns a FC hybrid electric system controlled by passivity-based power management associated with an aging prognosis algorithm. The other reports on the SoC FPGA implementation of a control system able to optimize online the dynamical configuration of a partially shadowed PV field.

In addition to these two case studies, we also analyzed in detail a series of recently reported results on smart controllers for complex electrical energy systems, highlighting the importance of the increasing number of smart monitoring tasks performed by this new generation of controllers, for example, diagnosis, prognosis, fault tolerant capabilities, optimization of the energy flow, and/or economical dispatching.

SoC FPGA to easily communicate with both the system to be controlled and the remote cloud services.

Despite a number of limitations like the cost (that is costs higher than for other technologies like SoC DSPs), a limited analog interface (analog-to-digital, digital-to-analog), and a designer's longer learning curve for optimal use, SoC FPGA is one of the most promising digital technologies for implementing smart controllers. By investigating with care the implications in terms of implementation of these new smart monitoring tasks, we showed that SoC FPGA devices are not only able to manage complex algorithm online processing (such as an EA optimization or a DT), but they can also help to accelerate their execution by parallelizing into customized HW accelerators several computationally demanding subtasks like fitness function calculation.

Furthermore, thanks to their highly performing FPGA fabric, SoC FPGAs also offer a high level of flexibility in terms of microarchitecture. A good illustration of this is the possibility for the designer to add one or more simple SW core processors, thus relieving the device processing system of low-level time-consuming tasks.

Finally, we pointed out another important advantage—the ability of SoC FPGA to easily communicate with both the system to be controlled, thanks to a very large number of I/Os, and the remote cloud services, because it can easily embed a Linux OS. This makes an SoC FPGA-based smart controller a high-performing ECP that is able to address incoming challenges, in terms of complexity and storage, brought on by data-driven approaches.

Biographies

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