Tanmay Verma
+1 (979) 739-8070

Email : tanmay2592@gmail.com
LinkedIn : tanmayverma25

Education

- **Texas A&M University** — College Station, TX
  Master of Science in Computer Engineering; GPA: 3.80/4.00 — *Aug 2017 – May 2019 (Expected)*
  - **Ongoing Thesis**: Optimizing Neural Network training/inference on memory and power constrained systems
- **Indian Institute of Technology (BHU)** — Varanasi, India
  Bachelor of Technology in Electronics Engineering; GPA: 8.08/10.0 — *Aug 2011 – May 2015*

Skills

- **Programming Languages**: C/C++(CUDA, MPI, OpenMP, OpenCL), Assembly, Python, MATLAB, Verilog, Bash
- **Platforms**: NVidia K20 GPU, HPE Moonshot, Oracle Servers(x86 and SPARC), Xilinx ML510 and Raspberry Pi 3.0
- **Relevant Coursework**: Deep Learning, Machine Learning, Online Decision Making, Analysis of Algorithms, Artificial Intelligence, Computer Architecture, Parallel and Distributed Numerical Algorithms and Microprocessor System Design
- **Positions of Responsibility**: • **Teaching Assistant** for **Operating Systems** (CSCE 611) in Spring 2018 • Mentor for On-boarding Engineers at Oracle (2016) • **Technical Head** of Udyam 2015 (technical fest of ECE department at IIT)

Experience

- **DeepMap Inc.** — Palo Alto, California
  System Software Engineer Intern — *May 2018 - Aug 2018*
  - **Sensor Raw Data Record and Replay**:
    Implemented a complete framework to emulate physical sensors for testing the integrity and scalability of the **Data Collection API** without any hardware restrictions. The framework was successfully demonstrated on Xsens GPS/IMU and Velodyne LiDAR. *(C++, Operating Systems, Sensor Synchronization, Sensor Drivers, Virtualization, Bazel, Protocol Buffers and Google Testing/Logging/Style)*
- **Oracle Systems** — Bangalore, India
  Associate Software Engineer — *July 2015 - July 2017*
  - **Diagnostic Tests for x86/SPARC based Servers (Oracle Validation Test Suite)**:
    Developed **diagnostic tests** to stimulate and detect manufacturing/functional faults in Processor and Memory with an emphasis on power subsystem.
    Outperformed **Intel Power Thermal Utility** by **13.63%** on Oracle X7-2 based on Skylake Architecture.
    Integrated drivers with Oracle VTS to access/modify CPU MSRs for targetted testing and data collection for anomaly detection on manufacturing floor. *(C, Assembly, Operating Systems, Computer Organization and Architecture)*
- **Indian Institute of Science** — Bangalore, India
  Research Intern — *May 2014 - July 2014*
  - **Cognition Engine**:
    Prototyped a **Soft-Core Multiprocessor System-on-Chip** on Xilinx FPGA ML510 and programmed it to function as a classifier using **Radial Basis Function Neural Network** under the supervision of Prof. SK Nandy. *(C, FPGA Prototyping, Neural Network and Parallel Programming)*

Academic Projects

- **x86 Operating System (Spring 2018)**: Programmed a kernel for x86 with features including virtual memory, threading, device drivers and file system.
- **QR SVM on Texas Instruments Keystone II LPSoC (Fall 2017)**: Optimized the performance of QR based SVM training algorithm by offloading critical sections to DSP using openCL, openMP and MPI.
- **Gaussian Process Regression (Fall 2017)**: Developed a High-Performance scalable code for Gaussian Process Regression on a Supercomputer with Nvidia K20 GPU in CUDA.
- **Doppelganger Cache (Fall 2017)**: Obtained **1.51x** reduction in area while suffering only a 4.5% hit in performance by implementing Doppelganger Cache in **ZSim simulator** against the Precise Cache.
- **FFT Accelerator (Spring 2013)**: Prototyped 16-point radix-2 FFT generator/accelerator in FPGA using Verilog.

Publication

- **"A Flexible Scalable Hardware Architecture for Radial Basis Function Neural Networks"**: 2015 28th International Conference on VLSI Design, Bangalore, 2015, pp. 505-510.