Arm M-Series
Cyclic Executive
Anti-Lock Braking System (ABS)

Overview: The prompt for this homework assignment asks us to consider the Arm M series, decide which software architecture makes sense and finally consider the application of anti lock braking. However, this seems almost backwards. So we will instead assume that we want to design a very simple ABS. We will list the basic requirements for such a system. Select a micro processor for this system. And finally purpose a software architecture based on the requirements and the hardware selection.

ABS Requirements: The wikipedia articles, references [1], [2], and [3], listed below will be used as the source of requirements. A simple ABS system monitors the rotational speed of the wheels in comparison to each other and to the vehicle's velocity. If one wheel's rotational speed is significantly greater than that of the other, hydraulic valves are opened to increase the braking force applied to that wheel. Likewise if one or more of the wheels is spinning faster than the velocity of the vehicle indicates it should, its hydraulic valve is actuated, slowing it down. Both of these cases indicate a wheel is slipping and losing contact with the rode.

With the above rationale we can determine a few key requirements of such a system that can be stated to help us choose a processor and a software architecture.

1. A digital signal processor.
2. Digital / Analog converters
3. CAN bus interface to speak to system computer
4. Floating Point Arithmetic
5. Detect a failure case in Xms and acuate in Yms (hard time). X and Y would be determined by an automotive engineer who would calculate the optimal latency that could be safely tolerable in such a system.
6. Minimal jitter in response time.
7. Must be highly deterministic.

Processor Selection: The ARM website characterizes the ARM m series using the following description "The Cortex-M processor family is based on the M-Profile Architecture that provides low-latency and a highly deterministic operation for deeply embedded systems" [4]. This seems to be a good match with an ABS system. Moreover, looking at the M4 this seems to be a good fit by meeting our first four requirements. This chips data sheet is here [5]. The main reason to choose an M series over an R series is that an R series is significantly more complicated than that of the M series and provides more compute power and additional logic such as "lock step instructions". The M series is going to provide slightly more deterministic responses, and will be significantly easier to run formal verification, thus meeting safety requirements. Moreover, the increased compute power is needed in this use case.

Software Architecture: A cyclic executive is the obvious choice. The M series does not have a whole lot of compute power. The specific chip [5], only has 512KB of flash and 128KB of SRAM

and a max CPU frequency of 180Mhz, single core. However, even if compute power / memory space was not an issue, a cyclic executive would still be the move, because we are really only providing one service. Detect one of several failure cases and react. Complex logic is not needed nor is wanted as building a system where formal verification can be used with great accuracy is the main factor here. Thus a cyclic executive the obvious choice.

References:

1. https://en.wikipedia.org/wiki/Anti-lock_braking_system
2. https://en.wikipedia.org/wiki/Cadence_braking
3. https://en.wikipedia.org/wiki/Threshold_braking
4. https://developer.arm.com/ip-products/processors/cortex-m
5. https://www.google.com/url?sa=t&rct=j&q=&esrc=s&source=web&cd=&ved=2ahUKEwi0wOuqpMT1AhU0NX0KHbIHBqkQFnoECCgQAQ&url=https%3A%2F%2Fwww.st.com%2Fresource%2Fen%2Fdatasheet%2Fdm00035129.pdf&usg=AOvVaw2dS_lQjf32i5JFXlyT0e3r
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