Application Report
SLAA848–October 2018

System Design Guidelines for SimpleLink™ MSP432P4 Microcontrollers

Yu Liu, Chris Sterzik *MSP432 Applications*

ABSTRACT

The SimpleLink™ MSP432P4 microcontrollers (MCUs) are highly optimized, ultra-low power, wireless host MCUs with a high-precision ADC and extensive processing capabilities. Consequently, there are many factors to consider when creating a schematic and designing a circuit board. By following the recommendations in this design guide, you can increase your confidence that the board will work successfully the first time it is powered it up.

Contents

List of Figures

List of Tables

Trademarks

SimpleLink, MSP432, LaunchPad are trademarks of Texas Instruments.
Arm, Cortex are registered trademarks of Arm Limited.
All other trademarks are the property of their respective owners.

1 Introduction

This document contains system design guidelines for MSP432P4 MCUs. For a full list of MSP432P4 MCUs, visit SimpleLink Wired MCUs – Products. Section 3 contains design information that applies to most designs. Topics include important factors in the schematic design and layout of power supplies, oscillators, and debug accessibility. Section 4 describes the high-precision ADC and the unique considerations that are relevant to your design.

To further assist with the design process, Texas Instruments provides a wide range of additional design resources, including application reports and reference designs. See Section 5 and Section 7 for links to these resources.

2 Using this Guide

The information in this design guide is general enough to cover a wide range of designs by describing solutions for typical situations. However, because every system is different, it is inevitable that there are conflicting requirements and potential trade-offs, particularly in designs that include a high-performance precision ADC, radio frequencies, high voltages, or high currents. If your design includes these features, then special considerations beyond the scope of this application report may be necessary.

Where possible, the distinction is made between *preferred practice* and *acceptable practice*. This distinction addresses the reality that constraints such as size, cost, and layout restrictions do not always allow for best-practice design.

When considering which practices to apply to a design, one of the most important factors is the pin switching rate and current.

NOTE: Some of the information in this guide comes directly from the individual MSP432P4 microcontroller data sheets. The microcontroller data sheets are the defining documents for device use and contain specific requirements that are not covered in this design guide. Always use the most current version of the data sheet and also check the most recent errata documents for the part number you have selected. Visit www.ti.com/msp432 to sign up for email alerts specific to a MSP432P4 part number.

3 General Design Information

The MSP432P4 family includes a number of different size and package variants and is also a very flexible MCU, with a number of peripherals. This section describes different package types and the general or common analog and digital circuits across the MSP432P4 product family.

3.1 Package Footprint

The MSP432P4 product family has three different package offerings, LQFP, nFBGA, and VQFN (see Table 1). For the smaller nFBGA and VQFN packages, some of the peripherals are unavailable or only a subset is available. The LCD, for example, is available only in the LQFP (100-pin) package of the MSP432P4111. Similarly, the ADC has 24, 16, and 12 channels available for the LQFP (100-pin), nFBGA (80-pin), and VQFN (64-pin) packages, respectively. In addition to size and function, the packages offer different thermal characteristics. The VQFN has a thermal pad that should be connected to DVSS. Finally, the nFBGA introduces routing and PCB requirements that increase system cost, which is another factor to consider in package selection.

Table 1. MSP432P4 Package Details

Package	MSP432P401R	MSP432P4111, MSP432P4111T	Pins	Approximate Size	$R\theta_{JC}$ (°C/W)
LQFP	✓	✓	100	14 mm × 14 mm	27.2
nFBGA	✓		80	5 mm × 5 mm	22.6
VQFN	✓	✓	64	9 mm × 9 mm	8.3

When creating PCB footprints for a particular package, use the IPC-7351 standard along with the package information found in both the data sheet and in SMT and packaging application notes. For BGA packages, the nominal ball diameter is used as a reference for the landing pad size and solder mask opening for each ball pad. For QFP and QFN packages, the maximum and minimum dimensions of the package and leads along with standard tolerances are used to calculate the pad size and locations.

As an alternative to creating the footprint, PCB layout footprints for the different packages are also provided on the TI website (for example, in the MSP432P401R product folder). These symbols are provided in a .bxl format associated with Ultra Librarian (UL). The bxl files include both the symbol and footprint for the associated package. The UL Reader can move the bxl components and their attributes to virtually any EDA CAD or CAE format.

3.1.1 BGA Package Considerations

The BGA package is the most challenging of the three packages in terms of routing. The rest of this section describes routing requirements and provides a routing example to help with layout of the BGA package.

The BGA package for the SimpleLink MSP432P4 MCUs is a 9×9 array of balls with 0.5-mm pitch. The ball at coordinate C3 is not populated, so the package provides 80 signals. Routing 80 signals makes "escaping the BGA" a challenge. A common practice to address this congestion is the use of blind and buried vias that can often be cost prohibitive. Figure 1 shows that it is possible to escape the BGA without the use of blind or buried vias, but this method requires smaller traces and spacing, which can increase board cost.

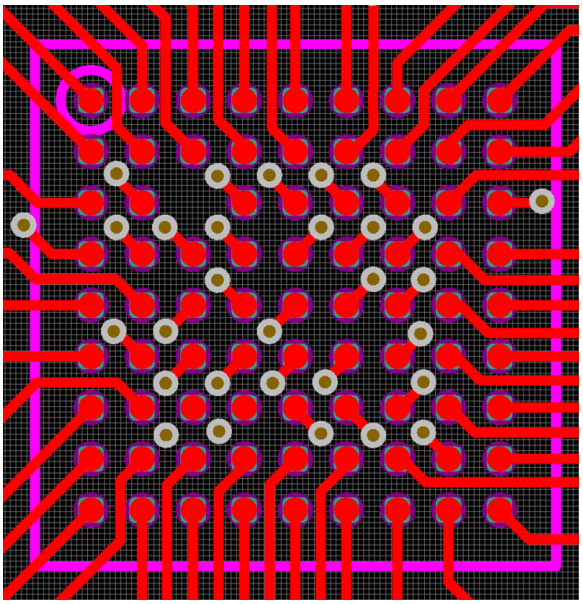


Figure 1. Top Layer of Example BGA Escape Routing

The rules in Table 2 are specified in PCB Design Guidelines for 0.5mm Package-on-Package Applications Processor, Part 1 and used in Figure 1.

Table 2. PCB Dimensions

Pad (NSMD)	Pitch	500 µm (≈ 20 mil)
	Size	250 µm (≈ 10 mil)
Mask	Shape	Round
	Opening	50 µm around pad (350 µm antipad for the 250 µm pad)
	Web	150 µm
Via	Pad size	254 µm
	Drill size	127 µm (5 mil)
Trace	Width	82 µm (≈ 3.2 mil)
	Pad to via length	354 µm pad center to via center
Clearance	Pad to trace	82 µm (≈ 3.2 mil)
	Pad to via	127 µm (5 mil)

PCB Design Guidelines for 0.5mm Package-on-Package Applications Processor, Part 1 states "Since there is only enough space to route one trace between vias, this strategy requires an additional routing layer for every inner row of solder pads after the fourth row."

In this example, the center signals D6, E5, and F5 are AVSS2, AVSS3, and AVSS1, respectively. Additionally, DVSS is found in locations E6 and C7. These power and ground pins can be easily connected to the internal power planes of a 4-layer board through a via. These connections avoid the need to add additional signal layers in addition to what is provided on the top (see Figure 1) and bottom (see Figure 2).

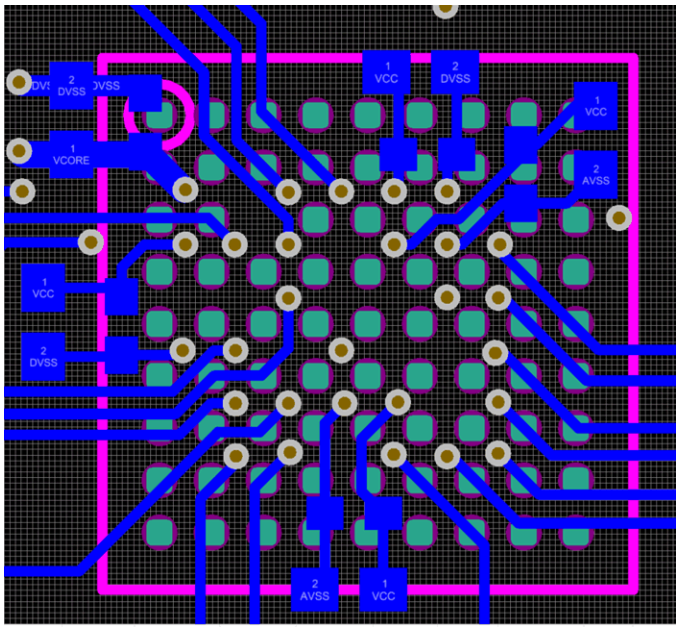


Figure 2. Bottom Layer of Example BGA Escape Routing

3.2 PCB Stackup

An important component of any layout is determining what PCB stackup to use. The PCB stackup configuration determines several elements of the design:

- Number of layers available for routing
- Number of layers available for power and ground planes
- Single-ended trace impedance, capacitance per inch and propagation delay per inch of a trace of a particular width. These factors are important for longer trace lengths (typically longer than 6 inches) on critically timed interfaces or on interfaces that are near the maximum capacitive load.

3.2.1 Four-Layer Stackup

A 4-layer stackup (2 signal layers and 2 power planes) is recommended for most designs. A 4-layer stackup has the following benefits:

- Low-impedance power and ground connections to components and decoupling capacitors through the planes.
- High-speed signals have lower impedance, smaller propagation delay and more immunity to crosstalk due to the closer distance to the reference plane on a 4-layer design as compared to a 2-layer design.
- Analog signals have more immunity to crosstalk, and the analog modules in the device can provide higher precision results when used with the solid ground plane reference that a 4-layer stackup provides.

Figure 3 shows a typical configuration for an FR-4 0.062-in (1.5748-mm) circuit board with 4 layers of 1-oz copper.

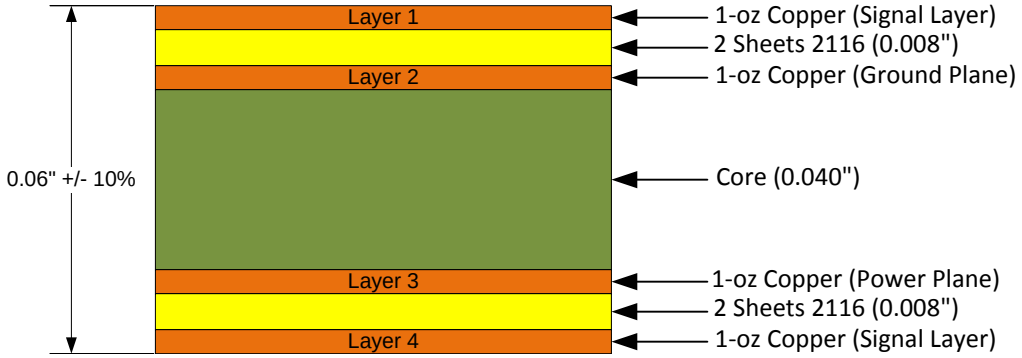


Figure 3. Typical 4-Layer PCB Stackup With Routing Assignments

For this example, a solid ground plane is on layer 2 and a power plane is on layer 3. The outer signal layers each consist of 1/2-oz base copper with 1/2-oz plating to total 1-oz copper. Each 1-oz copper layer is 1.4 mil (.0014 in or 0.0355 mm) thick. The height of traces above the ground plane is defined by the thickness of the PCB prepreg material; in this case, 0.008 in (0.2032 mm) thick. Therefore, total thickness is:

Total thickness = 0.062 in = 4 × 0.0014 in + 0.040 in + 2 × 0.008 in

3.2.2 Two-Layer Stackup

A 2-layer stackup is acceptable if the design allows for adequate power and ground routing with good decoupling placement and ESD protection.

Figure 4 shows a typical configuration for an FR-4, 0.062-in (1.5748-mm) circuit board with 2 layers of 1-oz copper (no plating).

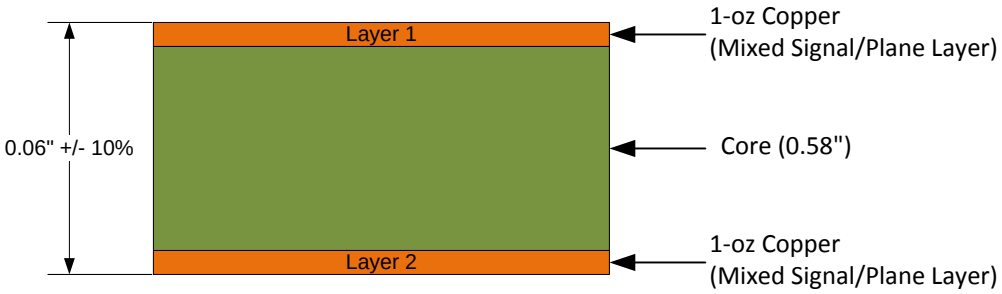


Figure 4. Typical 2-Layer PCB Stackup With Routing Assignments

For this example, the top and bottom layers are used for both signal routing and copper power floods. The 1-oz copper mixed plane is 1.4 mil (.0014 in or 0.0355 mm) thick. The height of traces above any ground pour is defined by the thickness of the PCB core material; in this case, 0.058 in (1.4732 mm) thick. Therefore, total thickness is:

Total thickness = 0.061 in = 2 × 0.0014 in + 0.058 in.

3.3 General Layout Design Choices

There are a number of layout design choices that can affect PCB fabrication cost, assembly costs, and operational reliability. This section describes some of these choices and the thoughts behind them including recommended trace width and spacing as well as via sizes based on the different packages and PCB fabrication costs.

3.3.1 Trace Width and Spacing

Trace width and spacing impact the design in many ways. The minimum trace width and space on the

PCB are two factors defining the cost of the PCB, and they are highly dependent on the capabilities of the PCB manufacturers. A large number of PCB manufacturers can produce boards with a minimum width and spacing of 3 mil (0.1016 mm) and a maximum 1-oz. finished copper weight on the outer layers.

As a general guideline for low volume production, there is a cost increase for a minimum width/spacing less than 7 mil (0.1778 mm).

For different packages, different trace widths can be used depending on costs and other factors listed above. These factors are some of the reasons why 7-mil trace width and space are recommended for routing I/O signals from the QFP packages. The BGA package is more dense and requires the 3.2-mil (0.082-mm) trace and space rules to route the I/Os from that package. Route power and ground nets with the wider and lower-impedance traces wherever possible. Accordingly, trace width routes must be 10 mil (0.2540 mm) or wider from decoupling caps and for main power nets and 7 mil (0.1778 mm) or 10 mil (0.2450 mm) from the QFP power pins. For the BGA, it is recommended to route using a 3.2-mil trace for only a short distance until a wider 7-mil or 10-mil trace can be used.

When routing a signal that is going to be used as a fast-edge-rate clock, provide two times the spacing requirement from adjacent signals where possible to reduce crosstalk to and from the clock net. For example, if routing with a 7-mil wide trace and space rule, make sure there is 14-mil spacing between the clock and adjacent signals.

3.3.2 Via Sizes

PCB manufacturers can vary in their capabilities for providing through-hole vias. The via size is often limited by the smallest mechanical drill the manufacturer uses. The minimum via pad size is usually required to be the drill size plus an additional adder called the annular ring. Drill size plus 8, 10, or 12 mil (annular ring of 4, 5, or 6 mil) are common pad sizes for very small vias (10-mil hole range). A recommended practice is to specify the annular ring to be as wide as the trace going into the via.

The amount of the adder is related to the IPC-6012 class of inspection requested by the customer and annular ring requirement of the customer. Boards fabricated and inspected with the IPC-6012 Class 2 requirement allow for one void per hole in not more than 5% of the holes. Boards fabricated and inspected with the IPC-6012 Class 3 requirements allow for no voids per hole. A PCB manufacturer usually requires a larger adder for Class 3 boards. A PCB manufacturer maintains a minimum annular ring, typically 1 mil, around each via hole, but the customer could choose to allow tangency where the hole is up to the edge of the pad but "breakout" has not occurred. This method can allow for a smaller diameter via pad if needed.

Table 3 lists some common via sizes along with some of characteristics calculated using the Saturn PCB Toolkit.

Table 3. Via Sizes and Properties

Via Type	Via Pad Size (mil)	Drill Size (mil)	Via Height (mil)	Reference Plane Opening Diameter (mil)	E_R	Via Capacitance (pF)	Via Inductance (nH)	Via Resistance (mΩ)	Via Impedance (Ω)	Notes
16D6	16	6	62	24	4.3	0.75	1.49	2.08	44.48	Small, lower capacitance but higher resistance via. Some PCB manufacturers do not accommodate this size. Useful for tight spaces and dense routes.
18D8	18	8	62	26	4.3	0.85	1.40	1.62	40.63	The largest via pad size (18 mil) that can be used to break out route of the BGA package with 4-mil spacing. Pad size is 10 mil over drill size of 8.
18D9	18	9	62	26	4.3	0.85	1.36	1.46	40.01	The largest via pad size (18 mil) that can be used to break out route of the BGA package with 4-mil spacing. Pad size is 9 mil over drill size of 9.
20D10	20	10	62	28	4.3	0.94	1.33	1.32	37.57	A standard via pad size (20 mil) that is 10 mil over the drill size of 10. Good for vias for power traces and general I/O traces. Achievable by a large number of PCB manufacturers.
22D10	22	10	62	30	4.3	1.03	1.33	1.32	35.81	A standard via pad size (22 mil) that is 12 mil over the drill size of 10. Good for vias for power traces and general I/O traces. Achievable by an even wider number of PCB manufacturers.

3.3.3 Trace Routing

3.3.3.1 90° Corners in PCB Traces

For many years, it has been common PCB design practice to avoid 90° corners in PCB traces. In fact, most PCB layout tools have a built-in miter capability to automatically replace 90° angles with two 45° angles.

The reality is that the signal-integrity benefits of avoiding 90° angles are insignificant at the frequencies and edge-rates seen in microcontroller circuits (even up to and past 1 GHz/100 ps) (see *High-Speed Digital Design: a Handbook of Black Magic*, ISBN 978-0133957242).

Additionally, one report could find no measurable difference in radiated electromagnetic interference (EMI) (see *Right Angle Corners on Printed Circuit Board Traces, Time and Frequency Domain Analysis*).[9]

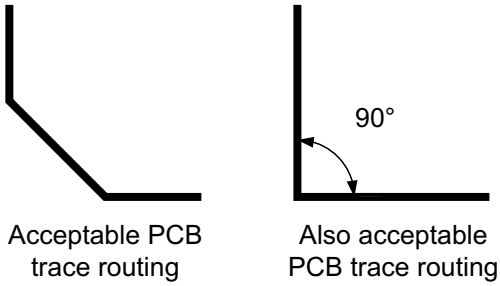


Figure 5. Acceptable PCB Trace Routing

NOTE: Loops in PCB traces are not acceptable, despite the references that indicate that the signal integrity benefits of avoiding 90° angles is negligible. Loops in traces form antennas and add inductance. The data shows that if your layout does have antenna loops, then mitering the angles to 135° is not going to help. Avoid loops in PCB traces.

Despite these conclusions, there are a few simple reasons to continue to avoid 90° angles:

- There is a higher possibility of an acid-trap forming during etching on the inside of the angle (especially in acute angles). An acid trap causes over-etching which can be a yield issue in PCBs with small trace widths.
- Routing at 45° typically reduces overall trace length. This practice frees board area, reduces current loops, and improves both EMC emissions and immunity.
- It looks better. This consideration is an important factor for anyone who appreciates the art of PCB layout.

3.3.3.2 Routing Across Plane Splits

Avoid discontinuities in ground planes and power planes under high-speed signals (see Figure 6). For all signals, a break in the ground plane removes a direct path for any return current to flow through. Therefore avoiding ground and power plane discontinuities under signals is recommended for all signals, even for balanced differential pairs.

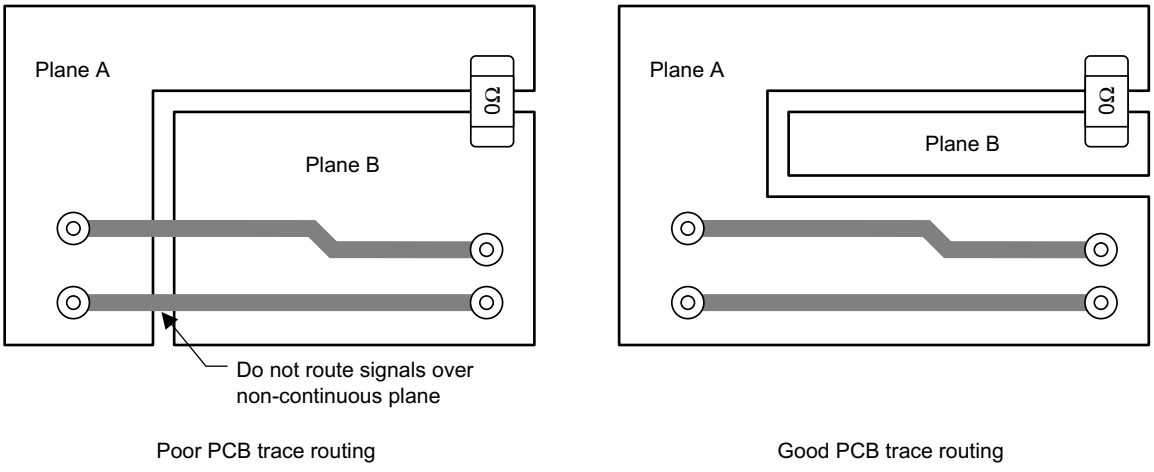


Figure 6. Examples of PCB Trace Layout

MSP432P4 microcontrollers provide high drive strength (20 mA) on four pins, P2.0 to P2.3. When initially evaluating the design, enable the high drive strength for these output pins if they are used for a high-speed interface to avoid any marginal timing caused by a drive strength that is too low. However, if a signal has signal integrity issues such as ringing and reflections, you can lower the GPIO drive strength to improve the performance as long as timing requirements are still met.

Do not run differential signal traces such that they cross a plane split (see Figure 7 and Figure 8). A signal that crosses a plane split can cause unpredictable return current paths and result in an impedance mismatch, which can affect signal quality and create EMI problems. Figure 9 shows proper routing, in which the traces go around the ground plane, which leads to better signal integrity.

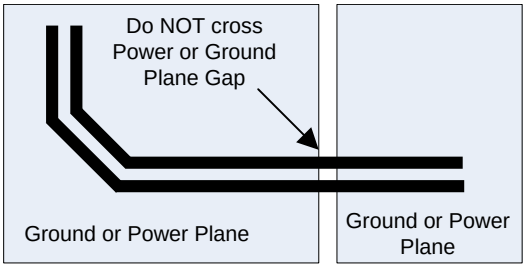


Figure 7. Differential Signal Pair Plane Crossing

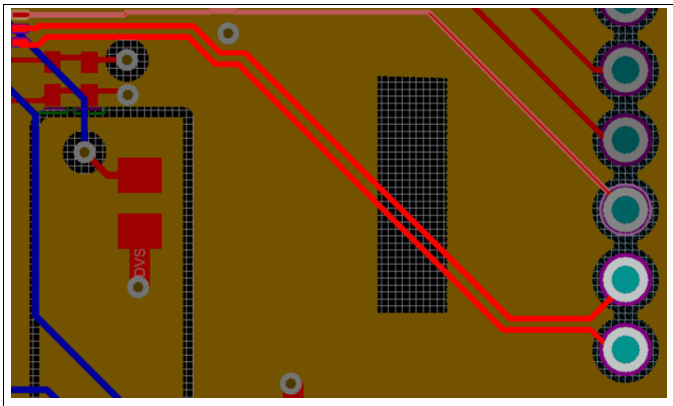


Figure 8. Poor Differential Signal Pair Plane Crossing

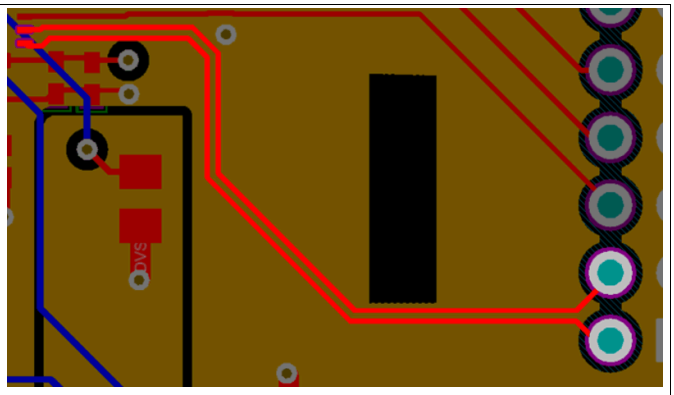


Figure 9. Improved Differential Signal Pair Plane Crossing

Figure 10 shows a general routing of single-ended traces as a poor example, and Figure 11 shows the recommended routing configuration for better noise immunity.

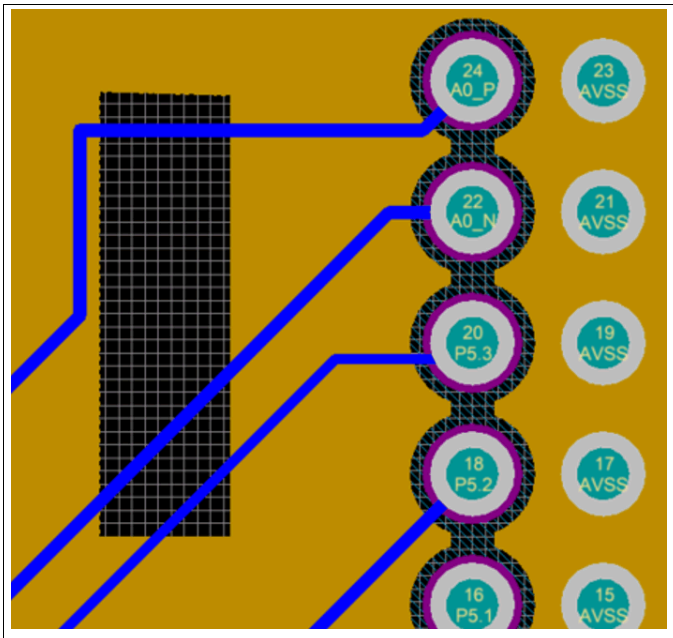


Figure 10. Poor Trace Routing Through Plane Split

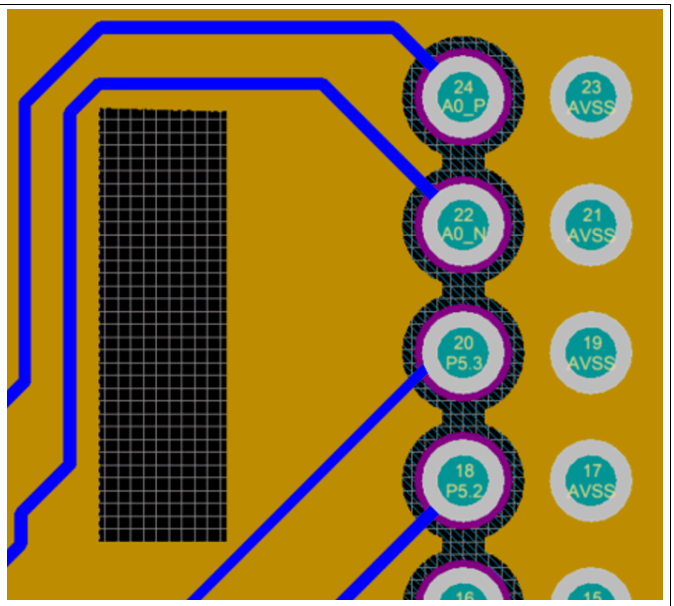


Figure 11. Good Trace Routing Through Plane Split

3.3.3.3 Routing Differential Traces

Differential traces are recommended when high levels of noise are present such as in analog signals. Differential traces are more immune to noise and provide a more stable reading. Follow these recommended guidelines:

- For each differential pair, run the traces within the pair parallel to each other and match the trace lengths. Matched lengths minimize propagation delay differences and avoid an increase in common-mode noise and increased EMI (see Figure 12). Figure 13 shows a poor example of routing differential traces with issues including 90° corners and poor parallelism. This configuration leads to an increase in noise and causes undesired results. Figure 14 shows the correct way to route, making sure the two traces are as close as possible and matched in length.
- If it is impossible to maintain parallelism immediately near the connector, ESD component, or microcontroller, minimize the distance the traces are not parallel and keep the nonparallel sections near the beginning or end of the traces.
- Ideally, there should be no crossover or via on the signal paths. Minimize vias, because they present impedance discontinuities. Route an entire trace pair on a single layer if possible.
- Choose ESD components in packages that support good differential routing of the signals that they protect without the need for stubs or vias. Many packages have no-connect pins that allow routing of the differential signal through the protection circuit and a no-connect pin to maintain signal spacing.

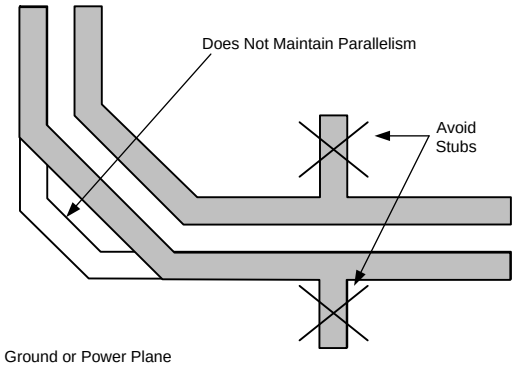


Figure 12. Differential Signal Pair

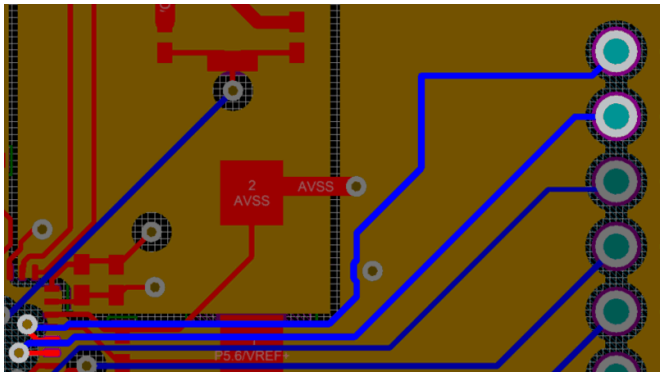


Figure 13. Poor Differential Pair Routing

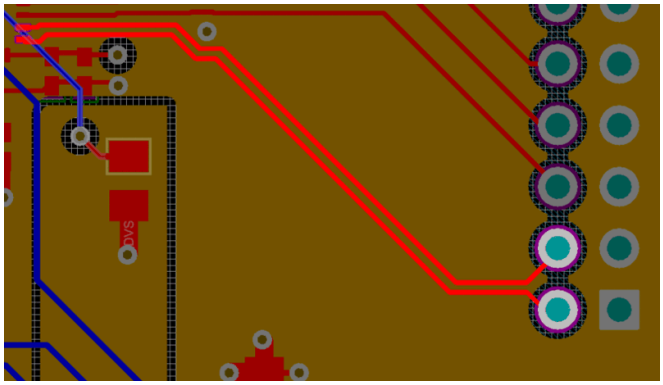


Figure 14. Improved Differential Pair Routing

3.3.4 Copper Pours

While solid ground and power planes are highly desirable, use small areas of copper pour cautiously. It is often not a good idea to pour every available area on the routing layers of multi-layer boards. Figure 15 shows the recommended ground plane layout of analog ground (AVSS) and digital ground (DVSS). AVSS is separated from DVSS. Design the precision analog ground so that an absolute minimum current flows through the two grounds.

On 1- and 2-layer board designs, multiple pours can be necessary, because dedicated plane layers are not available. If using small copper pours, never leave them floating or unconnected. Isolated conductor areas can cause unwanted coupling and EMC problems if they act as antennas. Small copper pours must have solid connections to a ground net or trace. Ideally, use several vias to provide a low-impedance connection.

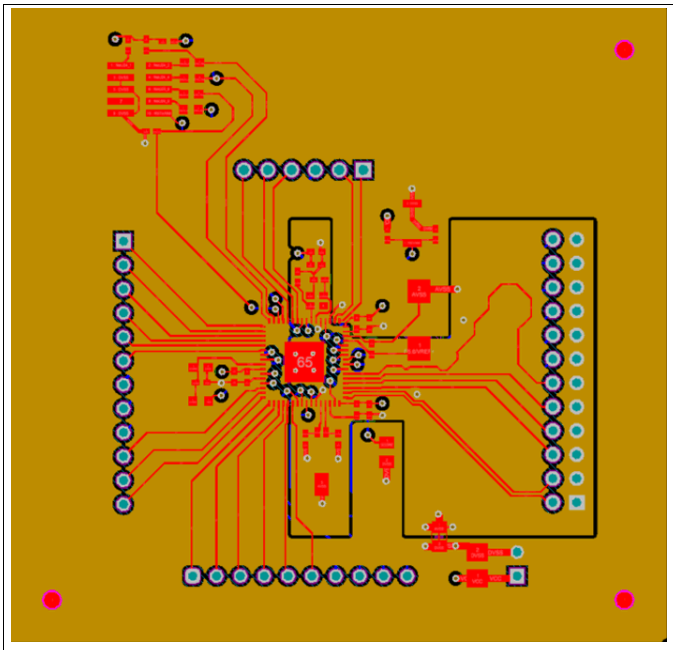


Figure 15. DVCC and AVCC Ground Plane

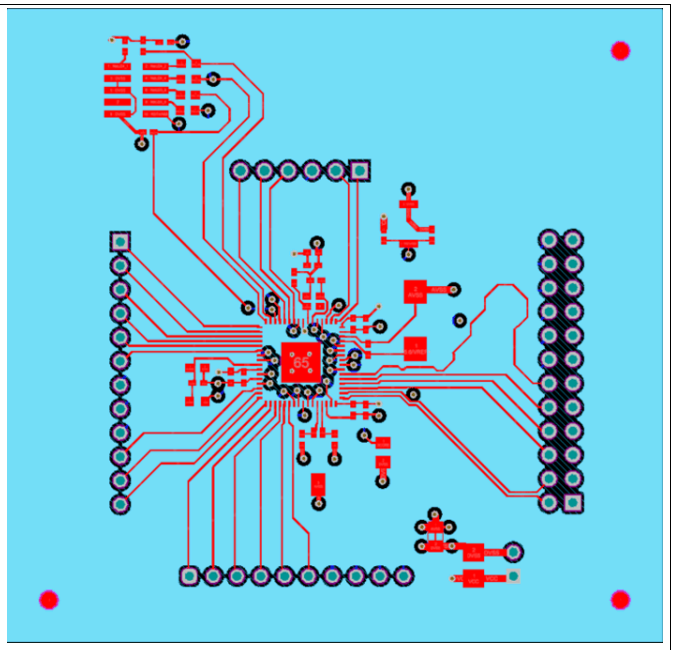


Figure 16. Power Plane

3.3.5 Chassis Ground

When properly designed, a chassis ground routed on the PCB can be a very effective feature for addressing a range of EMC challenges.

One specific benefit is improved electro-static discharge (ESD) immunity due to the provision of a safe discharge path that avoids sensitive circuitry in the center of the board.

In general, a chassis ground on the PCB works in conjunction with the overall enclosure to improve electro-magnetic emissions and especially immunity.

The chassis ground must be routed or poured copper around the perimeter of the PCB, ideally on all layers. If the ground is not present on all PCB layers, then other layers must be pulled back from the chassis ground to avoid coupling. The chassis ground must not route over the top of any power or ground layer.

Typically, the chassis ground must have a break or void in it to prevent loops that could cause loop antenna effects. However, depending on the size of the board, enclosure design, and ground connection point locations, a continuous chassis ground around the board can be acceptable or preferable.

3.4 Power

This section describes design considerations related to the microcontroller power supply.

3.4.1 Microcontroller Power Supply

MSP432P4 microcontrollers require only a single 3.3 V power supply connected to V_{CC}. It is recommended that AVCC and DVCC are powered from the same source. Other supply rails are generated internally by on-chip low-drop-out (LDO) regulators.

During normal microcontroller operation, the power-supply rail must remain within the electrical limits listed in the data sheet [V_{CC} (min) and V_{CC} (max)]. For optimal performance of the on-chip analog modules, the supply rail must be well regulated and have minimal ripple. This can be achieved by selecting the optimal decoupling capacitor values as recommended in the data sheet. A separate supply rail is also recommended for electrical noise sources such as motor drivers, relays, and other power-switching circuits, especially if analog-to-digital (ADC) performance is a factor.

The microcontroller has power-on reset (POR) and reboot reset circuits that perform a complete initialization of the application settings and device configuration information. The microcontroller also has Hard Reset which resets all modules that are set up or modified by the application and Soft Reset which resets only the execution component of the system remaining nonintrusive to all other peripherals and system components. Details on the operation and threshold levels of these circuits can be found in the device-specific data sheet listed in Section 7.

The supply connected to V_{CC} must accommodate a short period of additional inrush current that occurs as the decoupling capacitors connected to the V_{CC} rail of the LDO charge up to the V_{CC} voltage level. Internal circuitry limits the inrush to the I_{INRUSH}(max) specified in the data sheet. The supply connected to V_{CC} can self-limit the current it supplies to something less than the maximum I_{INRUSH}; however, self-limiting extends the time it takes to bring V_{CC} up to operating voltage. External supervisors can also be used to assert the external reset signal $\overline{RST}$ under power-on, brownout, or watchdog expiration conditions.

3.4.2 Core Voltage (V_{CORE}) Components

All MSP432P4 microcontrollers have both LDO and DC/DC regulators that can be configured to provide power to the core. The LDO voltage regulator requires a filter capacitor to operate properly, while the DC/DC requires both a capacitor on the VCORE pin and an inductor between the VSW and VCORE pins. See Table 4 or the *Recommended External Components* section in the device-specific data sheet for the acceptable capacitor and inductor value range.

Table 4. Recommended Component Values for Regulator Selection

			MIN	NOM	MAX	UNIT
C_{VCORE}	Capacitor on VCORE pin	For DC/DC operation, including capacitor tolerance	1.54	4.7	9	µF
		For LDO-only operation, including capacitor tolerance	70	100	9000	nF
L_{VSW}	Inductor between VSW and VCORE pins for DC/DC		3.3	4.7	13	µH

Follow these recommendations to place and route the capacitors connected to VCORE and the inductor between VSW and VCORE.

- Split the capacitance into two values so that total capacitance does not exceed the 9-µF maximum for either LDO or DC/DC modes of operation.
- Make the traces short and wide. See Section 3.1 for an example of how to do this with the BGA package

3.4.3 Decoupling Capacitors

Ideally, MSP432P4 microcontrollers have a combination of a 4.7-µF plus a 100-nF low ESR ceramic capacitor to each AVCC and DVCC pin (see Figure 17)

Higher-value capacitors can be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple. For optimal performance, place one decoupling capacitor adjacent to each V_{CC} power and ground pin pair. At a minimum, there must be one decoupling capacitor on each side of the microcontroller package connected between V_{CC} and ground.

Packages that support VREFA+ and VREFA- have specific decoupling requirements as defined by $C_{VREF\pm}$ in the data sheet (see REF_A in the device-specific data sheet for additional details).

The capacitance of most ceramic capacitors decreases with increasing voltage. Avoid using capacitors at close to their rated voltage unless reduced capacitance is acceptable. X7R capacitors can lose 15% to 20% of their capacitance at rated voltage, while Y5V capacitors can drop 75% to 80%.

Figure 18 shows different options for routing QFP PCB traces between the MSP432P4 microcontroller power pins and a decoupling capacitor.

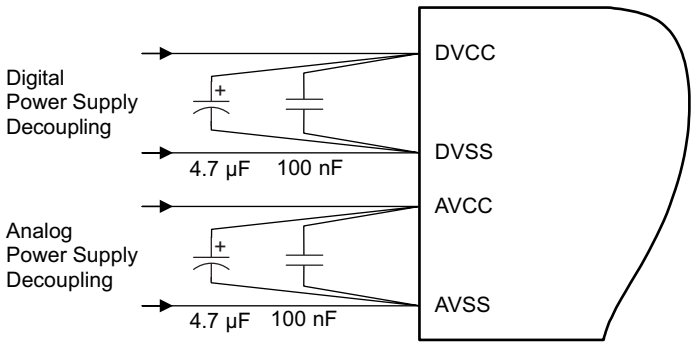
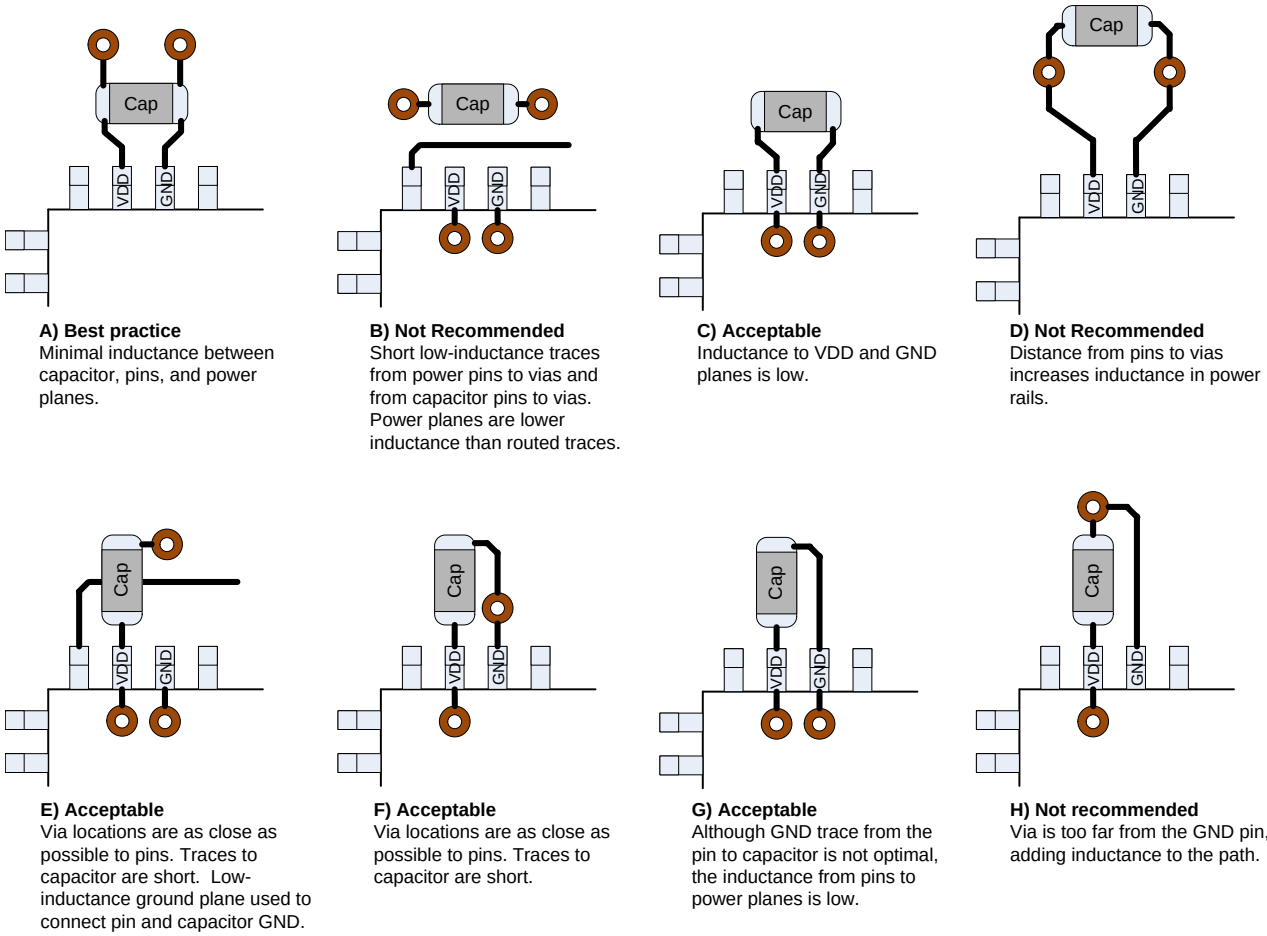


Figure 17. Power Supply Decoupling



A) Best practice
Minimal inductance between capacitor, pins, and power planes.

B) Not Recommended
Short low-inductance traces from power pins to vias and from capacitor pins to vias. Power planes are lower inductance than routed traces.

C) Acceptable
Inductance to VDD and GND planes is low.

D) Not Recommended
Distance from pins to vias increases inductance in power rails.

E) Acceptable
Via locations are as close as possible to pins. Traces to capacitor are short. Low-inductance ground plane used to connect pin and capacitor GND.

F) Acceptable
Via locations are as close as possible to pins. Traces to capacitor are short.

G) Acceptable
Although GND trace from the pin to capacitor is not optimal, the inductance from pins to power planes is low.

H) Not recommended
Via is too far from the GND pin, adding inductance to the path.

Figure 18. QFP PCB Routing Options

3.4.4 Splitting Power Rails and Grounds

TI recommends powering AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in the *Absolute Maximum Ratings* of the data sheet. Exceeding the specified limits can cause malfunction of the device. Additionally, TI recommends separated grounds with a single-point connection for better noise isolation from digital-to-analog circuits on the board and for high analog accuracy. Depending on the design, this can be done through a net tie (see Figure 19) or a 0-Ω resistor.

Some applications can justify separation of DVCC from AVCC to allow insertion of a filter to improve analog performance. Before deciding to split these power rails, the power architecture of the device must be reviewed to determine which on-chip modules are powered by each supply. Filter options include filter capacitors in conjunction with either a low-value resistor or inductor (or ferrite bead) to form a low-pass filter.

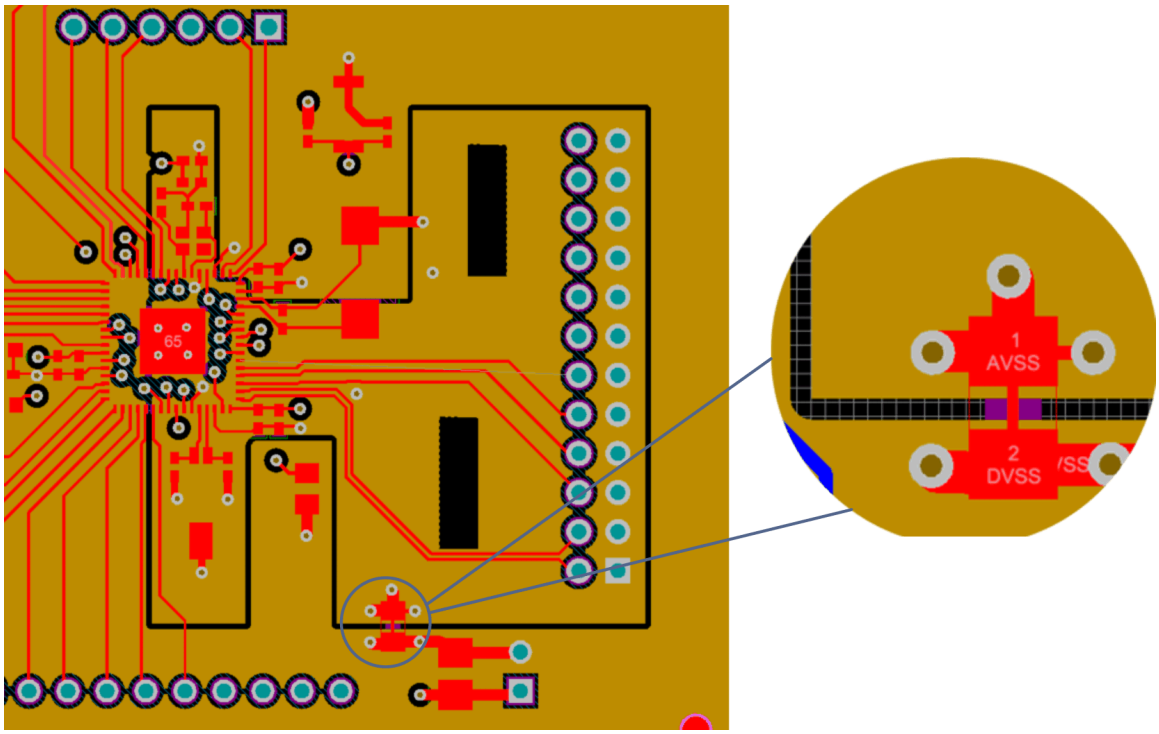


Figure 19. Net Tie

3.4.5 Analog Voltage Reference

Software can configure the voltage reference pins as either inputs or outputs. VREFA+ and VREFA- are the nomenclature for voltage outputs, while VeREF+ and VeREF- are for voltage inputs. The internal voltage reference peripheral (VREF_A) supports three selectable voltage levels of 1.2 V, 1.45 V, and 2.5 V, which can be output to the VREFA+ and VREFA- pins. The input range of VeREF+ is 1.45 V to AVCC.

When using an external reference (ADC14VRSEL = 1110b or 1111b), TI recommends connecting VeREF- to onboard ground as shown in Figure 20. Place decoupling capacitors as close as possible to the device, and make the traces a minimum length and maximum width.

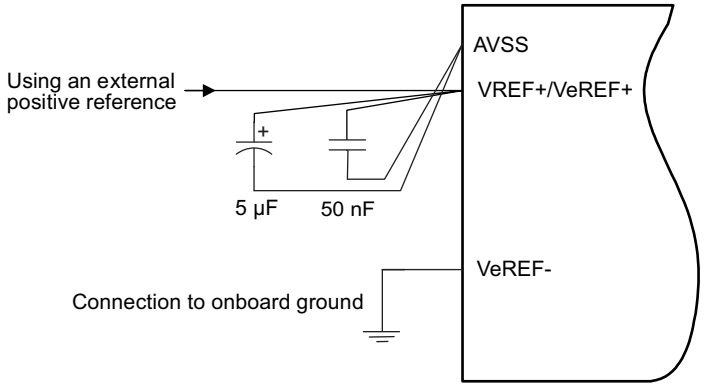


Figure 20. Precision ADC Grounding and Noise Considerations

3.5 Reset

MSP432P4 microcontrollers support a power-on-reset (POR) class reset from the $\overline{\text{RST}}$ pin. The $\overline{\text{RST}}$ input pin can be used to hold off initialization of the device if asserted prior to power on reset, or to create the equivalent of a power-on reset if asserted after power has been applied.

Never leave the $\overline{\text{RST}}$ pin floating. It can be driven from a voltage supervisor or other control chip. It can be connected to an external RC combination using a 47-kΩ resistor pulled up to DVCC and a 1.1-nF capacitor pulled down to DVSS.

The $\overline{\text{RST}}$ pin input contains a glitch filter to prevent noise from causing a system reset.

To protect the $\overline{\text{RST}}$ signal from noise, use a pulldown capacitor to DVSS. This protection is particularly important in applications that involve power switching that can allow fast transitions to couple into the reset line. Route the reset PCB trace away from noisy signals. Do not run the reset trace close to the edge of the board or parallel to other traces with fast transients. Make sure the capacitor is located as close as possible to the $\overline{\text{RST}}$ pin on the device.

A simple push-switch can be used to provide a manual reset.

3.6 Oscillators and Clock Sources:

The following sections describe the components and layout for an external oscillator and for the optional low-temperature coefficient resistor that can be used with the internal digitally controlled oscillator (DCO).

3.6.1 External Oscillators

The MSP432P4 family of devices support a low-frequency crystal (32.768 kHz) and a high-frequency crystal (1 to 48 MHz) on the LFXT and HFXT pins, respectively. The following equations show how to select the load capacitors to ensure that the oscillator oscillates at the desired frequency.

Capacitors need to have a value based on Equation 1.

$$C_{Load} = \frac{C'_{L1} \times C'_{L2}}{C'_{L1} + C'_{L2}}$$

where

- $C'_{L1} = C_{L1} + C_{L1Parasitic}$
- $C'_{L2} = C_{L2} + C_{L2Parasitic}$ (1)

Where if both capacitors C_{L1} and C_{L2} are equal then the equation simplifies to Equation 2.

$$C_{Load} = \frac{C_{L1} \times C_{Parasitic}}{2} \quad (2)$$

Example:

Crystal requires 12-pF load.

Parasitic capacitance per pin is 2 pF.

$C_{L1} = (2 \times C_{Load}) – C_{Parasitic} = (2 \times 12\ pF) – 2\ pF = 22\ pF$

$C_{L2} = C_{L1} = 22\ pF$

Figure 21 shows a typical connection diagram.

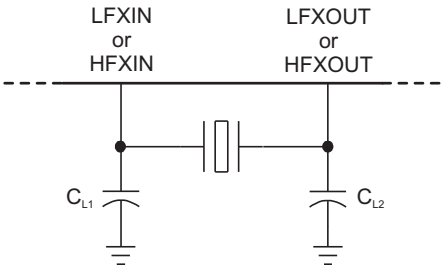


Figure 21. Typical Crystal Connection

One result of choosing the wrong load capacitors, which can be easily measured, is an incorrect oscillation frequency. Figure 22 shows a typical curve of frequency vs load capacitance.

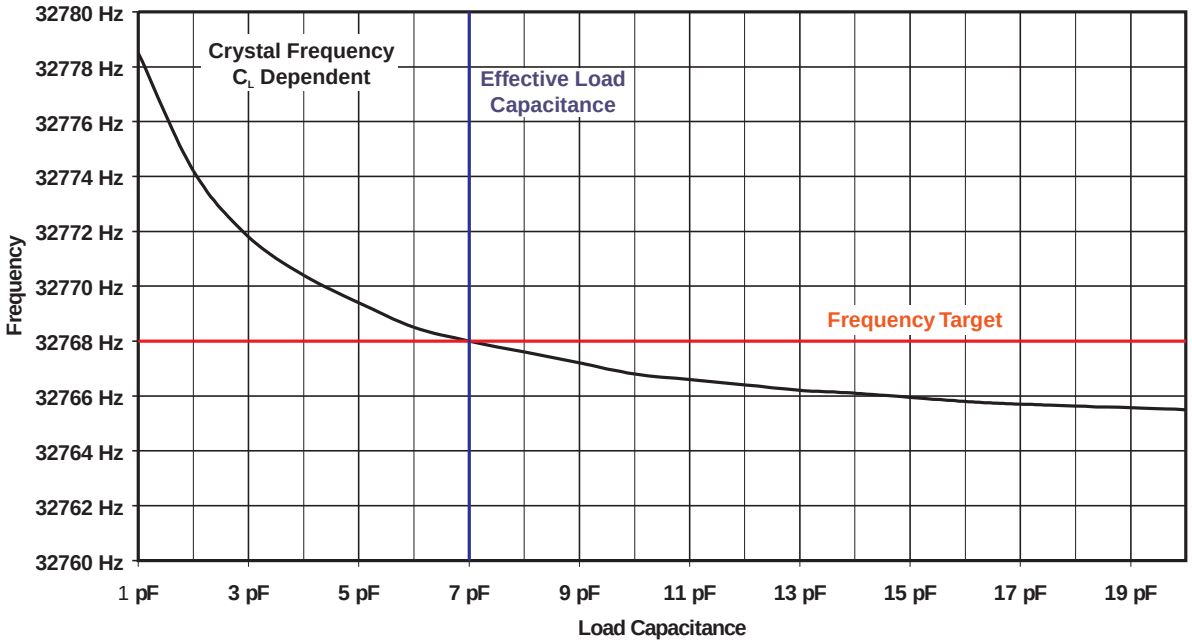


Figure 22. Frequency vs Load Capacitance for a 0-ppm Crystal

It is also possible to apply digital clock signals to the LFXIN and HFXIN input pins that meet the specifications of the respective oscillator if the appropriate LFXTBYPASS or HFXTBYPASS mode is selected. In this case, the associated LFXOUT and HFXOUT pins can be used for other purposes.

See MSP430 32-kHz Crystal Oscillators for more information on selecting, testing, and designing a crystal oscillator with the MSP432™ MCUs.

3.6.2 Crystal Oscillator Circuit Layout

The key layout objectives are to minimize both the loop area of the oscillator signals and the overall trace length. A poor oscillator layout can result in unreliable or inaccurate oscillator operation and can also be a noise source. Ideal trace length is less than 0.25 in (6 mm). Do not exceed 0.75 in (18 mm).

Figure 23 shows a preferred layout for a small surface-mount crystal. The GND side of each capacitor routes directly to a via that provides a low-impedance connection to the GND plane.

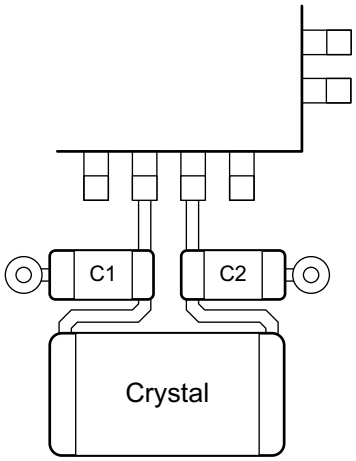


Figure 23. Recommended Layout for Small Surface-Mount Crystal

3.6.3 Internal Oscillators

The device supports a number of internal oscillators such as the DCO, VLO, REFO, MODOSC, and SYSOSC. The DCO is a power-efficient tunable internal oscillator that generates up to 48 MHz. The DCO also supports a high-precision mode when using an external precision resistor. The VLO is an ultra-low-power internal oscillator that generates a low-accuracy clock at typical frequency of 9.4 kHz. The REFO can be used as an alternate low-power lower-accuracy source of a 32.768 kHz clock instead of the LFXT. The REFO can also be programmed to generate a 128-kHz clock. The MODOSC is an internal clock source that has a very low latency wake-up time. It is factory-calibrated to a frequency of 25 MHz. The MODOSC is typically used to supply a 'clock on request' to different modules. It can be used as a clock source for ADC operation at 1-Msps sampling rate. The SYSOSC is an internal clock source that is factory calibrated to a frequency of 5 MHz. It can be used as a clock source for ADC operation at 200-ksps sampling rate. In addition, the SYSOSC is also used for timing of various system-level control and management operations.

3.6.4 DCO External Resistor Option

The internal DCO can use an external resistor to bias the oscillator. An external resistor with a low temperature coefficient can reduce the DCO drift across temperature. The recommended value for this resistor is 91 kΩ with a 0.1% tolerance and a temperature drift of ±25 ppm/°C.

Like decoupling capacitors, place this resistor as close as possible to the device with wide traces to prevent noise coupling or increase in the impedance of the trace.

3.7 JTAG Interface

This section describes design considerations related to the microcontroller JTAG interface.

3.7.1 Debug and Programming Connector

The MSP432 microcontroller provides a JTAG/SWD interface for both debugging and programming the device. If only programming access is needed, the BSL can be used to access the device. In pin-constrained applications, Serial Wire Debug (SWD) can be used instead of JTAG. SWD requires only 2 signals (SWCLK and SWDIO) instead of the 4 signals that JTAG requires, which frees 2 additional signals for use as GPIOs. Make sure that your preferred tool-chain supports SWD before choosing this option.

Recommended headers include the 2×10-way 0.1-in pitch header and a 0.05-in half-pitch 2×5 connector known as the Arm® Cortex® debug connector. Table 5 lists the applicable assignments for both connectors. Figure 24 and Figure 25. show how the headers are connected to the board. See Using SimpleLink™ MSP432E4 Microcontrollers Over the JTAG Interface for more details.

Table 5. Applicable Debug Connector Pin Assignments

JTAG or SWD Signal	Legacy Arm 20-Pin (0.1-in Pitch)	Cortex Debug Connector 10-Pin (0.05-in Pitch)
TCK/SWCLK	9	4
TMS/SWDIO	7	2
TDI	5	8
TDO/SWO	13	6
$\overline{\text{RESET}}$	15	10
GND	4, 6, 8, 10, 12, 14, 16, 18, 20	3, 5, 9
TVCC	1	1

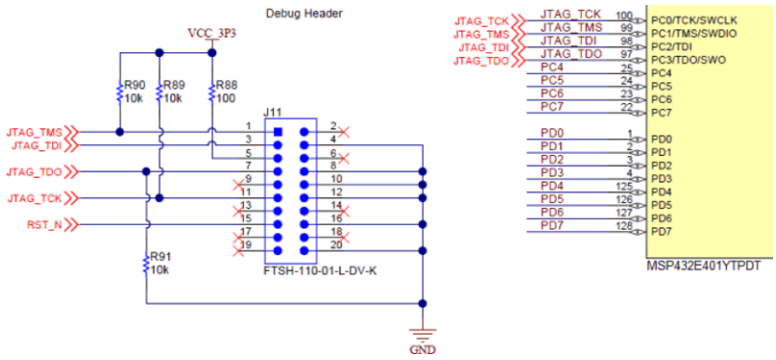


Figure 24. CTI 20-Pin Header

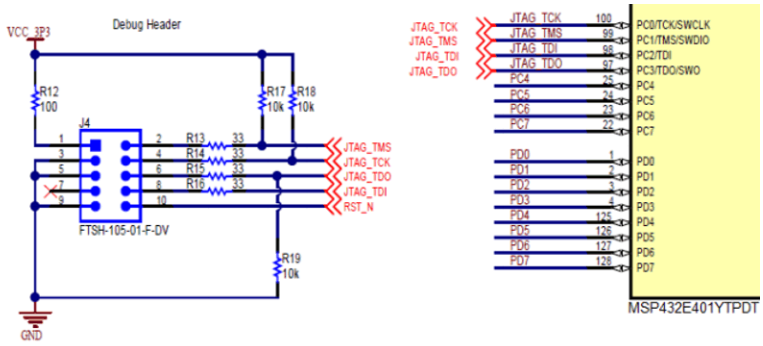


Figure 25. Arm 10-Pin Header

See the *Connection for Unused Pins* section of the device-specific data sheet for more information on how to connect the TCK, TMS, TDI, and TDO pins.

3.8 System

This section describes system-level design considerations related to the MSP432P4 microcontrollers.

3.8.1 I/O Drive Strengths

There are two types of I/Os available. One with regular drive strength and the other with high drive strength. Most of the I/Os have regular drive strength while some selected I/Os have high drive strength. Four 20-mA high-drive I/Os on pins P2.0 to P2.3. See device-specific data sheet for more I/Os with high drive strength. PxDS register is used to select the drive strength of the high drive strength I/Os.

- Bit = 0: High drive strength I/Os are configured for regular drive strength
- Bit = 1: High drive strength I/Os are configured for high drive strength

PxDS register does not have any effect on the I/Os with only regular drive strength.

3.8.2 Series Termination Resistors

Series termination resistors provide two different functions. The first function is for outputs with fast rise and fall times driving light loads to help match the output impedance of the driver to the impedance of the net being driven. This configuration helps with several items:

- Lower overshoot or undershoot at the input destination.
- Reduce ringing near the transition region of the input that could cause false clocking or timing violations.
- Limit crosstalk induced on neighboring signals.
- Reduce EMC emissions.

Output series termination is best placed within 0.5 in (12.7 mm) of the output pin. The values used are system dependent but are often 0 Ω, 10 Ω, 22 Ω, or 33 Ω.

The second function of series termination resistors is to protect input and output pins from ESD strikes by limiting the currents and voltages seen at these pins. This protection is particularly important for signals that go to connectors that are exposed outside the system and for signals that go through connectors to other boards or cables that remain in the system. Higher-speed signals that go from board to board typically have resistor values of 10 Ω to 33 Ω. Lower-speed signals that connect to cables or external connectors typically have resistor values of 50 Ω to 150 Ω.

3.8.3 ESD and EMC Protection

Any signal from the MSP432P4 microcontroller that is exposed outside the system enclosure through a connector must have ESD protection.

In some system environments, signals that stay internal but come through a connector from another board or cable can be subject to radiated noise from electrical noise sources such as motor drivers, relays, and other power-switching circuits. Radiated noise is particularly a concern for 2-layer boards that do not have a solid ground plane to shield the signals from this type of noise. For signals that fall into this category, TI recommends including an ESD protection circuit like the one described in Figure 26 or Figure 27. Package options for the TVS diodes that support multiple I/O are also available.

The exact resistor values and TVS diode configuration highly depends on the system and environment.

Timing requirements of the interface, input or output signal direction, exposure to electrical noise sources, and IEC test level must be taken into account when determining what values to use.

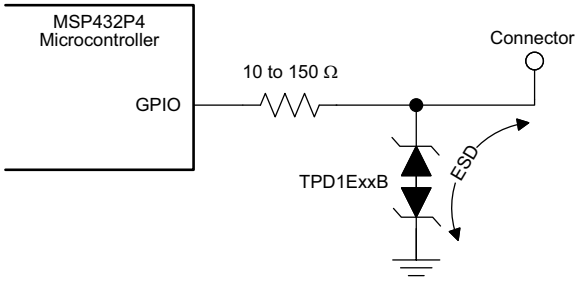


Figure 26. General ESD Protection Using Bidirectional TVS Diode

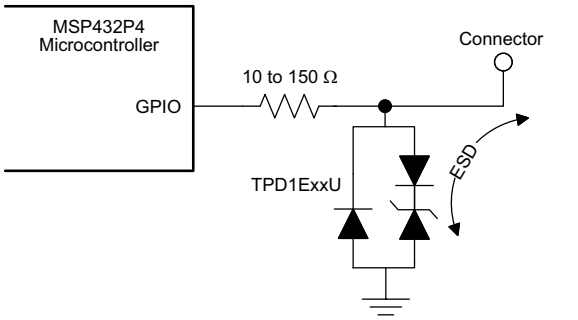


Figure 27. General ESD Protection Using Unidirectional TVS Diode

Proper ESD level protection must be considered to protect the device from unintended high-voltage electrostatic discharge. See MSP430™ System-Level ESD Considerations for guidelines.

3.8.4 Interrupt Pin Selection

Any GPIO pin in the microcontroller can be used as an interrupt input pin. In most cases, there is one interrupt vector per GPIO port, so the interrupt service routine must check status registers to determine which port pin generated the interrupt. The MSP432P401 can have interrupts on any ports 1 through 6. See the device-specific data sheet to determine which GPIO pins have this capability.

3.8.5 Clock Routing

Pay special attention to any pins or nets that are used as clock signals. The cleanest clock is one that routes directly from an output pin to an input pin without stubs, tees, or multiple destinations. Consider the following guidelines when routing clock signals:

- Give clock traces twice the spacing of other signals. For example, if a 7-mil trace with 7-mil space routing rules are being used, give 14-mil spacing between the clock and any other signal. This distance limits crosstalk from neighboring nets.

- Add a footprint for a series resistor close to the clock output pin to adjust for any ringing or EMI concerns beyond what changing the I/O drive strength can do. Typical series resistor values are 0 Ω, 10 Ω, 22 Ω, or 33 Ω.
- If probe points are added for clocks, place them as close as possible to the clock destination. Consider adding a ground point nearby for ease of measurement. Clock signals are noisiest near the middle of the net due to reflections. Clocks measured at a location other than the destination are usually not representative of how the signal appears at the destination.
- When routing a clock to multiple destinations, try to group the destination points in the same area. In most cases, it is best to daisy-chain route the clock instead of tee routing the clock to the destinations.
- Tee routing generally causes greater reflections unless carefully balanced.
- When routing a clock to multiple destinations, place the most timing sensitive and critical of the destination devices at the end of the net where the clock is the cleanest.
- The clock must follow the same general path as the data and control signals associated with the interface it clocks in order to maintain the same general length and any relative bus timings.

3.8.6 Unused Pins

The preferred connection for an unused microcontroller pin depends on the pin function. Each data sheet lists the fixed function pins as well as both the acceptable practice and the preferred practice for reduced power consumption and improved electromagnetic compatibility (EMC) characteristics. See the *Connection for Unused Pins* section in the data sheet for correct termination of all unused pins.

To prevent a floating input and to reduce power consumption, configure unused I/O pins as I/O function, output direction, and left unconnected on the PC board. The value of the PxOUT bit is don't care, because the pin is unconnected. Alternatively, the integrated pullup or pulldown resistor can be enabled by setting the PxREN bit of the unused pin to prevent a floating input.

NOTE: Configuring port PJ and shared JTAG pins

Make sure that port PJ is configured properly to prevent a floating input. Some pins of port PJ are shared with the JTAG TDI and TDO functions and are initialized to the JTAG functionality on reset. Other pins of Port J are initialized to high-impedance inputs by default.

3.8.7 Errata Documentation

Part of any good system design includes reviewing and understanding any errata associated with the revision of device being used. Each errata document (for example, MSP432P401R Device Erratasheet) describes any deviations from the data sheet. These advisories must be followed to ensure correct device operation.

3.9 All External Signals

This section describes design considerations related to signals that connect directly from the microcontroller to a connector that takes the signal to another board or external device.

The system design must ensure that the ground reference of any incoming signal is the same as the microcontroller ground. If the grounds do not match, the signal level seen at the input pin of the microcontroller can be significantly higher than what the data sheet specifies. Ground connections between boards must be low impedance, be able to handle the return current load, and be as short as possible.

The system design must avoid routing the V_{CC} 3.3-V supply that connects to the microcontroller directly to a connector pin that can be subject to ESD or EMC radiated emissions. If V_{CC} does need to be routed to a connector, route it through a ferrite bead and optionally a TVS diode.

Do not drive I/O signals that are sourced from cables or other boards before applying power to the microcontroller unless the strict guidelines for injection current and voltage limits from the data sheet are followed.

Implement layout options for ESD protection on external I/O signals that come directly from the microcontroller, as described in Section 3.8.3.

4 Feature Specific Design Information

This section contains feature-specific design information and is grouped by function or peripheral:

- eUSCI
  - UART
  - I^2C
  - ADC
- Comparators
- Timer/PWM
- GPIO
- LCD Controller

4.1 eUSCI

The enhanced universal serial communication interface (eUSCI) supports synchronous communication protocols such as SPI (3-pin or 4-pin) and I^2C, and asynchronous communication protocols such as UART, enhanced UART with automatic baud-rate detection, and IrDA. eUSCI is separated into two modules eUSCI_A which supports UART and eUSCI_B which supports I^2C. Both eUSCI_A and eUSCI_B supports SPI mode.

The eUSCI_An module provides support for SPI (3-pin or 4-pin), UART, enhanced UART, and IrDA.

The eUSCI_Bn module provides support for SPI (3-pin or 4-pin) and I^2C.

The MSP432P4 MCUs offer up to four eUSCI_A and four eUSCI_B modules.

See the eUSCI specification in the data sheet for more information about the supported clock frequencies and V_{CORE} voltages for the different modes.

Table 6 lists the supported channels for eUSCI functions for each MSP432P4 device package.

Table 6. Device eUSCI Channel

Package	eUSCI		20-mA Drive I/Os	Total I/Os
	Channel A: UART, IrDA, SPI	Channel B: SPI, I^2C		
100-pin PZ	4	4	4	84
80-pin ZXH	3	4	4	64
64-pin RGC	3	3	4	48

4.1.1 UART

In UART mode, the eUSCI_A transmits and receives characters at a bit rate asynchronous to another device. Timing for each character is based on the selected baud rate of the eUSCI_A. The transmit and receive functions use the same baud-rate frequency.

In asynchronous mode, the eUSCI_Ax modules connect the device to an external system through two external pins, UCAxRXD and UCAxTXD. Depending upon the device package, either 3 or 4 eUSCI instances are available. UART mode is selected when the UCSYNC bit is cleared. See the *Enhanced Universal Serial Communication Interface (eUSCI) – UART Mode* chapter of the MSP432P4 SimpleLink™ Microcontrollers Technical Reference Manual for detailed information.

The specific pin number and corresponding BSL functions are the same for the three different packages.

- UART BSL pins include P1.2/BSLRXD and P1.3/BSLTXD
- SPI BSL pins include P1.4/BSLSTE, P1.5/BSLCLK, P1.6/BSLSIMO, P1.7/BSLSOMI

- I²C BSL pins include P3.6/BSLSDA, P3.7/BSLSCL

4.1.2 SPI

Both the eUSCI_A and the eUSCI_B support serial communication in SPI mode.

The eUSCI connects the device to an external system through 3 or 4 pins, depending upon the configuration selected: UCxSIMO, UCxSOMI, UCxCLK, and UCxSTE. The slave transmit enable is the additional pin in 4-wire mode. UCxSTE is not a chip select. SPI mode is selected when the UCSYNC bit is set, and SPI mode (3 pin or 4 pin) is selected with the UCMODEx bits.

The UCxSTE is designed to control the data flow between a single master and slave device. If additional slaves are added, TI recommends that you use a GPIO to implement a chip select function. See the *Enhanced Universal Serial Communication Interface (eUSCI) – SPI Mode* chapter of the MSP432P4 SimpleLink™ Microcontrollers Technical Reference Manual for detailed information.

4.1.3 I²C

The I²C mode supports any slave or master I²C-compatible device. Figure 28 shows an example of an I²C bus. Each I²C device is recognized by a unique address and can operate as either a transmitter or a receiver. A device connected to the I²C bus can be considered as the master or the slave when performing data transfers. A master initiates a data transfer and generates the clock signal SCL. Any device addressed by a master is considered a slave. I²C data is communicated using the serial data (SDA) pin and the serial clock (SCL) pin. Both SDA and SCL are bidirectional and must be connected to a positive supply voltage using a pullup resistor. Typical pullup values are 10-kΩ resistors, but the value depends on bus speed and total bus capacitance. See the *Pull-up resistor sizing* section of the I²C-bus specification and user manual from NXP for details on how to calculate the minimum and maximum pullup resistor values.

Only 3.3-V I²C buses are directly supported. 5-V and 1.8-V buses can be supported with the use of external level shifters. An I²C bus that is pulled up and connected to a 3.3-V power rail different from the one attached to the V_{CC} of the MSP432P4 MCU can be pulled low by the ESD structures of the MCU when V_{CC} to the device is not powered. See the *Enhanced Universal Serial Communication Interface (eUSCI) – I²C Mode* chapter of the MSP432P4 SimpleLink™ Microcontrollers Technical Reference Manual for detailed information.

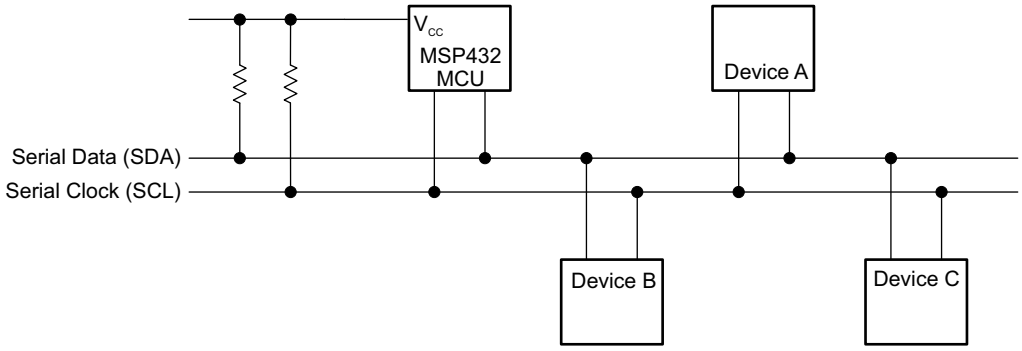


Figure 28. I²C Bus Connection Diagram

4.1.3.1 Routing Considerations

Route the I²C bus so that the SCL and SDA signals follow similar layer transitions. There is no length-matching requirement for these signals. Do not route I²C signals next to signals that can cause significant crosstalk to the SCL signal. Crosstalk noise can interfere with the I²C transaction and cause bus errors that require an I²C bus reset.

4.2 ADC

Up to 24 pins on the MSP432P4 devices support analog inputs AIN00 to AIN23. All inputs can be used in single-ended mode, while differential mode is supported for consecutive even-and-odd pairs. All analog inputs are equivalent in function and capability. Base the selection of which analog inputs on ease of PCB routing and pin muxing selection.

To achieve the best possible conversion results from an ADC, it is important to start with a good schematic design.

4.2.1 ADC External Partial Schematic

Figure 29 shows a partial schematic of the Precision ADC external connections.

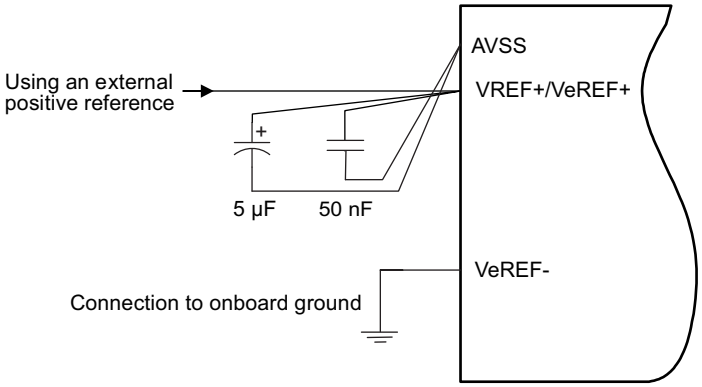


Figure 29. Precision ADC Grounding and Noise Considerations

4.2.2 ADC Design Requirements

As with any high-resolution ADC, follow appropriate PCB layout and grounding techniques to eliminate ground loops, unwanted parasitic effects, and noise. Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small unwanted offset voltages that can add to or subtract from the reference or input voltages of the ADC.

In addition to grounding, ripple and noise spikes on the power-supply lines that are caused by digital switching or switching power supplies can corrupt the conversion result. To achieve high accuracy, TI recommends a noise-free design with separate analog and digital ground planes with a single-point connection.

Figure 29 shows the recommended decoupling circuit when an external voltage reference is used.

The reference voltage must be a stable voltage for accurate measurements. The capacitor values that are selected in the general guidelines filter out the high- and low-frequency ripple before the reference voltage enters the device. In this case, the 5-µF capacitor is used to buffer the reference pin and filter any low frequency ripple. A 50-nF bypass capacitor is used to filter out any high-frequency noise.

4.2.3 Layout Guidelines

Place the components in the partial schematic (see Figure 29) as close as possible to the respective device pins. Avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal.

Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal.

If differential mode is used for the Precision ADC, the analog differential input signals must be routed close together to minimize the effect of noise on the resulting signal.

4.3 Comparators

Two window comparators and two independent integrated analog comparators are available on MSP432P4 MCUs. See the *COMP_E* chapter of the MSP432P4 SimpleLink™ Microcontrollers Technical Reference Manual for details.

NOTE: Comparator Input Connection

When the comparator is on, connect the input terminals to a signal, power, or ground. Otherwise, floating levels can cause unexpected interrupts and increased current consumption.

4.4 Timer and PWM

Several general-purpose timer pins are available on MSP432P4 devices. This device contains up to four 16-bit timers (TA0, TA1, TA2, TA3) and two 32-bit timers. Timer_A is a 16-bit timer/counter with five capture/compare registers. Timer_A can support multiple capture/compares, PWM outputs, and interval timing. Timer32 consists of two programmable 32-bit or 16-bit down counters that can generate interrupts on reaching zero. Each timer module can be configured as two independent 16-bit timers or a combined 32-bit timer. See the Timer_A section in the data sheet or Timer32 and Timer_A chapters in the MSP432P4 SimpleLink™ Microcontrollers Technical Reference Manual for details.

4.5 GPIO

Most pins on an MSP432P4 device can be used as GPIOs. GPIO pins are designated by the letter P followed by the port number (1 to 10) and the pin number (0 to 7). GPIOs also include pins PJ.0 to PJ.5. GPIO pins can be used for inputs that are sampled by software, inputs that generate interrupts, outputs that drive logic inputs high or low, or outputs that drive LEDs.

See the *Specifications* chapter of the device-specific data sheet where important operational conditions are detailed. See the Digital I/O specifications in the data sheet for the characteristics of the digital inputs.

Up to 10 8-bit I/O ports are implemented:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Edge-selectable interrupt capability is available on ports P1 to P6.
- Wake-up capability from LPM3, LPM4, LPM3.5, and LPM4.5 modes on ports P1 to P6.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise or in pairs (16-bit widths).
- Capacitive-touch functionality is supported on all pins of ports P1 to P10 and PJ.
- Four 20-mA high-drive I/Os on pins P2.0 to P2.3.
- Glitch filtering capability on selected digital I/Os.

Consider the following when selecting and designing with pins configured as GPIO inputs:

- Pins are 3.3-V tolerant and are not 5-V tolerant.
- GPIO pins can be configured with an internal pullup or pulldown. See the *Specifications* chapter of the device-specific data sheet for the internal pullup and pulldown values. It can be desirable to use external pullups or pulldowns in situations where a more consistent rise/fall time is required.

Consider the following when selecting and designing with pins configured as GPIO outputs:

- At system power-on reset, pins power up as GPIO inputs with no pullup or pulldown configured. Externally pull up or pull down any pins that are used as outputs and that must be at a high or low at system power up. The exceptions are the JTAG pins—leave the JTAG TDI pin open and externally pull down the JTAG TDO/SWO pin.

4.6 LCD Controller

Some MSP432P4 MCUs include an LCD controller. The signal interface to the LCD panel is likely to be an ESD-exposed interface. TI recommends using series resistors on all of the LCD interface signals. The value of the resistor can be 10 Ω to 150 Ω. For a detailed explanation, see the MSP432P4 SimpleLink™ Microcontrollers Technical Reference Manual. Also see the LCD section of the device-specific data sheet for operating conditions of the LCD controller.

5 System Design Examples

Table 7 lists example designs using the MSP432P4 microcontrollers.

Table 7. MSP432P4 Example Designs

Part Number	Description	Device	Device Package	Key Features	PCB Layer Count
MSP432P401R	SimpleLink MSP432P401R LaunchPad™ development kit	MSP432P401RIPZ	100-pin LQFP	Low power, high precision	4
MSP432P4111	SimpleLink MSP432P4111 LaunchPad development kit	MSP432P4111IPZ	100-pin LQFP	Low power, high precision, LCD	4

6 Conclusion

Applying good system design practices from the earliest design stages ensures a successful board bring up. The design process must include thorough design reviews using the information in this application report, other embedded system design resources, and reports created by the design team. These efforts will be rewarded with a reliable and properly performing MSP432P4 microcontroller-based design.

7 References

The following related documents and software are available on the TI MSP432 website:

1. MSP432P401R, MSP432P401M SimpleLink™ Mixed-Signal Microcontrollers
2. MSP432P411x, MSP432P401x SimpleLink™ Mixed-Signal Microcontrollers
3. MSP432P4 SimpleLink™ Microcontrollers Technical Reference Manual
4. SimpleLink™ MSP432P4 Software Development Kit (SDK)
5. MSP430™ System-Level ESD Considerations
6. PCB Layout Footprints for MSP432P4
7. MSP430™ 32-kHz Crystal Oscillators
8. PCB Design Guidelines for 0.5mm Package-on-Package Applications Processor
9. M. I. Montrose, "Right angle corners on printed circuit board traces, time and frequency domain analysis," 1999 International Symposium on Electromagnetic Compatibility (IEEE Cat. No.99EX147), Tokyo, Japan, 1999, pp. 638-641. doi: 10.1109/ELMAGC.1999.801409
10. MSP432™ SimpleLink™ Microcontrollers Hardware Tools
11. nFBGA Packaging
12. Quad Flatpack No-Lead Logic Packages
13. SMT and packaging application notes
14. PCB Design Guidelines for 0.5mm Package-on-Package Applications Processor, Part 1

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265