MOST25 Interface Product Specification (M25I)

1 Features

Compact Network Interface 2+0 Optical Header

2 Description

This document describes the hardware for the SMN MOST25 Network Interface.



3 Hardware Specifications

3.1 Host Connector:

This is the primary interface between the Network PCB and the Host PCB.

3.1.1 Connector type:

Hirose DF11Z-22DS-2V(50) female header

3.1.2 Mating connector on Host PCB:

Through-hole: Hirose DF11-22DP-2DSA(01), Board-Board spacing =

7.55mm

SMT: Hirose DF11-22DP-2V(20), Board-Board Spacing = 8.2mm

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3.1.3 Pin Assignments:

1	FSY (LRCLK)	2	SCK (BCLK)
3	SR1	4	SX1
5	SR0	6	SX0
7	RMCK (256fs)	8	Reserved/MLBCLK
9	SCL	10	SDA
11	INT*	12	RESET*
13	STATUS	14	ERR/BOOT*
15	RSOUT	16	Reserved/TBD1
17	Reserved/TBD2	18	Reserved/TBD3
19	GND	20	Reserved/DIAG*
21	+3V3	22	+12VP

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3.1.4 Signal Definitions:

Pin #	Signal	Туре	Description
1	FSY	Dout	Frame Sync clock for I2S serial data, clocks at audio sample rate, with leading pulse low.
2	SCK	Dout	Bit Clock for I2S serial data, clocks at 256Fs with leading pulse low
3	SR1	Din	Receive data1 for I2S
4	SX1	Dout	Transmit data1 for I2S
5	SR0	Din	Receive data0 for I2S
6	SX0	Dout	Transmit data0 for I2S
7	RMCK	Dout	256Fs Master clock output
8	MLBCLK	Dout	Not used
9	SCL	Di/o	I2C bit clock, Most card includes 2.2k pullup
10	SDA	Di/o	I2C data, Most card includes 2.2k pullup
11	INT*	Dout	Active Low Interrupt request for I2C service, must be connected to Host INT input.
12	RESET*	Din	Active Low reset input. Must be connected to HOST GP output.
13	RXSTATUS	Dout	Low indicates light at receiver, Must be connected to Host GP input
14	ERR/BOOT*	Dout	Low indicates Network is locked. Must be connected to Host GP input
15	RSOUT		Not used
16	TBD1		Not used, can be connected to GPIO
17	TBD2		Not used, can be connected to GPIO
18	Reserved		Not used
19	GND	PWR	Digital Ground
20	Reserved		
21	+3V3	PWR	Switched +3V3 input for digital logic & FOT.
22	+12VP	PWR	+12V input for battery monitoring, can be unswitched. Should be protected vs overvoltage.

3.2 INIC Debug Connector:

This header allows connection of the INIC Explorer for development

3.2.1 Connector Type:

Generic 2x7, .070" male header

1	NC	2	GND
3	NC	4	ERR/BOOT*
5	GND	6	+3V3
7	TDI/DSDA	8	TCK/DSCL
9	+3V3	10	GND
11	TDO/DINT*	12	RST_Debug
13	NC	14	TMS

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3.2.2 Signal Definitions:

Per OS81050 INIC specification

3.3 Optical Connector

Tyco # 1-1670571-1, 3.3V Most 2+0 connector with "type A" keying/coding.

3.4 Power State Monitor

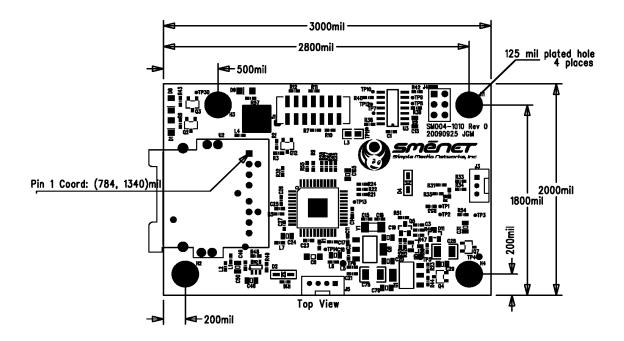
The MOST network requires monitoring of the battery voltage, and entry into a low power state. Circuitry will be included on the network interface to monitor the battery level, and trigger the appropriate state changes.

3.5 Mechanical Parameters

3.5.1 Overall Dimensions:

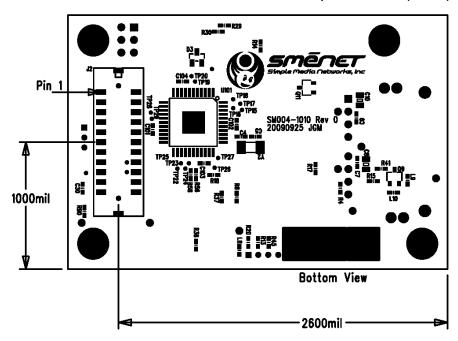
PCB assembly dimension: 2.00" x 3.00"x 1.00"

3.5.2 Board Outline/Placement:



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3.5.3 Mounting locations:

4 110mil holes for #4 screws

The following mounting hole coordinates are relative to the lower left corner of the PCB, as shown in the Top View Drawing. All dimensions in thousandths of an inch (mils):

(200, 200)

(2800, 200)

(2800, 1800)

(500, 1800)

4 Electrical Specifications

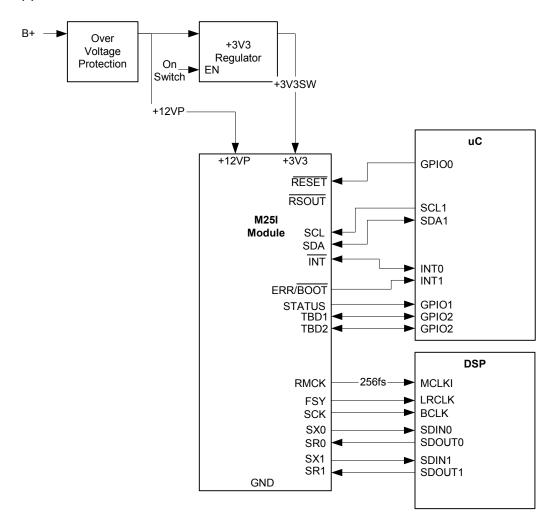
Symbol	Definition	Min	Nom	Max	Units
+3V3	Supply Voltage		+3.3V		V DC
+12V	Protected Battery Voltage		14.4	26	VDC
Fs	Most Frame Rate		48.00		kHz
Frmck	Most Master Clock Frequency (256Fs)		12.288		MHz
UVcrit	At Vbat < UVcrit net enters low power state		9.0		
UVIo	At Vbat< UVIo, net will shutdown.		7.0		
I12vp0	+12V current when +3V3 is <1VDC			20	uA
I12vp	+12V current			20	mA
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		 	 	 /	
13V3	+3V3 current			250	mA

Application Circuit



It should be noted that the M25I is the clocking master for the audio sources.

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