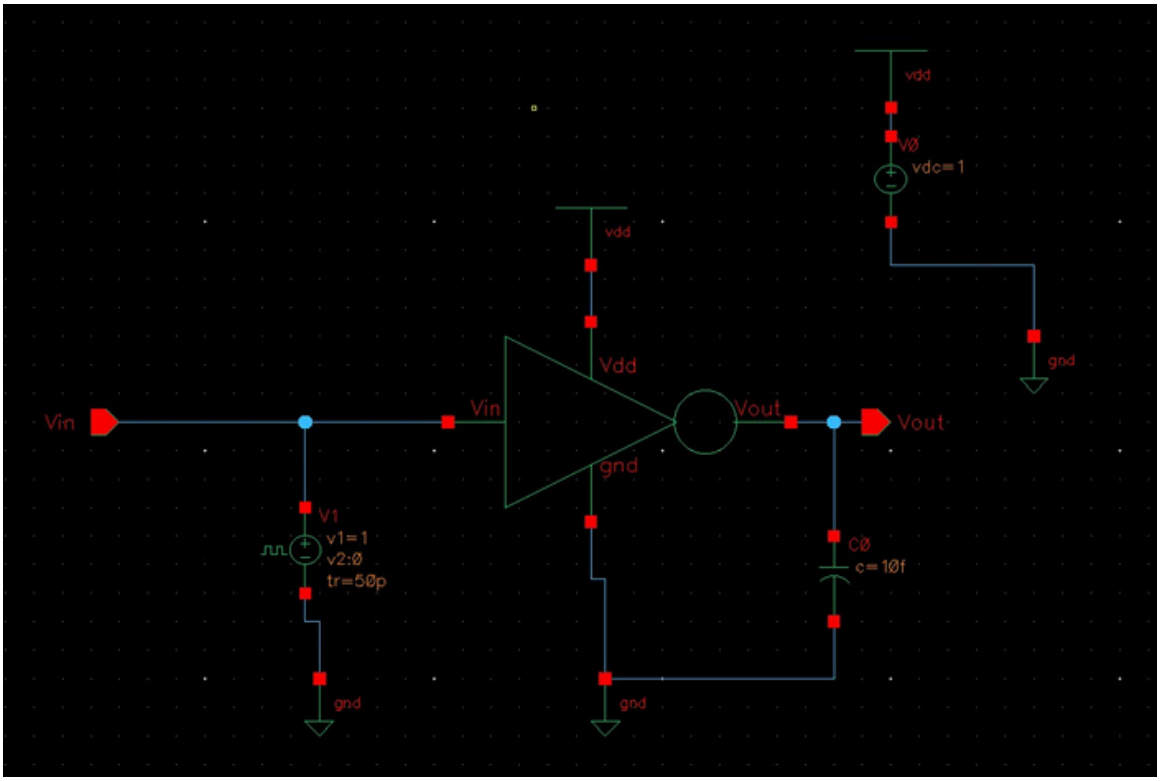
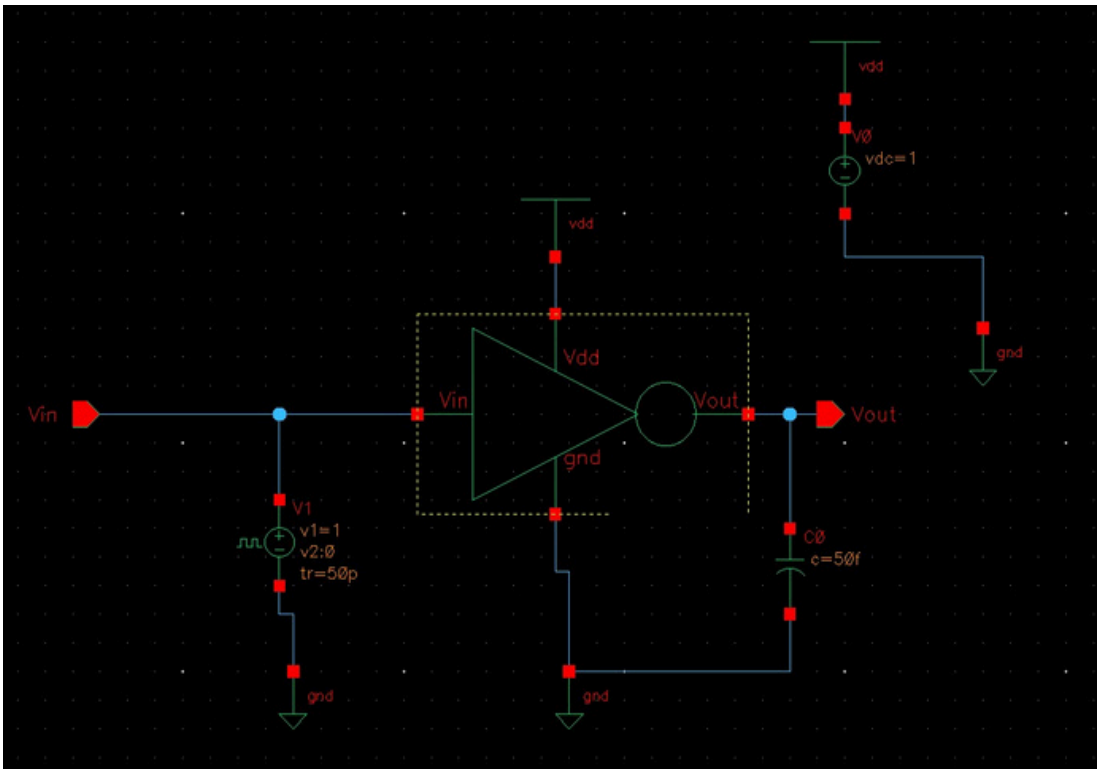
Tanushri Lute
2317099

Ques1 Implement a CMOS inverter driving capacitive loads of 10 fF, 50 fF, and 100 fF.

a) 10fF

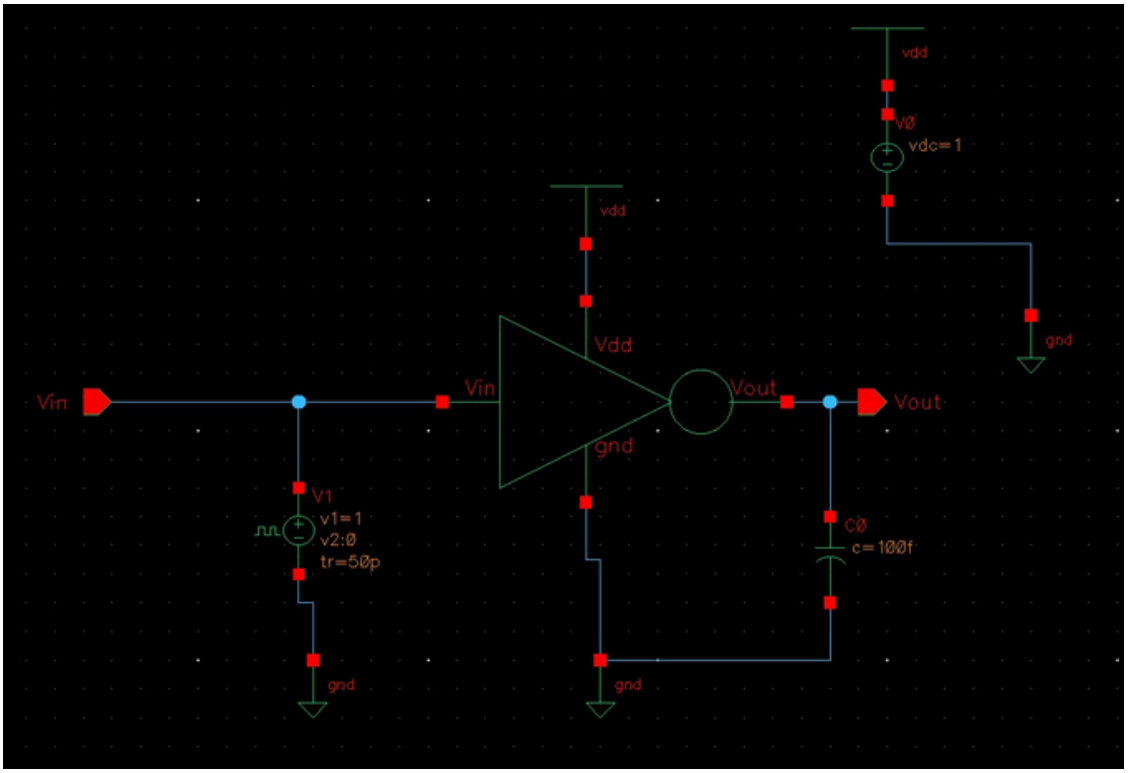


b) 50 fF

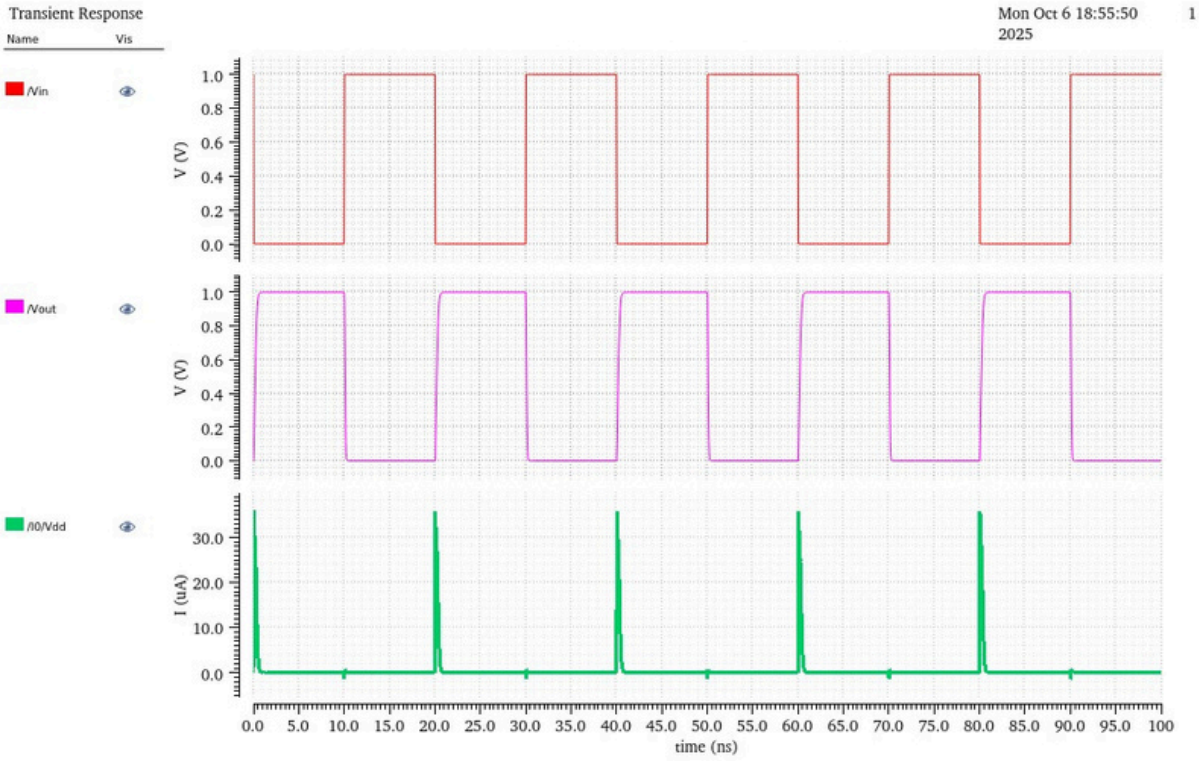


Tanushri Lute
2317099

c) 100fF



Ques2 Measure tpHL, tpLH, and dynamic power for each case.



Tanushri Lute
2317099

For 10fF

Dynamic power for 10fF is 15.52 E-6

tphl = 73.7281p tplh = 59.2745p

For 50fF

Dynamic power for 50fF is 25.52 E-6

tphl = 866.837p

tphl =878.307p

For 100fF

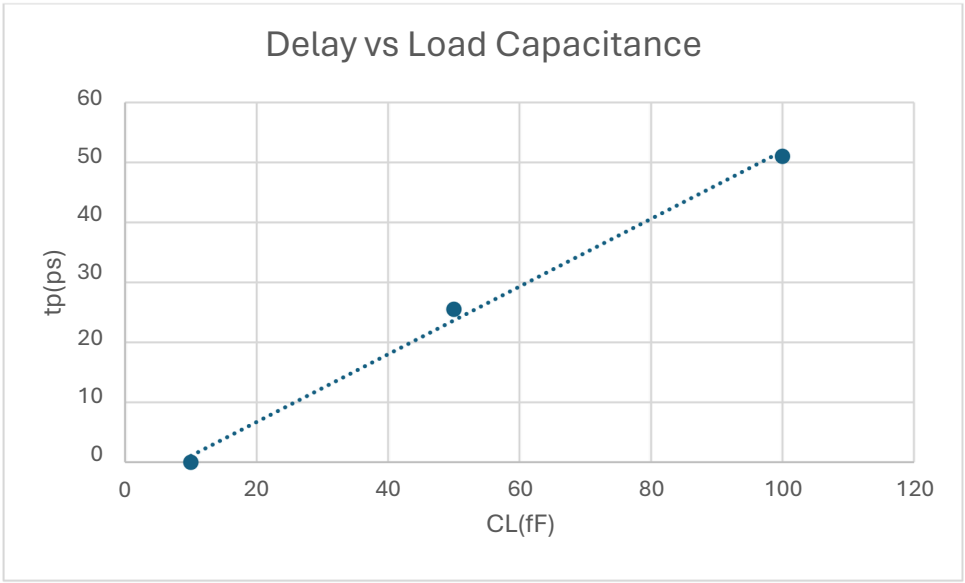
Dynamic power for 100fF is 15.52 E-6

tphl =1.85424n

tphl =1.7281n

Ques 3 Plot delay vs load capacitance.

CL (fF)	tp(ps)
10	66.5
50	872.57
100	1791.17

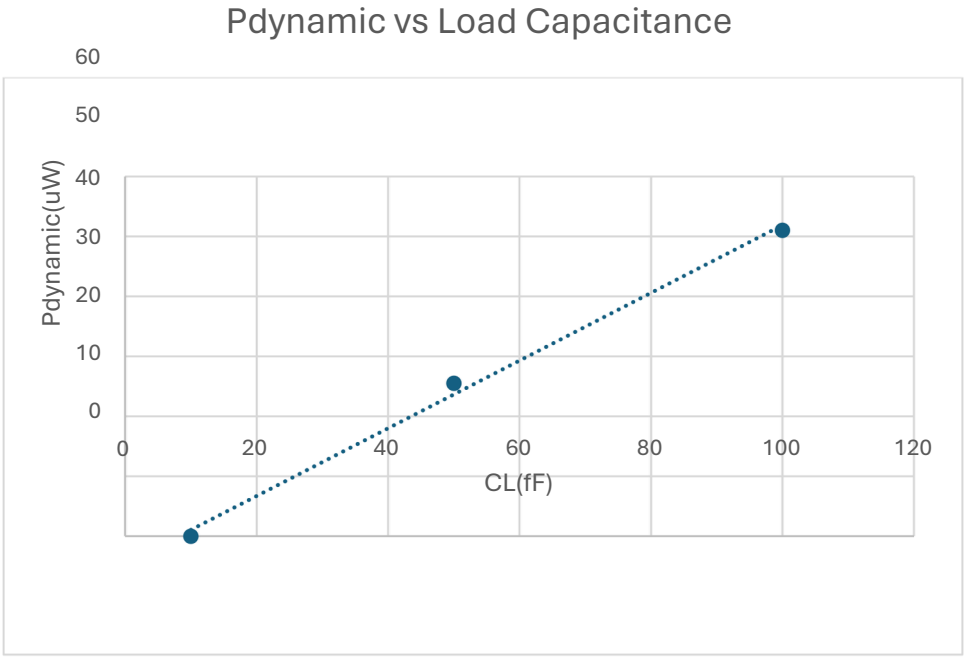


Tanushri Lute
2317099

From this trend, we can say that Delay is directly proportional to Load Capacitance.

Ques 4 Plot power vs. load capacitance.

CL (fF)	Pdyn (µW)
10 50	5.10 **25.52**
100	**51.04**



From this trend, we can say that Dynamic Power is directly proportional to Load Capacitance.