

# Walchand College of Engineering, Sangli

*(Government Aided Autonomous Institute)*

**AY 2023-24**

## Course Information

<b>Programme</b>	B.Tech. (Electronics Engineering)
<b>Class, Semester</b>	Third Year B. Tech., Sem VI
<b>Course Code</b>	6EN321
<b>Course Name</b>	Electromagnetic Engineering
<b>Desired Requisites:</b>	

<b>Teaching Scheme</b>		<b>Examination Scheme (Marks)</b>			
<b>Lecture</b>	3 Hrs/week	<b>MSE</b>	<b>ISE</b>	<b>ESE</b>	<b>Total</b>
<b>Tutorial</b>	# Hrs/week	30	20	50	100
<b>Credits: #</b>					

## Course Objectives

<b>1</b>	To <b>understand</b> the electric fields, electric energy and potential.
<b>2</b>	To <b>understand</b> the magnetic flux and forces, energy stored in magnetic field.
<b>3</b>	To <b>develop</b> in-depth understanding of time-varying fields and electromagnetic waves.
<b>4</b>	To <b>study</b> the electromagnetic wave transmission methods like transmission lines, antennas and waveguides.

## Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,		
<b>CO1</b>	<b>Explain</b> the principles of static and time-varying electric and magnetic fields.	Understan d
<b>CO2</b>	<b>Compare</b> the behaviour of electromagnetic waves in free space and guided medium like two-wire transmission line.	Understan d
<b>CO3</b>	<b>Solve</b> the problems on static and time-varying electromagnetic fields.	Apply
<b>CO4</b>	<b>Analyze</b> the effects of electromagnetic radiation and electromagnetic interference.	Analyze

<b>Module</b>	<b>Module Contents</b>	<b>Hours</b>
I	<b>Electrostatics</b> Review of vector analysis and coordinate systems. Coulomb's Law, electric field intensity, field due to line charge, sheet charge; electric flux density, Gauss's Law and its applications, divergence theorem; energy and potential, potential gradient, electric dipole; energy density in electrostatic field	4
II	<b>Conductors, Dielectrics and Capacitance</b> Current and current density, continuity of current, conductor properties and boundary conditions; boundary conditions for perfect dielectric materials, Poisson's and Laplace's equations; Capacitance.	8
III	<b>Steady Magnetic Field</b> Magnetic field intensity, Biot-Savart Law, Ampere's circuital Law, Stokes' theorem, magnetic flux and magnetic flux density; scalar and vector magnetic potential; Force on a moving charge, force between differential current elements, properties of magnetic materials, energy stored in magnetic field, forces on magnetic materials, inductance, magnetic boundary conditions.	8
IV	<b>Time Varying Fields and Maxwell's Equations</b> Faraday's Law, displacement current, Maxwell's equations in point (differential) form and integral form, time varying potentials, time-harmonic fields	8
V	<b>Uniform Plane Electromagnetic Waves</b> Wave propagation in free space and dielectrics, Power flow in uniform plane wave, Poynting's theorem, wave propagation in conductors: skin depth, reflection of plane waves, standing wave ratio, polarization of uniform plane waves.	7

VI	<b>Transmission Lines</b> Types of two-conductor transmission lines, equivalent circuit, transmission line parameters, transmission line equations, lossless propagation, wave reflection, standing waves and voltage standing wave ratio, reflection coefficient, Smith Chart.	4
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#### Textbooks

1	William H. Hayt and John A. Buck, "Engineering Electromagnetics", 7 <sup>th</sup> Edition, Tata McGraw- Hill, 2007.
2	Matthew N. O. Sadiku, "Elements of Electromagnetics", 3 <sup>rd</sup> Edition, Oxford University Press, 2007.
3	S. C. Mahapatra and Sudipta Mahapatra, "Principles of Electromagnetics", Tata McGraw-Hill, 2011.
4	

#### References

1	E. C. Jordan & K. Balman, "Electromagnetic Waves and Radiating Systems", 2 <sup>nd</sup> Edition, PHI, 2007.
2	David K. Cheng, "Field and Wave Electromagnetics", Pearson Education, 2015.
3	
4	

#### Useful Links

1	<a href="https://nptel.ac.in/courses/108/106/108106073/">https://nptel.ac.in/courses/108/106/108106073/</a>
2	<a href="https://nptel.ac.in/courses/108/104/108104087/">https://nptel.ac.in/courses/108/104/108104087/</a>
3	
4	

#### CO-PO Mapping

	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
<b>CO1</b>		2												2
<b>CO2</b>		2		1										2
<b>CO3</b>	3													2
<b>CO4</b>	3			2										2

The strength of mapping is to be written as 1: Low, 2: Medium, 3: High

Each CO of the course must map to at least one PO.

#### Assessment

The assessment is based on MSE, ISE and ESE.

MSE shall be typically on modules 1 to 3.

ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.

ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.

For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

**Walchand College of Engineering, Sangli**  
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**AY 2023-24**

**Course Information**

<b>Programme</b>	B.Tech. (Electronics Engineering)
<b>Class, Semester</b>	Third Year B. Tech., Sem VI
<b>Course Code</b>	6EN322
<b>Course Name</b>	Digital System Architecture
<b>Desired Requisites:</b>	Digital Electronics

<b>Teaching Scheme</b>		<b>Examination Scheme (Marks)</b>			
<b>Lecture</b>	3 Hrs/week	<b>MSE</b>	<b>ISE</b>	<b>ESE</b>	<b>Total</b>
<b>Tutorial</b>	-	30	20	50	100
<b>Credits: 3</b>					

**Course Objectives**

<b>1</b>	To explain the designs of building blocks of digital system viz. data path design, control unit design, memory units to finally design the microprocessor 2. 3. 4. 5.
<b>2</b>	To illustrate the concepts behind designing the robust digital systems.
<b>3</b>	To unfold the architectures of DACs and ADCs using various approaches motivating students to compare their performance.
<b>4</b>	To assign medium complexity digital system design related problems in batches as a self study exercise.
	To illustrate HDL implementation of digital designs in FPGA

**Course Outcomes (CO) with Bloom's Taxonomy Level**

At the end of the course, the students will be able to,

<b>CO1</b>	Explain the architectures of FPGAs and the concept behind programmable devices	Understand
<b>CO2</b>	Apply FSM approach to develop sequential digital circuits, and floating point and fixed point arithmetic to develop architectures of floating/fixed point data-path blocks.	Apply
<b>CO3</b>	Analyze digital circuits and their architectures for functionality, and memory units for timing performance using timing diagrams.	Analyze
<b>CO4</b>	Compare various approaches of designing memory blocks, DACs and ADCs with references to their merits and demerits and performance parameters respectively	Evaluate
<b>CO5</b>	Develop architectures of digital blocks (Data-path, Control units) with knowledge of functionality extending further to 4-bit/8-bit microprocessor with defined set of instructions.	Create

<b>Module</b>	<b>Module Contents</b>	<b>Hours</b>
I	<b>Designing Datapath Blocks</b> Number representation (fixed point and floating point), Fixed Point arithmetic, floating point arithmetic, High speed adders/ Multipliers (Robertson's algorithm and Booth's algorithm), pipeline processing.	8
II	<b>Designing Control units</b> Concepts, Hardwired Control, Examples on hardwired control (Multiplier control unit), CPU control unit, Microprogrammed Control Unit, Example based on micro-programmed control unit, Concepts in Pipeline control	6

III	<b>Designing Memory Blocks</b> ROM, Internal Structure, Rom control inputs and timing, Static RAM, Internal Structure, Timing, Dynamic RAM, Timing, Memory Systems (Multilevel memories, Address translation, replacement policies), Caches (Address mapping, Associative, Direct and set-associative mapping), Cache performance	7
IV	<b>Processor Design</b> Introduction, Microcomputer Organization, Microprocessor Organization, Set of Instructions, Addressing Modes, Designing instruction, stack, subroutines and interrupt, Input-Output interface, Serial and parallel communication with processor, Direct Memory Access	6
V	<b>PLDs and Their Architectures</b> Introduction to Programmable Logic Devices, Field Programmable Gate Arrays, FPGA Architectures (Xilinx Spartan Series, Altera Stratix Series) involving Configurable Logic Blocks, I/O blocks, Programmable interconnects.	4
VI	<b>Data Converters: DAC</b> Binary weighted Resistor , R/2R ladder, Performance metrics of DAC (Resolution, Settling time, linearity, speed and Errors) <b>ADC</b> – Flash ADC, Successive Approximation ADC, Single slope ADC, Dual Slope ADC, ADC specifications (Quantization error, Integral non-linearity error, Gain and Offset Error, Signal to Noise Ratio, Dynamic Range, Effective number of bits, Bit Error Rate, Figure of Merit)	9

#### Textbooks

- |   |   |
|---|---|
| 1 | <i>Morris Mano, "Digital Logic and Microprocessoor Design", PHI, 2001</i>                         |
| 2 | <i>John Wakerley, "Digital Design , Principles and Practices", PHI, 2005 3.</i>                   |
| 3 | <i>Hayes, "Computer Architecture and Organization", McGraw Hill, 3<sup>rd</sup> Edition, 2012</i> |

#### References

- |   |  |
|---|--|
| 1 | <i>Frank Vahid "Digital Electronics" Wiley Publication. 2012</i>   |
| 2 | <i>Enoch O. Hwang, "Digital Logic and Microprocessoor Design with VHDL", Thomson Publication, 2007 Reprint</i> |

#### Useful Links

- |   |  |
|---|--|
| 1 | <a href="http://www.xilinx.com">www.xilinx.com</a> |
| 2 | <a href="http://www.altera.com">www.altera.com</a> |

#### CO-PO Mapping

	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
<b>CO1</b>		2												
<b>CO2</b>	3													
<b>CO3</b>		3												
<b>CO4</b>		3												
<b>CO5</b>			3			1	1							3

The strength of mapping is to be written as 1: Low, 2: Medium, 3: High  
Each CO of the course must map to at least one PO.

### **Assessment**

The assessment is based on MSE, ISE and ESE.

MSE shall be typically on modules 1 to 3.

ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.

ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.

For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

# Walchand College of Engineering, Sangli

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**AY 2023-24**

## Course Information

<b>Programme</b>	B. Tech. (Electronics Engineering)
<b>Class, Semester</b>	Third Year B. Tech., Sem.VI
<b>Course Code</b>	6EN323
<b>Course Name</b>	Power Electronics
<b>Desired Requisites:</b>	Basic Electrical Engineering, Circuit Theory

<b>Teaching Scheme</b>		<b>Examination Scheme (Marks)</b>			
<b>Lecture</b>	3 Hrs/week	<b>MSE</b>	<b>ISE</b>	<b>ESE</b>	<b>Total</b>
<b>Tutorial</b>	-	30	20	50	100
<b>Practical</b>	-				
<b>Interaction</b>	-	<b>Credits: 3</b>			

## Course Objectives

<b>1</b>	<b>Explain</b> the working of modern power semiconductor devices and their applications.
<b>2</b>	<b>Explain</b> the working of power converter circuits like controlled rectifier, inverter, AC voltage controller and chopper and provide the knowledge of performance parameters of converters in the analysis of their performance.
<b>3</b>	<b>Explain</b> the use of different power control techniques like converters, choppers, inverters and cycloconverters to control the speed of DC motors and Induction motors.
<b>4</b>	<b>Illustrate</b> to choose an appropriate power electronic circuit and a power semiconductor device while designing an electrical power control system.

## Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

<b>CO1</b>	<b>Explain</b> the working of power semiconductor devices such as SCR, GTO, Power MOSFET and IGBT.	Understand
<b>CO2</b>	<b>Analyze</b> the performance of controlled rectifiers, DC to DC converters, Inverters, AC to AC converter.	Analyze
<b>CO3</b>	<b>Evaluate</b> the performance parameters of controlled rectifier, DC to DC converter, DC to AC converter and AC to AC converter.	Evaluate
<b>CO4</b>	<b>Analyze</b> the speed control techniques/ methods for AC and DC motors.	Analyze

<b>Module</b>	<b>Module Contents</b>	<b>Hours</b>
I	<b>Power Semiconductor Devices</b> SCR (Silicon Controlled Rectifier): two transistor model, protection circuits, series and parallel operation of SCR, triggering and commutation circuits; GTO, TRIAC, DIAC, Power Diode, Power BJT, Power MOSFET, IGBT.	7
II	<b>Phase Controlled Rectifiers</b> Single phase half and full wave controlled rectifier with R and RL load, Single phase half controlled (semiconductor) and fully controlled bridge rectifier. Three phase half wave controlled rectifier with resistive load, three phase half controlled and fully controlled bridge rectifier with R and RL load; Calculation of performance parameters of line commutated converters: Fourier analysis; effect of source impedance on the performance of controlled rectifiers.	9
III	<b>Inverters and AC voltage Controllers</b> Single phase half and full bridge inverter using transistor/MOSFET/IGBT, performance parameters, Fourier analysis of inverter output voltage; Three phase bridge inverter- $120^{\circ}$ and $180^{\circ}$ conduction mode; PWM inverters; Series and Parallel resonant inverter. AC voltage controllers: single phase and three phase AC voltage controllers, AC power control using TRIAC; Cycloconverters: single phase to single phase, three phase to single phase, three phase to three phase cycloconverter.	8
IV	<b>DC to DC converters</b> Choppers: principles of operation, control strategies: TRC, current limit control; types of chopper, step up chopper, multiphase chopper; SMPS.	4

V	<b>D.C. Motor Control</b> Equivalent circuit, speed torque characteristics (separately excited and series motor), operating modes, single phase and three phase controlled rectifier fed drives; four quadrant drive-single phase and three phase dual converter; Chopper-fed DC drive.	6
VI	<b>A.C. Motor Control</b> Equivalent circuit, speed torque characteristics, speed control methods-stator voltage control, rotor voltage control, frequency control, stator voltage and frequency control (V/F); Vector Control.	6

#### Text Books

1	M. D. Singh & K. B. Khanchandani, "Power Electronics", Second Edition, Tata McGraw-Hill Publishing Company Ltd., New Delhi, 2007.
2	M.H. Rashid, "Power Electronics: Circuits, Devices & Applications", Third Edition, PHI, New Delhi, 2008.
3	P. S. Bimbhra, "Power Electronics", Third Edition, Khanna Publishers, 2004.
4	

#### References

1	P. C. Sen, "Power Electronics", First Edition, Tata McGraw Hill Publishing Company Ltd, 2008.
2	V. R. Moorthi, "Power Electronics-Devices, Circuits and Industrial Applications", Oxford University Press, 2010.
3	Ned Mohan, T. M. Undeland, W. P. Robbins, "Power electronics-Converters, Applications and Design", Third Edition, John Wiley and Sons Inc., 2003.
4	

#### Useful Links

1	<a href="https://nptel.ac.in/courses/108/105/108105066/#">https://nptel.ac.in/courses/108/105/108105066/#</a>
2	<a href="https://nptel.ac.in/courses/108/108/108108077/">https://nptel.ac.in/courses/108/108/108108077/</a>
3	<a href="https://nptel.ac.in/courses/108/102/108102145/">https://nptel.ac.in/courses/108/102/108102145/</a>
4	

#### CO-PO Mapping

	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
<b>CO1</b>	2													
<b>CO2</b>	2	3	1											2
<b>CO3</b>	2	3												
<b>CO4</b>		2	2											2

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High

Each CO of the course must map to at least one PO.

#### Assessment

The assessment is based on MSE, ISE and ESE.

MSE shall be typically on modules 1 to 3.

ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.

ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.

For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

# Walchand College of Engineering, Sangli

*(Government Aided Autonomous Institute)*

**AY 2022-23**

## Course Information

<b>Programme</b>	B.Tech. (Electronics Engineering)
<b>Class, Semester</b>	Third Year B. Tech., Sem -VI
<b>Course Code</b>	6EN371
<b>Course Name</b>	Digital System Architecture Lab
<b>Desired Requisites:</b>	Digital Electronics Lab

<b>Teaching Scheme</b>		<b>Examination Scheme (Marks)</b>			
<b>Practical</b>	2 Hrs/ Week	<b>LA1</b>	<b>LA2</b>	<b>Lab ESE</b>	<b>Total</b>
<b>Interaction</b>		30	30	40	100
<b>Credits: 2</b>					

## Course Objectives

- 1** To know the HDL language for Digital Design
- 2** To understand the difference in HDL and other high level programming language
- 3** To understand the concept in simulation and synthesis

## Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

<b>CO1</b>	The students will be able to design the basic digital circuits and test them.	Understand
<b>CO2</b>	Able to develop designed circuit using VHDL	Apply
<b>CO3</b>	Able to implement the control unit using VHDL	Analyse

## List of Experiments / Lab Activities/Topics

**VERILOG:** Introduction to VERILOG, Program structure, Attributes, Functions and Procedures, Types of VERILOG architectures(Structural, Data flow, Behavioral), VERILOG concurrent and sequential constructs, Combinational and Sequential logic design using Verilog

### List of Lab Activities:

- 1 Introduction to Xilinx with sample experiment in Verilog
- 2 1 bit full adder using 1 bit half adder as a component
- 3 4 bit full adder using 1 bit full adder as a component.
- 4 1 bit full adder using 8:1 multiplexer as component
- 5 1 bit full adder using 1:8 demux as component
- 6 Implementation of 4:1 mux using 2:1 mux as a component
- 7 Implementation of demultiplexer IC 74138
- 8 4 bit comparator
- 9 Implementation of flip flops
- 10 4-bit Counter using D-f/f
- 11 Counter using operators
- 12 UP counter and DOWN counter
- 13 Shift registers
- 14 Universal Shift register

## Textbooks

1	Douglas Perry , "VERILOG", , Tata McGraw-Hill,
2	Charles H Roth, "Digital System Design Using VHDL", Cengage Learning India

## References

1	Steafan,"Fundamentals of Digital Logic Using VERILOG ", McGraw Hill
2	Manjita Srivastava ,”Digital Design: HDL-Based Approach”,Cengage Learning India

Useful Links												
1	www.xilinx.com											
2	www.altra.com											

CO-PO Mapping														
	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
<b>CO1</b>	3													
<b>CO2</b>		3												
<b>CO3</b>						1	1							2

The strength of mapping is to be written as 1,2,3; where, 1: Low, 2: Medium, 3: High  
Each CO of the course must map to at least one PO, and preferably to only one PO.

Assessment				
There are three components of lab assessment, LA1, LA2 and Lab ESE. IMP: Lab ESE is a separate head of passing.(min 40 %), LA1+LA2 should be min 40%				
Assessment	Based on	Conducted by	Typical Schedule	
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 8 Marks Submission at the end of Week 8	30
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 9 to Week 16 Marks Submission at the end of Week 16	30
Lab ESE	Lab activities, journal/ performance	Lab Course Faculty and External Examiner as applicable	During Week 18 to Week 19 Marks Submission at the end of Week 19	40

Week 1 indicates starting week of a semester. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming, and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments and related activities if any.

# Walchand College of Engineering, Sangli

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**AY 2023-24**

## Course Information

<b>Programme</b>	B. Tech. (Electronics Engineering)
<b>Class, Semester</b>	Third Year B. Tech., Sem. VI
<b>Course Code</b>	6EN372
<b>Course Name</b>	Power Electronics Lab
<b>Desired Requisites:</b>	Basic Electrical Engineering, Circuit Theory

<b>Teaching Scheme</b>		<b>Examination Scheme (Marks)</b>			
<b>Practical</b>	2 Hrs/Week	<b>LA1</b>	<b>LA2</b>	<b>Lab ESE</b>	<b>Total</b>
<b>Interaction</b>	-	30	30	40	100
<b>Credits: 1</b>					

## Course Objectives

<b>1</b>	Explain the V-I characteristics of power semiconductor devices and their use as a switch.
<b>2</b>	Demonstrate the operating and handling procedure (i.e. safety measures) of power electronic experimental set ups.
<b>3</b>	Explain the need of isolating power circuit ground and control circuit ground (use of Powerscope or isolation transformer) during observation of waveforms and measurement of input and output voltage of a power electronic circuit i.e. controlled rectifier, inverter and chopper.
<b>4</b>	Demonstrate the use of simulation software (PSIM, MATLAB, PSPICE) in the analysis and design of power electronic circuits /systems.

## Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

<b>CO1</b>	Experiment with power semiconductor devices and plot its V-I characteristics.	Understand
<b>CO2</b>	Build and test power electronic circuits (controlled rectifiers, inverters, choppers)	Apply
<b>CO3</b>	Analyze the performance power electronic circuits (controlled rectifiers, inverters, choppers)	Analyze
<b>CO4</b>	Examine and compare speed control techniques/ methods for AC and DC motors.	Analyze

## List of Experiments / Lab Activities/ Topics

The primary objective of this laboratory is to impart the practical knowledge of power electronic circuits for the conversion and control of electrical energy. This laboratory course develops a basic foundation for analysis, design, test, and control of power electronics converters by experimentation and simulation.

### **List of Experiments: (Minimum 8 experiments)**

1. Study of power semiconductor devices: SCR, Power MOSFET, IGBT.
2. SCR triggering circuits: R, RC, and UJT
3. Single phase half controlled bridge rectifier.
4. Single phase fully controlled bridge rectifier.
5. Single phase transistorized inverter.
6. Single phase to Single phase Cycloconverter.
7. Design and implementation of a Type-A chopper (Power MOSFET based) circuit.
8. AC power control using TRIAC.
9. Single/ Three phase controlled rectifier fed DC drive.
10. Chopper fed DC drive.
11. Three phase induction motor drive.
12. Four quadrant DC drive (Dual converter).
13. Speed control of brushless DC motor.
14. Simulation of Controlled Rectifier and Three Phase Inverter Circuit using MATLAB/ PSIM.

## Text Books

<b>1</b>	M.H. Rashid, “ <i>Power Electronics: Circuits, Devices &amp; Applications</i> ”, Third Edition, PHI, New Delhi, 2008.
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2	M. D. Singh & K. B. Khanchandani, "Power Electronics", Second Edition, Tata McGraw-Hill Publishing Company Ltd., New Delhi, 2007.
3	V. R. Moorthi, "Power Electronics: Devices, Circuits and Industrial Applications", Oxford University Press, 2010.
4	

### References

1	D. R. Grahams, J. C. Hey, "SCR Manual", Fifth Edition, General Electric, New York, 1972.
2	<a href="https://www.powersimtech.com/wp-content/uploads/2021/01/PSIM-User-Manual.pdf">https://www.powersimtech.com/wp-content/uploads/2021/01/PSIM-User-Manual.pdf</a>
3	
4	

### Useful Links

1	<a href="https://powersimtech.com/products/psim/capabilities-applications/">https://powersimtech.com/products/psim/capabilities-applications/</a>
2	<a href="https://in.mathworks.com/solutions/power-electronics-control/power-electronics-simulation.html">https://in.mathworks.com/solutions/power-electronics-control/power-electronics-simulation.html</a>
3	<a href="https://www.plexim.com/products/plecs">https://www.plexim.com/products/plecs</a>
4	

### CO-PO Mapping

	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
<b>CO1</b>	1			3										
<b>CO2</b>				3	3									2
<b>CO3</b>		1		3	3									2
<b>CO4</b>	1			3	2									

The strength of mapping is to be written as 1,2,3; where, 1: Low, 2: Medium, 3: High

Each CO of the course must map to at least one PO, and preferably to only one PO.

### Assessment

There are three components of lab assessment, LA1, LA2 and Lab ESE.

IMP: Lab ESE is a separate head of passing.(min 40 %), LA1+LA2 should be min 40%.

Assessment	Based on	Conducted by	Typical Schedule	Marks
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 6 Marks Submission at the end of Week 6	30
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 7 to Week 12 Marks Submission at the end of Week 12	30
Lab ESE	Lab activities, attendance, journal	Lab Course Faculty	During Week 15 to Week 18 Marks Submission at the end of Week 18	40

Week 1 indicates starting week of a semester. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming, and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments and related activities if any.

# Walchand College of Engineering, Sangli

*(Government Aided Autonomous Institute)*

**AY 2023-24**

## Course Information

<b>Programme</b>	B. Tech. (Electronics Engineering)
<b>Class, Semester</b>	Third Year B. Tech., Sem-VI
<b>Course Code</b>	6EN342
<b>Course Name</b>	Mini Project-2
<b>Desired Requisites:</b>	ECAD-I, ECAD-II, Digital Signal Processing, Embedded System Design, Digital Signal Processing

## Teaching Scheme

## Examination Scheme (Marks)

<b>Practical</b>	2 Hrs/ Week	<b>LA1</b>	<b>LA2</b>	<b>Lab ESE</b>	<b>Total</b>
<b>Interaction</b>	-	30	30	40	100

**Credits: 1**

## Course Objectives

<b>1</b>	To provide students hands on experience on, troubleshooting, maintenance, fabrication, innovation, record keeping, documentation etc. thereby enhancing the skill and competency part of technical education.
<b>2</b>	To create an Industrial environment and culture within the institution.
<b>3</b>	To inculcate innovative thinking and practice based learning and thereby preparing students for their final year project.
<b>4</b>	To set up self-maintenance cell within departments to ensure optimal usage of infrastructure Facilities.

## Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

<b>CO1</b>	Choose, Initiate and manage a minor project.	Understand
<b>CO2</b>	Propose research problem and present it in a clear and distinct manner through different oral, written and design techniques.	Apply
<b>CO3</b>	Construct the circuit using hardware and/or software.	Create
<b>CO4</b>	Execute the project and comment upon the results of it.	Analyze

## List of Experiments / Lab Activities/ Topics

### Mini Project Description:

A project group shall consist of normally 3 students per group. The mini project will involve the design, construction, and debugging of an electronic system approved by the department. Each student should conceive, design and develop the idea leading to a project/product. **The theme of the project should be related to electronics engineering discipline to be decided by the students based on the societal needs after an exhaustive survey.**

Each student must keep a project notebook/logbook. The project notebooks will be checked periodically throughout the semester, as part of in-semester-evaluation. The student should submit a soft bound report at the end of the semester. The final product as a result of mini project should be demonstrated at the time of examination.

## Textbooks

1	Electronics Projects For Dummies, by Earl Boysen and Nancy Muir, Published by Wiley Publishing, Inc., 2006
2	Make: Electronics, by Charles Platt, Published by Maker Media, 2015
3	
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## References

1	A. E. Ward, J.A.S. Angus, "Electronic Product Design", Stanley Thrones (Publishers) Limited, 1996.
2	Paul Horowitz, Winfield Hill, "The Art of Electronics", Cambridge University Press, 1989

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<b>Useful Links</b>	
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CO-PO Mapping														
	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
<b>CO1</b>	3	3								2	2			2
<b>CO2</b>			3		2									
<b>CO3</b>			3		2						1		1	1
<b>CO4</b>		2							3	3				

The strength of mapping is to be written as 1,2,3; where, 1: Low, 2: Medium, 3: High

Each CO of the course must map to at least one PO, and preferably to only one PO.

Assessment				
Assessment	Based on	Conducted by	Typical Schedule	Marks
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 8 Marks Submission at the end of Week 8	30
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 9 to Week 16 Marks Submission at the end of Week 16	30
Lab ESE	Lab activities, journal/ performance	Lab Course Faculty and External Examiner as applicable	During Week 18 to Week 19 Marks Submission at the end of Week 19	40

Week 1 indicates starting week of a semester. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming, and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments and related activities if any.

# Walchand College of Engineering, Sangli

*(Government Aided Autonomous Institute)*

**AY 2023-24**

## Course Information

<b>Programme</b>	B.Tech. (Electronics Engineering)
<b>Class, Semester</b>	Third Year B. Tech., Sem VI
<b>Course Code</b>	6EN331
<b>Course Name</b>	Mobile Communication Engineering
<b>Desired Requisites:</b>	Probability Theory and statistics, Digital Communication Engineering

Teaching Scheme		Examination Scheme (Marks)			
Lecture	3 Hrs/week	MSE	ISE	ESE	Total
Tutorial	-	30	20	50	100
<b>Credits: #</b>					

## Course Objectives

<b>1</b>	To introduce the concepts and techniques associated with Wireless Cellular Communication systems
<b>2</b>	To familiarize with state of art standards used in wireless cellular systems

## Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,		
<b>CO1</b>	Apply fundamentals of cellular system design to improve performance of cellular network	Apply
<b>CO2</b>	Distinguish between different multiple access technology	Analyze
<b>CO3</b>	Study evolution of mobile communication generation standards	Analyze

Module	Module Contents	Hours
I	<b>Mobile Radio Propagation</b> Large Scale Path Loss - Free Space Propagation Model, Relating Power to Electric Field, Three Basic Propagation Mechanisms -Reflection (Ground Reflection), Wave Propagation and its types: Ground wave, space wave and sky wave propagation, Diffraction, Scattering, Practical Link Budget, Fading and Multipath.	6
II	<b>Basics of Antenna</b> Basic Antenna Parameters – Patterns, Beam Area, Radiation Intensity, Beam Efficiency, Directivity-Gain-Resolution, Antenna Apertures, Effective Height. Fields from Oscillating Dipole, Field Zones, Front - to-back Ratio, Antenna Theorems, Radiation, Retarded Potentials – Helmholtz Theorem	6
III	<b>The Cellular Concept – System Design Fundamentals</b> Introduction of Cells, Channel Reuse, SIR Calculations, Traffic Handling Capacity: Erlang Performance, Cellular system design, Cochannel interference ratio, Co channel interference reduction techniques and methods to improve cell coverage, Frequency management and channel assignment, concepts of cell splitting, handover in cellular system.	9
IV	<b>Multiple Access Technologies</b> Frequency Division Multiple access (FDMA), Time Division Multiple access (TDMA), Code Division Multiple access (CDMA), Orthogonal Frequency Division, spectral efficiency calculations, comparison of T/F/CDMA technologies based on their signal separation techniques, advantages, disadvantages and application areas.	4
V	<b>Fundamentals of GSM</b> GSM standard. The basic architecture of a GSM network, Interfaces in a GSM network. Air interface in GSM, logical and physical channels. Radio Network GSM system functions TRAU, BSC, BTS and MS. The central network functions VLR, HLR, AUC and EIR.	8

VI	<b>5G Technology</b> HSPA and LTE – Architecture – Radio interface and channels – Resource mapping – Session, mobility and security procedures – LTE Advanced – Heterogeneous Networks – Internetworking, IP based coupling Architecture - Multimode terminals and intersystem handover	7
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#### Textbooks

1	T.S.Rappaport, “ <i>Wireless Communications Principles and Practice</i> ”, II Ed. PHI, Publications, 2010
2	Prashant Kumar Patra, Sanjit Kumar Dash, “ <i>Mobile Computing</i> ”, 2nd Edition, Scitech, 2014
3	V.K.Garg, J.E.Wilkes, “ <i>Principle and Application of GSM</i> ” Pearson Education, 1999
4	

#### References

1	William C. Y. Lee, “ <i>Mobile Communication Engineering: Theory and Applications</i> ”, 2nd Edition, McGraw Hill Publication, 1997
2	Iti Saha Misra, “ <i>Wireless Communication and Networks – 3G and Beyond</i> ”, Mc Graw Hill Education, Second Edition, 2013
3	Mischa Schwartz, “ <i>Mobile Wireless Communication</i> ”, 1st Edition, Cambridge University Press, 2009.
4	Antenna Theory - C.A. Balanis, John Wiley & Sons, 3rd Ed., 2005.

#### Useful Links

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#### CO-PO Mapping

	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
<b>CO1</b>		3												
<b>CO2</b>			3										3	
<b>CO3</b>		3												

The strength of mapping is to be written as 1: Low, 2: Medium, 3: High

Each CO of the course must map to at least one PO.

#### Assessment

The assessment is based on MSE, ISE and ESE.

MSE shall be typically on modules 1 to 3.

ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.

ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.

For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

**Walchand College of Engineering, Sangli**  
*(Government Aided Autonomous Institute)*

**AY 2023-24**

**Course Information**

<b>Programme</b>	B.Tech. (Electronics Engineering)
<b>Class, Semester</b>	Final Year B. Tech., Sem VII
<b>Course Code</b>	6EN332
<b>Course Name</b>	Digital System Engineering
<b>Desired Requisites:</b>	

<b>Teaching Scheme</b>		<b>Examination Scheme (Marks)</b>			
<b>Lecture</b>	3 Hrs/week	<b>MSE</b>	<b>ISE</b>	<b>ESE</b>	<b>Total</b>
<b>Tutorial</b>	0 Hrs/week	30	20	50	100
<b>Credits: 3</b>					

**Course Objectives**

<b>1</b>	To understand the fundamental issues such as power, noise, signaling and timing associated with high speed digital systems.
<b>2</b>	To analyze the effect of parasitic of wires/interconnects in restricting the high speed performance of digital circuits and design the approaches to tackle this associate problem by using their engineering models
<b>3</b>	To comprehend the different sources of interference (noise) in digital systems and apply engineering/statistical models of these to compute and compare bit error rates
<b>4</b>	Understand the significance of signaling & timing issues and apply the knowledge of encoding a signal for error-free transfer of information (bits) from one location to another

**Course Outcomes (CO) with Bloom's Taxonomy Level**

At the end of the course, the students will be able to,

<b>CO1</b>	Understand Interconnects as design objects, Noise in digital systems and its impact to system operation	II
<b>CO2</b>	Analyze Timing and synchronization for functional operations and signalling	IV
<b>CO3</b>	Distinguish Power distribution schemes for low noise	IV
<b>CO4</b>	Explain Signal and signalling conventions for on-chip and off-chip communication	II

<b>Module</b>	<b>Module Contents</b>	<b>Hours</b>
I	<b>Wires:</b> Geometry and Electrical properties, Electrical models of wires (Ideal wire, Transmission line), Simple transmission lines (RC, lossless LC, lossy LRC transmission lines, Dielectric absorption), Special transmission lines (Multi drop buses, Balanced Transmission lines, Common and differential mode impedance, Isolated lines)	7

II	<b>Noise in Digital System:</b> Noise sources in a digital system, Power Supply Noise, Cross-talk, Inter-symbol Interference, Noise due to other sources (Alpha particles, Electro-magnetic Interference, Process variation, Thermal Noise, Shot Noise, Flicker or 1/f Noise), Managing noise.	7
III	<b>Signaling Conventions:</b> CMOS and Low swing current mode signaling system, Considerations in transmission system design, Signaling modes for transmission lines, Transmitter signaling methods, Receiver signal detection, Source termination, Under-terminated Drivers, Differential Signaling, Signaling over capacitive transmission medium, Signal encoding	7
IV	<b>Timing Convention:</b> Conventional Synchronous system and closed loop pipelined system, considerations in timing design, Timing fundamentals, Timing properties of combinational logic and clock storage elements, Eye diagram, Encoding Timing (Signals and Events), Open loop synchronous timing, Closed loop timing, Phase locked loops, Clock Distribution	6
V	<b>Synchronization:</b> Synchronization Fundamentals, Applications of synchronization (Arbitration of asynchronous signals, Sampling asynchronous signals, Crossing clock domains), Synchronization failure and meta-stability, Synchronizer Design (Mesochronous, Plesiochronous, Periodic Asynchronous)	6
VI	<b>Power Distribution:</b> The power supply network (Local loads, Signal loads), Local Regulation, Logic loads and on-chip power supply distribution (Logic current profile, IR drops, Area Bonding, On-chip by-pass capacitor), Power supply isolation (Supply-supply isolation, Signal-supply isolation), Bypass capacitors, Power Distribution system	6

#### Textbooks

1	<i>Digital System Engineering</i> , William Dally and John Poulton, Cambridge University Press, Reprint 2007
2	
3	
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References	
1	<i>High Speed Digital Design, A Handbook of Black Magic</i> , Howard W. Johnson, Martin Graham, Prentice Hall PTR, Englewood Cliffs, NJ 0763.
2	<i>High Speed Digital System Design: Interconnect Theory and Design Practices</i> Stephen H. Hall, Garrett W. Hall, James A. McCall, Wiley-IEEE Press (ISBN: 978-0-471-36090-2)
3	
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Useful Links	
1	<a href="http://cva.stanford.edu/books/dig_sys_engr/">http://cva.stanford.edu/books/dig_sys_engr/</a>
2	
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CO-PO Mapping													PSO	
	Programme Outcomes (PO)												1	2
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
<b>CO1</b>	3													
<b>CO2</b>	3													
<b>CO3</b>				3										
<b>CO4</b>				3										

The strength of mapping is to be written as 1: Low, 2: Medium, 3: High  
Each CO of the course must map to at least one PO.

Assessment													
The assessment is based on MSE, ISE and ESE.													
MSE shall be typically on modules 1 to 3.													
ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.													
ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.													
For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)													

# Walchand College of Engineering, Sangli

*(Government Aided Autonomous Institute)*

**AY 2023-24**

## Course Information

<b>Programme</b>	B.Tech. (Electronics Engineering)
<b>Class, Semester</b>	Third Year B. Tech., Sem VI
<b>Course Code</b>	6EN333
<b>Course Name</b>	Professional Elective 3- Design and Analysis of Algorithm
<b>Desired Requisites:</b>	Data Structure and Algorithms

## Teaching Scheme

## Examination Scheme (Marks)

Lecture	3 Hrs/week	MSE	ISE	ESE	Total
Tutorial	-	30	20	50	100
<b>Credits: 3</b>					

## Course Objectives

<b>1</b>	To provide different algorithm approaches like static, dynamic, iterative and recursive techniques.
<b>2</b>	To explain Comparative features of algorithms on the basis of space, time computational complexities,
<b>3</b>	To explain the selection criteria for identifying, formulating and applying a typical algorithm for given problem.
<b>4</b>	

## Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

<b>CO1</b>	Interpret different algorithm approaches like static, dynamic, iterative and recursive techniques.	Apply
<b>CO2</b>	Compare the different algorithms on the basis of space, time computational complexities	Analyze
<b>CO3</b>	Identify the optimum algorithm for given problem.	Analyze
<b>CO4</b>		

Module	Module Contents	Hours
I	<b>Introduction</b> Static and dynamic structures, stacks, queues, dynamic memory allocation and pointers, linked stacks and queues, trees and recursion, Hashing:- Sparse-table, hash function, collision resolution with open addressing and collision resolution by chaining	4
II	<b>Searching and Sorting Algorithms</b> Sequential search, Binary search, Comparison of trees, Insertion sort, Selection sort(Heap sort), Shell sort. Computational Complexity, lower bound, & comparison of searching and sorting algorithm	8
III	<b>Divide and Conquer</b> Merge sort, quick sort (portioning), Matrix multiplication algorithm, Limitation of divide and conquer. Computational complexity of divide and conquer algorithms.	8
IV	<b>Dynamic Programming &amp; Greedy Approach</b> Binomial Coefficients, Floyd's algorithm for shortest path, Chain matrix multiplication, optimal binary search trees and the traveling salesperson problem, Dynamic programming approach to 0-1 knapsack problem, Minimum spanning traces algorithms and their Comparison.	8

V	<b>Back Tracking &amp; Branch and Bound</b> Back tracking techniques, the n-queens problem, Back tracking algorithm's efficiency using Monte Carlo algorithm. Graph coloring, the Hamiltomian circuits' problem. Backtracking Algorithm for 0-1 Knapsack problem and its comparison	7
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VI	<b>Theory of NP</b> The three general categories of problems. The sets P & NP. NP complete problems, NP-Hard, NP-easy, NP – Equivalent problems, NP Hard problems	4
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### Textbooks

1	Ellis Horowitz, Sartaj Sahani, Sangutheraar "Fundamentals of Computer Algorithms", Rajasekaran., Galgotia Publication Ltd, 2010
2	I. Chandra Mohan, "Design and Analysis of Algorithms", PHI Publication, 2012.
3	Horowitz and Sahni, "Analysis of Computer Algorithms", Galgotia Publishers., 2007
4	

### References

1	Richard E. Neapolita & Kumarss Naimipour, "Foundation of Algorithms", (Northeastern Illinois University), D.C. Heath and Company, Publication, 1996.
2	Robert L. Kruse & Brunce P. Leung et. Al, "Data Structures and Program Design" CPHI Publication, 1984.
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### Useful Links

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### CO-PO Mapping

	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
<b>CO1</b>		1												
<b>CO2</b>	2													2
<b>CO3</b>			2											
<b>CO4</b>		1												

The strength of mapping is to be written as 1: Low, 2: Medium, 3: High

Each CO of the course must map to at least one PO.

### Assessment

The assessment is based on MSE, ISE and ESE.

MSE shall be typically on modules 1 to 3.

ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.

ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.

For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

**Walchand College of Engineering, Sangli**  
*(Government Aided Autonomous Institute)*

**AY 2023-24**

**Course Information**

<b>Programme</b>	B.Tech. (Electronics Engineering)
<b>Class, Semester</b>	Third Year B. Tech., Sem VI
<b>Course Code</b>	6EN334
<b>Course Name</b>	Communication Network Protocols
<b>Desired Requisites:</b>	Digital Communication, Data Communication

<b>Teaching Scheme</b>		<b>Examination Scheme (Marks)</b>			
<b>Lecture</b>	2 Hrs/week	<b>MSE</b>	<b>ISE</b>	<b>ESE</b>	<b>Total</b>
<b>Tutorial</b>	1 Hrs/week	30	20	50	100
<b>Credits: 3</b>					

**Course Objectives**

- 1** To develop an understanding of computer networking basics
- 2** To be exposed to the TCP/IP protocol suite
- 3** To develop an understanding of different components of computer networks, various protocols, modern technologies and their applications.
- 4** To gain conceptual understanding of Software Defined Networks (SDN)

**Course Outcomes (CO) with Bloom's Taxonomy Level**

At the end of the course, the students will be able to,

<b>CO1</b>	Design a small TCP/IP Network	Apply
<b>CO2</b>	Identify security issues and suggest suitable solution	Analyze
<b>CO3</b>	Explain concept of cloud and its models.	Understand
<b>CO4</b>	Explain OpenFlow challenges in SDN, and developments in SDN	Understand

<b>Module</b>	<b>Module Contents</b>	<b>Hours</b>
I	<b>Introduction to Network and Data Link Layer</b> Introduction to Network, Transmission media, Topology, Switching techniques. OSI Model, TCP/IP Model Data Link layer design issues, Logical Link Control, Medium Access Control, Elementary Data link layer protocols, Sliding window protocol , Medium access sub layer- Multiple access protocols.	7
II	<b>Internet Protocol : IPv4 :</b> IP Datagram Formats - Data and Fragmentation - Address Masks- Prefixes- and Subnetworks - Network Address Translation (NAT) - IP Switching and Routing - Local Delivery and Loopbacks - Address Resolution Protocol ICMP.	8
III	<b>Transport layer protocols</b> UDP and TCP segments, comparison, TCP state flow diagram, TCP flow control, congestion control, error control. TCP Timers.	7
IV	<b>Application layer protocols:</b> Audio video streaming over IP (RTP,RTCP, SCTP), Application layer protocols, HTTP, SMTP, SNMP, FTP.	6
V	<b>Security:</b> The Need of Security, Security Approaches, Principal of Security, Types of Attacks. Network Security: Brief Introduction to Firewalls, IP Security, Virtual Private Networks (VPN)	6

VI	<b>Cloud Computing and Software Defined Networking(SDN):</b> Business Drivers - Technology Innovations - Basic Concepts and Terminology Cloud Characteristics - Cloud Delivery Models - Cloud Deployment Models, Basics and Open flow, SDN Controller, SDN challenges, SDN and virtualization.	6
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#### Textbooks

1	B A Forouzan," Computer Networks", McGraw Hill Education 2016
2	Chuck Black, "Software defined Networking", Elsevier 2014
3	
4	

#### References

1	Wayne Tomasi, "Introduction to Data Communication and Networking", 1/e, Pearson Education .
2	Greg Tomsho, Ed Tittel, David Johnson. "Guide to Networking Essentials", fifth edition, Thomson India Learning, 2007.
3	
4	

#### Useful Links

1	<a href="https://www.cloudflare.com/en-in/learning/ddos/glossary/tcp-ip/">https://www.cloudflare.com/en-in/learning/ddos/glossary/tcp-ip/</a>
2	<a href="https://networkengineering.stackexchange.com/questions/63278/what-layers-of-the-tcp-ip-model-does-an-sdn-involve">https://networkengineering.stackexchange.com/questions/63278/what-layers-of-the-tcp-ip-model-does-an-sdn-involve</a>
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#### CO-PO Mapping

	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
<b>CO1</b>			2										2	
<b>CO2</b>		2												1
<b>CO3</b>		1												1
<b>CO4</b>	1	1												1

The strength of mapping is to be written as 1: Low, 2: Medium, 3: High

Each CO of the course must map to at least one PO.

#### Assessment

The assessment is based on MSE, ISE and ESE.

MSE shall be typically on modules 1 to 3.

ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.

ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.

For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

# Walchand College of Engineering, Sangli

*(Government Aided Autonomous Institute)*

**AY 2023-24**

## Course Information

<b>Programme</b>	B.Tech. (Electronics Engineering)
<b>Class, Semester</b>	Third Year B. Tech., Sem. VI
<b>Course Code</b>	6EN335
<b>Course Name</b>	Professional Elective-IV: CMOS Digital VLSI Design
<b>Desired Requisites:</b>	Digital Electronics, Electronic Circuits Analysis and Design, Microelectronics

<b>Teaching Scheme</b>		<b>Examination Scheme (Marks)</b>			
<b>Lecture</b>	2 Hrs/week	<b>MSE</b>	<b>ISE</b>	<b>ESE</b>	<b>Total</b>
<b>Tutorial</b>	1 Hr/week	30	20	50	100
<b>Practical</b>	-				
<b>Interaction</b>	-	<b>Credits: 3</b>			

## Course Objectives

- 1** *Explain* the long and short channel MOS transistor models with emphasis on unified model.
- 2** *Explain* the steps involved in manufacturing process of MOS devices.
- 3** *Explain* the considerations in optimizing the physical dimensions of MOS transistors in obtaining the trade-off between area, speed and power requirements of CMOS based systems.
- 4** *Develop* the logical and design skills of CMOS combinational and sequential logic circuits.

## Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

<b>CO1</b>	<b>Explain</b> the basic steps with theoretical principles involved in the process of manufacturing of CMOS devices.	Understand
<b>CO2</b>	<b>Model</b> sub-micron, deep submicron MOS transistors and Interconnects.	Apply
<b>CO3</b>	<b>Analyze</b> the fundamental principles involved with MOS devices to <b>design</b> CMOS inverter to meet the area, speed and power requirements.	Analyze
<b>CO4</b>	<b>Design</b> static and dynamic CMOS Combinational Logic circuits and Sequential Logic Circuits by considering the performance parameters like area, speed and power.	Create

<b>Module</b>	<b>Module Contents</b>	<b>Hours</b>
I	<b>MOS Transistor Theory</b> MOS Transistor under Static Conditions, Dynamic Behaviour, Secondary Effects, SPICE Models for MOS Transistor, Technology Scaling.	3
II	<b>Manufacturing Process for CMOS ICs</b> Photolithography, Design Rules, Packaging Integrated Circuits, Thermal Considerations in Packaging.	2
III	<b>CMOS Inverter</b> Static and Dynamic Behaviour of CMOS Inverter, Power and Energy-Delay, Impact of Technology Scaling on Inverter Metrics.	6
IV	<b>CMOS Combinational Logic Circuits</b> Static CMOS Logic Design, Dynamic CMOS Logic Design, Comparison between the two Design Styles.	6
V	<b>CMOS Sequential Logic Circuits</b> Static Latches and Registers, Dynamic Latches and Registers, Pulse Registers, Non-Bistable Sequential Circuits: Schmitt Trigger Circuit, Ring Oscillator, Voltage Controlled Oscillator.	5

VI	<b>Interconnect and Semiconductor Memories</b> Electrical Models of Wires, Lumped RC Model, Distributed rc line, Transmission Line; Memory Classification, Memory Architectures and Building Blocks, Memory Core: ROM, RAM.	4
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#### **Text Books**

1	Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "Digital Integrated Circuits-A Design Perspective", 2 <sup>nd</sup> Edition, Prentice-Hall India Learning Pvt. Limited/ Pearson Education, 2014.
2	Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", 3 <sup>rd</sup> Edition, McGraw-Hill Education (India) Pvt. Ltd., 2015.
3	
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#### **References**

1	Neil Weste, Kamran Eshraghian, "Principles of CMOS VLSI Design: Analysis and Design", Addison Wesley/Pearson Education, 2008
2	William Dally and John Poulton, "Digital System Engineering", Cambridge University Press, Reprint 2007.
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#### **Useful Links**

1	<a href="https://nptel.ac.in/courses/108/107/108107129/">https://nptel.ac.in/courses/108/107/108107129/</a>
2	<a href="https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-374-analysis-and-design-of-digital-integrated-circuits-fall-2003/index.htm">https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-374-analysis-and-design-of-digital-integrated-circuits-fall-2003/index.htm</a>
3	
4	

#### **CO-PO Mapping**

	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
<b>CO1</b>	2													1
<b>CO2</b>			2											1
<b>CO3</b>		3	2											2
<b>CO4</b>		2	3											2

The strength of mapping is to be written as 1: Low, 2: Medium, 3: High

Each CO of the course must map to at least one PO.

#### **Assessment**

The assessment is based on MSE, ISE and ESE.

MSE shall be typically on modules 1 to 3.

ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.

ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.

For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

**Walchand College of Engineering, Sangli**  
*(Government Aided Autonomous Institute)*

**AY 2023-24**

**Course Information**

<b>Programme</b>	B.Tech. (Electronics Engineering)
<b>Class, Semester</b>	Third Year B. Tech., Sem VI
<b>Course Code</b>	6EN336
<b>Course Name</b>	Professional Elective IV: Digital Image Processing
<b>Desired Requisites:</b>	Digital Signal Processing

<b>Teaching Scheme</b>		<b>Examination Scheme (Marks)</b>			
<b>Lecture</b>	2 Hrs/week	<b>MSE</b>	<b>ISE</b>	<b>ESE</b>	<b>Total</b>
<b>Tutorial</b>	1 Hr/ week	30	20	50	100
<b>Credits: 3</b>					

**Course Objectives**

- 1** To develop an overview of the field of image processing.
- 2** To illustrate the fundamental algorithms and their implementation.
- 3** To apply image processing algorithms for real problems.

**Course Outcomes (CO) with Bloom's Taxonomy Level**

At the end of the course, the students will be able to,

<b>CO1</b>	Apply digital image enhancement techniques for gray scale images and colour images	Apply
<b>CO2</b>	Analyze various image segmentation techniques	Analyze
<b>CO3</b>	Explain image restoration, de noising and image compression techniques	Evaluate
<b>CO4</b>	Identify image representation and description techniques	Understand

<b>Module</b>	<b>Module Contents</b>	<b>Hours</b>
I	<b>Introduction to Digital Image Processing</b> Fundamental steps in digital image processing- Components of Image processing system Image sensing and acquisition - Image sampling and Quantization - relationship between pixels. Image file formats	5
II	<b>Image Enhancement Techniques</b> Spatial Domain: Gray level transformation - Histogram processing, Spatial filtering - smoothing filters , sharpening filters ; Frequency Domain: Fourier transform – smoothing frequency domain filters , sharpening filters , Homographic filtering.	5
III	<b>Image Restoration, Denoising and Image Compression Techniques</b> Model of Image degradation/ restoration process Types of image blur- Noise models , Classification of Image restoration techniques, Blind de convolution, Image de noising, Median filtering, Inverse filtering, Weiner, least square, Geometric mean filters; Classification of compression techniques, Fundamentals of Information Theory, Shannon Fano coding, Huffman coding, Transform based compression.	7
IV	<b>Color Image Processing</b> Color fundamentals, color models, pseudo color image processing, basics offull-color image processing, color transforms, smoothing and sharpening, color segmentation.	7
V	<b>Image Segmentation</b> Classification of Image segmentation Techniques, Region approach to Imagesegmentation, Edge based segmentation, Classification of edges, edge detection, edge linking, Hough Transform, Clustering Techniques, Watershed Transformation.	7

VI	<b>Representation &amp; Description</b> Chain codes - Polygonal Approximations – signatures - Boundary segments - Skeletons; Boundary Descriptors - Regional descriptors.	7
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#### Textbooks

1	R.C. Gonzalez and R.E. Woods, “Digital Image Processing”, 3 <sup>rd</sup> Edition, Prentice-Hall,
2	Pratt, W.K., “Digital Image Processing”, John Wiley and Sons, New York, 1978.
3	
4	

#### References

1	A.K. Jain , “Fundamentals of Digital Image Processing”
2	M Sonka, V Hlavac and R Boyle, “Image Processing, Analysis and Machine Vision”, PWS 1999
3	
4	

#### Useful Links

1	www.nptel.com
2	
3	
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#### CO-PO Mapping

	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
<b>CO1</b>	3												2	3
<b>CO2</b>		3											2	
<b>CO3</b>	3												2	3

The strength of mapping is to be written as 1: Low, 2: Medium, 3: High

Each CO of the course must map to at least one PO.

#### Assessment

The assessment is based on MSE, ISE and ESE.

MSE shall be typically on modules 1 to 3.

ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.

ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.

For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

**Walchand College of Engineering, Sangli**  
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**AY 2023-24**

**Course Information**

<b>Programme</b>	B.Tech. (Electronics Engineering)
<b>Class, Semester</b>	Third Year B. Tech., Sem VI
<b>Course Code</b>	6OE364
<b>Course Name</b>	Cyber Physical System
<b>Desired Requisites:</b>	

<b>Teaching Scheme</b>		<b>Examination Scheme (Marks)</b>			
<b>Lecture</b>	3 Hrs/week	<b>MSE</b>	<b>ISE</b>	<b>ESE</b>	<b>Total</b>
<b>Tutorial</b>	-	30	20	50	100
<b>Credits: 3</b>					

**Course Objectives**

- 1** To illustrate the fundamental concepts of Cyber Physical Systems
- 2** To explain design of Cyber Physical Systems.
- 3** To enable the students for the design and development of CPS
- 4**

**Course Outcomes (CO) with Bloom's Taxonomy Level**

At the end of the course, the students will be able to,

<b>CO1</b>	Explain fundamentals and components of CPS	Understand
<b>CO2</b>	Analyze the components of CPS	Analyze
<b>CO3</b>	Design the CPS Systems for given Applications	Create
<b>CO4</b>		

<b>Module</b>	<b>Module Contents</b>	<b>Hours</b>
I	<b>Introduction</b> Introduction of Cyber Physical Systems, various components of CPS, Applications of Cyber Physical System, Design aspects of Cyber Physical system, Introduction to Real Time System	7
II	<b>Sensing</b> Types of sensors, Classifications of sensors, Different selection criteria of sensors, Sensor Instrumentation, Concept of Smart sensors, Wireless sensors	8
III	<b>Sensor Network and Protocol</b> Sensor Network, Wireless Sensor Network, working of WSN, routing in wireless sensor network, Gateway functions, Data Aggregations, design issues of WSN Short distance protocols : Bluetooth, BLE ( Bluetooth Smart ), Zigbee, and Industrial protocol Modbus, Mbus, 6LoWPAN, IEC68XX	5
IV	<b>Embedded system computing</b> Introduction to Embedded system, Architecture, Programming aspects, peripherals and system design	7
V	<b>CPS Security</b> CPS security, Holistic Approach to Security, Overview of Security Technologies Principal security requirements,Security Issues, Types of attacks to CPS.	5
VI	<b>CASE Study</b> Industry Automation, Smart Grid, SCADA, general case study of any CPS.	8

**Textbooks**

1	Olivier Hersent, David B. Omer Elloumi, "The Internet of Things key applications and Protocols", Wiley publications
2	
3	

4	
<b>References</b>	
1	Lars T Berger K Iniewski, "Smart Grid Applications, Communications, and Security", Wiley Publications
2	
3	
4	
<b>Useful Links</b>	
1	<a href="http://www.cyphylab.ee.ucla.edu">http://www.cyphylab.ee.ucla.edu</a>
2	
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<b>CO-PO Mapping</b>														
	<b>Programme Outcomes (PO)</b>												<b>PSO</b>	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
<b>CO1</b>	2													
<b>CO2</b>		2												
<b>CO3</b>				3										
<b>CO4</b>														

The strength of mapping is to be written as 1: Low, 2: Medium, 3: High  
 Each CO of the course must map to at least one PO.

<b>Assessment</b>													
The assessment is based on MSE, ISE and ESE.													
MSE shall be typically on modules 1 to 3.													
ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.													
ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.													
For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)													

# Walchand College of Engineering, Sangli

*(Government Aided Autonomous Institute)*

**AY 2023-24**

## Course Information

<b>Programme</b>	B.Tech. (Electronics Engineering)
<b>Class, Semester</b>	Third Year B. Tech., Sem-VI
<b>Course Code</b>	6OE365
<b>Course Name</b>	Biomedical Engineering
<b>Desired Requisites:</b>	Electronics Measurement and Instrumentation

<b>Teaching Scheme</b>		<b>Examination Scheme (Marks)</b>			
<b>Lecture</b>	3 Hrs/week	<b>MSE</b>	<b>ISE</b>	<b>ESE</b>	<b>Total</b>
<b>Tutorial</b>	-	30	20	50	100
<b>Credits: 3</b>					

## Course Objectives

- 1** To explain the basics body cell structure and different types of transducers
- 2** To explain the different types of patient monitoring system
- 3** Understand the design concept of different Medical instruments
- 4** To demonstrate different medical instruments

## Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

<b>CO1</b>	Understand CNS-PNS and Cardio pulmonary system	Understand
<b>CO2</b>	Apply proper sensors for sensing biomedical signals to biomedical instrumentation setup	Apply
<b>CO3</b>	Design ECG,EEG and EMG amplifier	Create
<b>CO4</b>	Explain block diagram of patient monitoring systems, X-ray machine, CT scan and Ultrasonography machine.	Understand

<b>Module</b>	<b>Module Contents</b>	<b>Hours</b>
I	<b>Fundamentals of Medical Instrumentation</b> Physiological Systems of the body, Sources of Biomedical signals, Basic Medical Instrumentation system, Micro-Electro-Mechanical System (Mems), Wireless Connectivity in Medical Instruments, General Constraints in design of Medical Instrumentation Systems	8
II	<b>The Origin of Bio potentials, Bio potential Electrodes &amp; Biosensors</b> Electrical activity of Excitable Cells, Functional Organization of the Peripheral Nervous System, Electrocardiogram(ECG), Electromogram(EMG), Electroencephalogram(EEG), Electroretinogram(ERG) and their recording system, Biomedical signal Analysis and Processing Techniques.	4
III	<b>Patient Monitoring Systems</b> System Concepts, Cardiac Monitor, Bedside patient Monitoring Systems, Central Monitors, Measurement of Heart rate, Measurement of Temperature, Measurement of respiration Rate, Biomedical Telemetry Systems	4
IV	<b>Modern Imaging Systems</b> X-ray machines And Digital Radiography, X-ray Computed Tomography, Nuclear Medical Imaging Systems, Magnetic Resonance Imaging Systems, Ultrasonic Imaging Systems and Thermal Imaging Systems.	8
V	<b>Assisting and Therapeutic Equipment's</b> Cardiac Pacemakers, Defibrillators, Diathermy, Hemodialysis Machines, Ventilators	8
VI	<b>Laser Application in Biomedical Field</b> The Laser, Types of Lasers, Laser Application, Laser Safety	7
<b>Textbooks</b>		

1	John. G. Webster, "Medical Instrumentation", John Wiley, 2009
2	Goddes& Baker, "Principles of Applied Biomedical Instrumentation", John Wiley, 2008
3	Carr & Brown, "Biomedical Instrumentation & Measurement", Pearson, 2004
4	

### References

1	R.S. Khandpur, "Hand book of Medical instruments", TMH, New Delhi, 1987.
2	Sanjay Guha,"Medical Electronics and Instrumentation", University Publication, 200.
3	Edwand J. Bukstein, "Introduction to Biomedical electronics" , Sane and Co. Inc, 1973
4	

### Useful Links

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### CO-PO Mapping

	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
<b>CO1</b>	3												2	
<b>CO2</b>					3	2							2	
<b>CO3</b>			3										2	
<b>CO4</b>									3				2	

The strength of mapping is to be written as 1: Low, 2: Medium, 3: High

Each CO of the course must map to at least one PO.

### Assessment

The assessment is based on MSE, ISE and ESE.

MSE shall be typically on modules 1 to 3.

ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.

ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.

For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

**Walchand College of Engineering, Sangli**  
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**AY 2023-24**

**Course Information**

<b>Programme</b>	B.Tech. (Electronics Engineering)
<b>Class, Semester</b>	Third Year B. Tech., Sem-VI
<b>Course Code</b>	6HS306
<b>Course Name</b>	Introduction to Entrepreneurship
<b>Desired Requisites:</b>	

<b>Teaching Scheme</b>		<b>Examination Scheme (Marks)</b>			
<b>Lecture</b>	2 Hrs/week	<b>LA1</b>	<b>LA1</b>	<b>ESE</b>	<b>Total</b>
<b>Tutorial</b>	-	30	30	40	100
<b>Practical</b>	-				
<b>Interaction</b>	1 Hr/week	<b>Credits: 2</b>			

**Course Objectives**

<b>1</b>	To explore the entrepreneurial mindset and culture that has been developing in companies of all sizes and industries.
<b>2</b>	To examine the entrepreneurial process from the generation of creative ideas to exploring feasibility to creation of an enterprise for implementation of the ideas.
<b>3</b>	To create and present a business plan for a technology idea.
<b>4</b>	To provide the background, tools, and life skills to participate in the entrepreneurial process within a large company, in a new venture, or as an investor.

**Course Outcomes (CO) with Bloom's Taxonomy Level**

<b>CO1</b>	<b>Exploit</b> the concept, meaning and features of entrepreneurship.	<b>Apply</b>
<b>CO2</b>	<b>Analyse</b> the business environment in order to identify business opportunities	<b>Analyse</b>
<b>CO3</b>	<b>Evaluate</b> the legal and financial conditions for starting a business venture.	<b>Evaluate</b>
<b>CO4</b>	<b>Interpret</b> the business plan, pitch to the investor and build the enterprise.	<b>Create</b>

<b>Module</b>	<b>Module Contents</b>	<b>Hours</b>
I	<b>The entrepreneurial perspective</b> The Entrepreneurial Mind-Set , Corporate Entrepreneurship , Generatingand Exploiting New Entries	5
II	<b>From idea to the opportunity</b> Creativity and the Business Idea , Identifying and Analyzing Domestic and International Opportunities , Protecting the Idea and Other Legal Issues forthe Entrepreneur	6
III	<b>From the opportunity to the business plan</b> The Business Plan: Creating and Starting the Venture , The Marketing Plan , The Organizational Plan , The Financial Plan	8
IV	<b>From the business plan to funding the venture</b> Sources of Capital , Informal Risk Capital, Venture Capital, and Going Public	4

V	<b>From funding the venture to launching, growing, and ending the new venture</b> Strategies for Growth and Managing the Implications of Growth , Accessing Resources for Growth from External Sources , Succession Planning and Strategies for Harvesting and Ending the Venture	7
VI	<b>Case Study</b> Case study of 3 to 4 successful entrepreneurs covering above theory. Case study of 2 to 3 failure entrepreneurs.	6

<b>Text Books</b>	
1	Robert D. Hisrich, Michael P. Peters, Dean A. Shepherd , "ENTREPRENEURSHIP" MGH 10 <sup>th</sup> Edition.
2	Howard , Allan , Donald "Entrepreneurship : Theory / Process / Practice" Cengage Learning 4 <sup>th</sup> Edition
3	William Bygrave , Andrew Zacharakis "Entrepreneurship" Wiley 2 <sup>nd</sup> Edition

<b>References</b>	
1	Lee A. Swanson "Entrepreneurship and Innovation Toolkit" 3 <sup>rd</sup> Edition
2	Lee A. Swanson "BUSINESS PLAN DEVELOPMENT GUIDE" 8 <sup>th</sup> Edition
3	Hitesh Jhanji "ENTREPRENEURSHIP AND SMALL BUSINESS MANAGEMENT" Lovely Professional University, India

<b>Useful Links</b>	
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<b>CO-PO Mapping</b>															
	<b>Programme Outcomes (PO)</b>												<b>PSO</b>		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
<b>CO1</b>															
<b>CO2</b>															
<b>CO3</b>															
<b>CO4</b>															

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High  
Each CO of the course must map to at least one PO.

<b>Assessment</b>													
The assessment is based on in-semester examinations in the form of online quiz and group activity of 30 marks each as LA1 and LA2. There shall be 1 End-Sem examination (ESE) of 40 marks. LA1 shall be typically on modules 1,2 and 3, and LA2 shall be typically on modules 4,5 and 6. ESE shall be on all modules.													

<b>Assessment Plan based on Bloom's Taxonomy Level (Marks)</b>				
<b>Bloom's Taxonomy Level</b>		<b>T1</b>	<b>T2</b>	<b>ESE</b>
1	Remember			Total

2	Understand				
3	Apply	5	5	12	22
4	Analyze	5	5	12	22
5	Evaluate	4	4	11	19
6	Create	6	6	25	37
<b>Total</b>		<b>30</b>	<b>30</b>	<b>40</b>	<b>100</b>

# Walchand College of Engineering, Sangli

*(Government Aided Autonomous Institute)*

**AY 2023-2024**

## Course Information

<b>Programme</b>	B.Tech. (Electronics Engineering)
<b>Class, Semester</b>	Third Year B. Tech., Sem.-VI
<b>Course Code</b>	6HS303
<b>Course Name</b>	Humanities II- German Language
<b>Desired Requisites:</b>	10+2 level English

## Teaching Scheme

## Examination Scheme (Marks)

Lecture		LA1	LA2	ESE	Total
Tutorial		30	30	40	100
Practical	-				
Interaction	2 Hrs/week	<b>Credits: 2</b>			

## Course Objectives

- 1 To acquire German language skills both written and spoken
- 2 Enable students to communicate in German language in day to day situations

## Course Outcomes (CO) with Bloom's Taxonomy Level

<b>CO1</b>	Communicate clearly in German in different scenario	Apply
<b>CO2</b>	Handle oral and written communications in German language confidently	Understand

Module	Module Contents	Hours
I	<b>Module 1 : Greetings</b> <ol style="list-style-type: none"> <li>To introduce oneself and others</li> <li>Greeting people/colleagues at office/work-place etc.</li> <li>Exchanging information about country of origin</li> <li>Place of residence, professions</li> <li>Things that we eat and drink</li> </ol>	4
II	<b>Module 2 : Days, Numbers and languages</b> <ol style="list-style-type: none"> <li>Date and Days of Week</li> <li>Names of months</li> <li>Numbers 1 to 1000</li> <li>Names of Continents, Countries and their Capitals</li> <li>Languages and Nationalities, main cultural festivals</li> <li>Health and Parts of body</li> </ol>	5
III	<b>Module 3 : Sentence Structure and Vocabulary Building</b> <ol style="list-style-type: none"> <li>Alphabet,</li> <li>Personal Pronouns</li> <li>German Articles</li> <li>Genders</li> <li>Plural Forms</li> <li>Nouns</li> </ol>	2
IV	<b>Module 4 :Grammar</b> <ol style="list-style-type: none"> <li>Forming questions,</li> <li>Prepositions,</li> <li>Conjunctions,</li> <li>Verbs</li> <li>Dative and Accusative forms with examples,</li> <li>Opposites</li> </ol>	6

V	<b>Module 5 : Oral Communication</b> 1. Asking for and telling telephone numbers with dial code numbers 2. Making request 3. Word order in sentences/statements and full question 4. Speak on given topic 5. Asking questions ( Forming Question)	5
VI	<b>Module 6 : Written Communication : Basic Writing Skills</b> 1. Paragraph Writing 2. Comprehension 3. Short Essay Writing 4. Filling in Personal Information	4

#### Text Books

1	.Hartmut Auf der strasse, Heiko Bock, Mechthild Gerdes, Jutta Mueller, Helmut Mueller,“Themen Aktuell1- Deutsch als Fremdsprache-Kursbuch”,Max Hueber Verlag,Munich,Germany and Langers International Pvt.Ltd.,New Delhi ,ISBN: 3-19-0001690-9,Reprint 2014
2	.Hartmut Auf der strasse, Heiko Bock, Mechthild Gerdes, Jutta Mueller,Helmut Mueller,“Themen Aktuell1- Deutsch als Fremdsprache-Arbeitsbuch”,Max Hueber Verlag,Munich,Germany and Langers International Pvt.Ltd.,New Delhi ,ISBN: 3-19-011690-3,Reprint 201
3	Alan B, Jones A.“Themen Aktuell 1- Deutsch als Fremdsprache - Glossar”,Max Hueber Verlag, Munich,Germany and Langers International Pvt.Ltd.,New Delhi ,ISBN: 3-19-0001690-9,Reprint 2014

#### References

1	Archana Gogate, “German Workbook”, Shubhasha Publications,Pune, Reprint July 2016
2	Stefanie Dengler,Paul Rusch,Helen Schmitz,Tanja Sieber, “Netzwerk A1- Deutsch als FremdspracheKursbuch ”,Klett Langenscheidt, Munich,Germany and GOYAL Publishers Pvt. Ltd.,New Delhi, First Indian edition-2015
3	Stefanie Dengler,Paul Rusch,Helen Schmitz,Tanja Sieber, “Netzwerk A1- Deutsch alsFremdspracheArbeitsbuch ”,Klett Langenscheidt,Munich,Germany and GOYAL Publishers Pvt.Ltd.,New Delhi, First Indian edition-2015
4	Stefanie Dengler,Paul Rusch,Helen Schmitz,Tanja Sieber, Gavin Schalliol“Netzwerk A1- Deutsch alsFremdsprache- Glossar ”,Klett Langenscheidt, Munich, Germany and GOYAL Publishers Pvt.Ltd.,New Delhi, First Indian edition-2015

#### Useful Links

1	<a href="http://www.klett-sprachen.de/netzwerk">www.klett-sprachen.de/netzwerk</a>
2	<a href="http://www.cornelsen.de/studio-d">www.cornelsen.de/studio-d</a>
3	
4	

#### CO-PO Mapping

	Programme Outcomes (PO)												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1										1					
CO2										1					

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High

Each CO of the course must map to at least one PO.

### **Assessment**

The assessment is based on 2 in-semester evaluations (LA) of 30 marks each, end-sem examination (ESE) of 40 marks.

LA1 and LA2 are based on the modules taught (typically Module 1-3) and ESE is based on all modules with 30-40% weightage on modules before LA1 and 60-70% weightage on modules LA2.