

Hardware Assignment-2

1. Seven segment decoder

To display a 4-bit number on a 7-segment display. It has 7 cathode pins, 1 anode pin (connected to all 7 LEDs) and 1 pin for decimal point. On the Basys 3 board anode/cathode are active low pins. Hence, both the cathode and anode have to be driven to 0 to light the led.

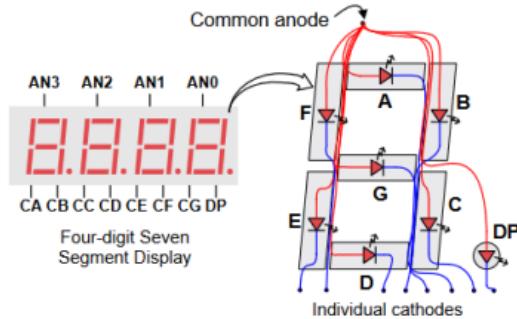
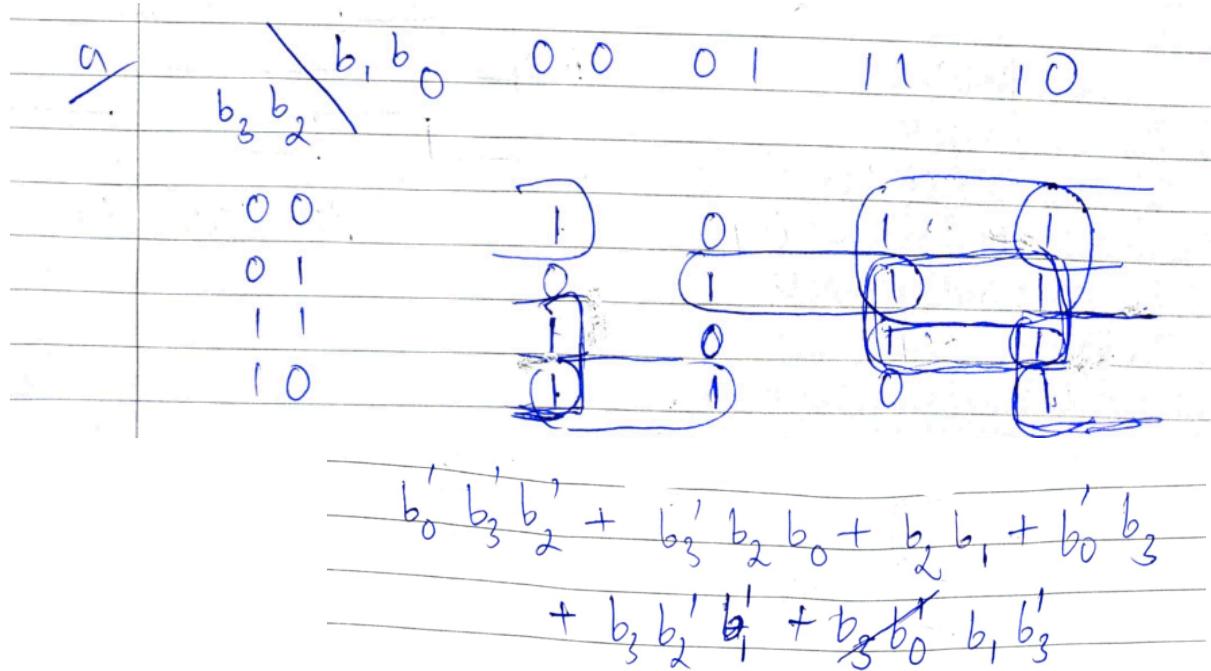


Figure 1: Pin details for 7 seven display on Basys 3 board

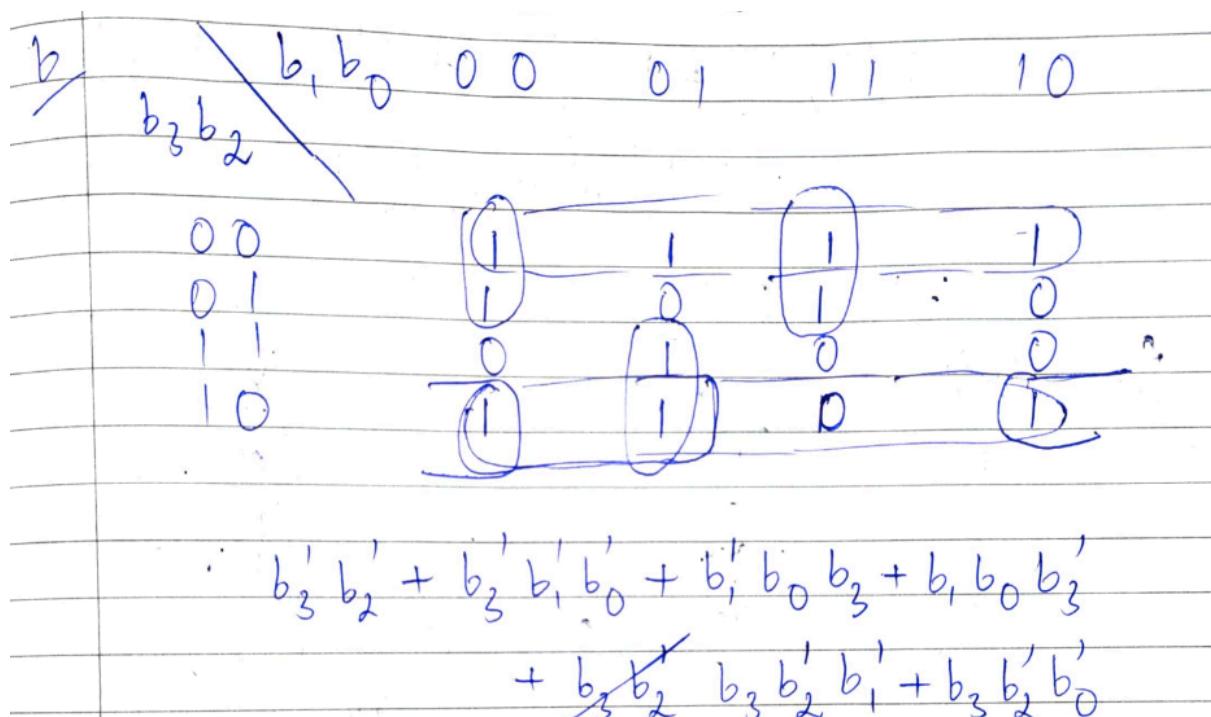
Value	$b_3b_2b_1b_0$	a	b	c	d	e	f	g
0	0000	1	1	1	1	1	1	0
1	0001	0	1	1	0	0	0	0
2	0010	1	1	0	1	1	0	1
3	0011	1	1	1	1	0	0	1
4	0100	0	1	1	0	0	1	1
5	0101	1	0	1	1	0	1	1
6	0110	1	0	1	1	1	1	1
7	0111	1	1	1	0	0	0	0
8	1000	1	1	1	1	1	1	1
9	1001	1	1	1	1	0	1	1
A	1010	1	1	1	0	1	1	1
B (b)	1011	0	0	1	1	1	1	1
C	1100	1	0	0	1	1	1	0
D (d)	1101	0	1	1	1	1	0	1
E	1110	1	0	0	1	1	1	1
F	1111	1	0	0	0	1	1	1

K-maps:

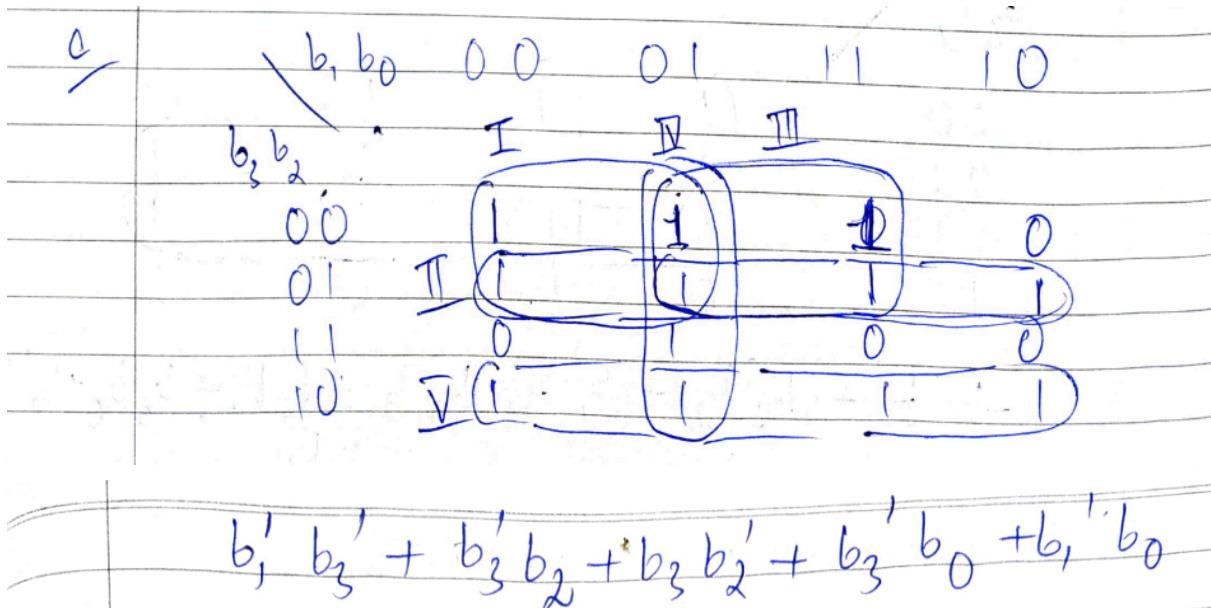
For a:



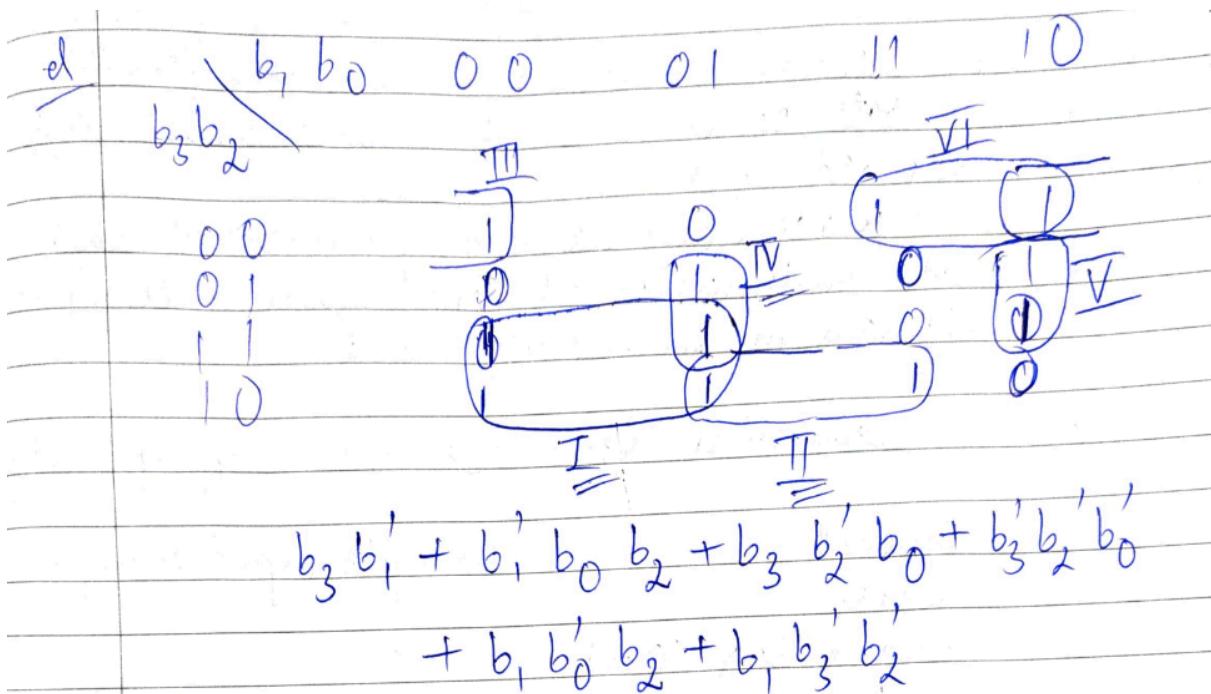
For b:



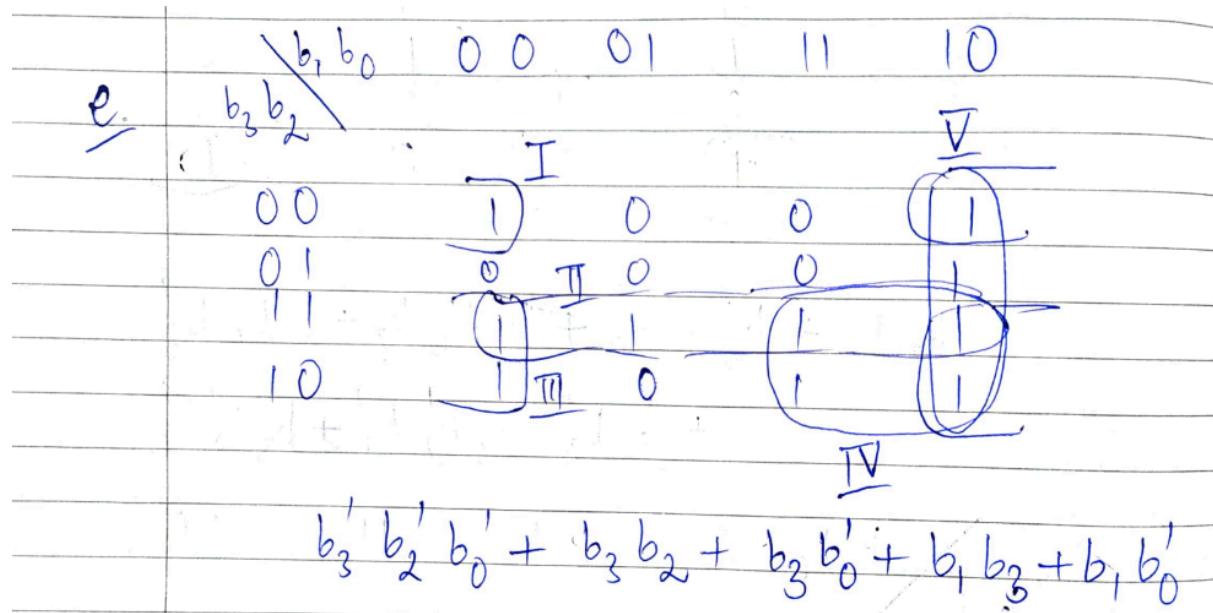
For c:



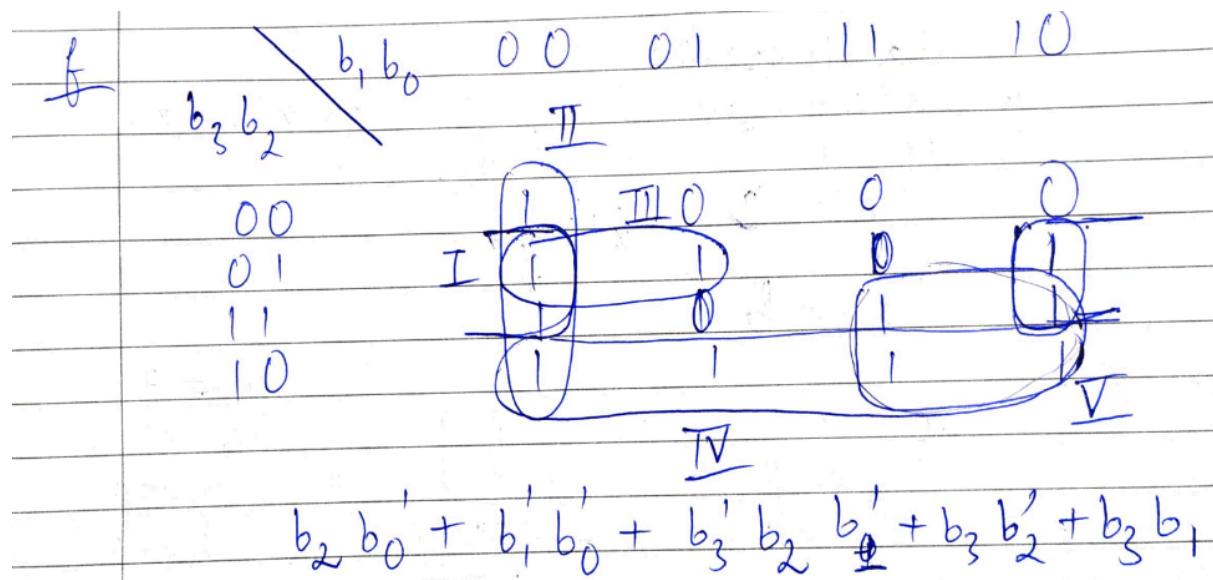
For d:



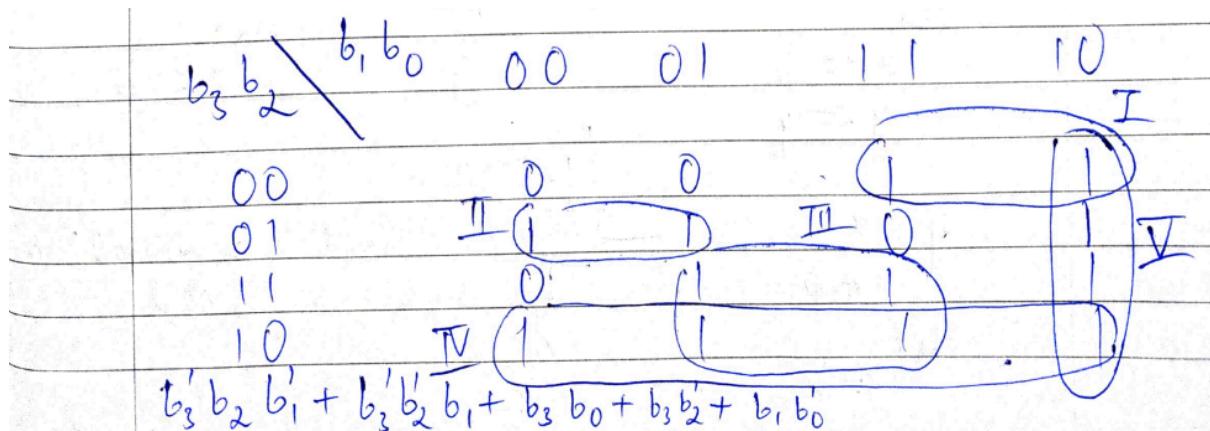
For e:



For f:

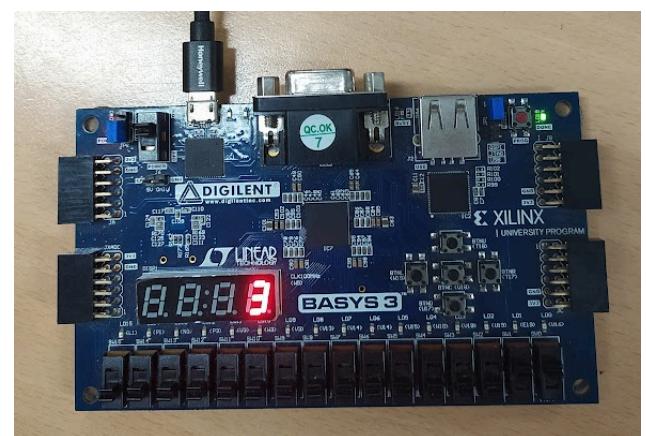
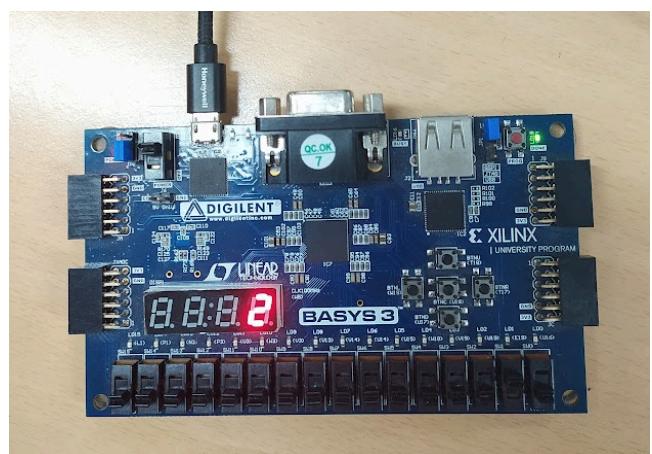
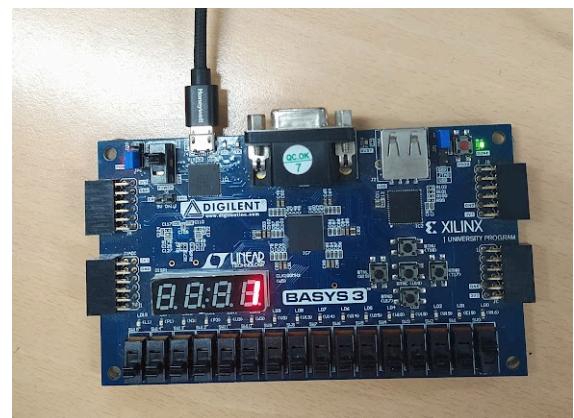
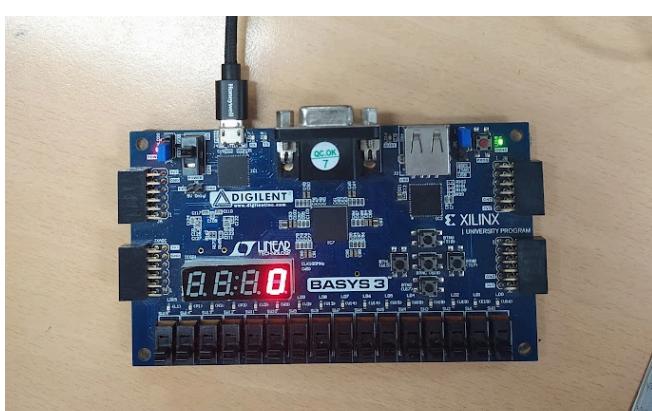


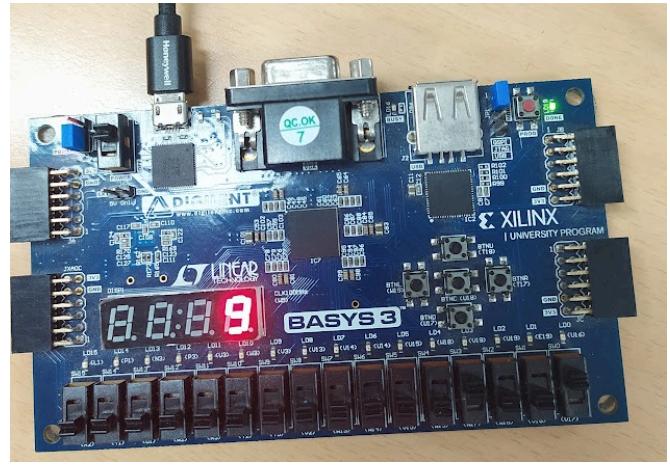
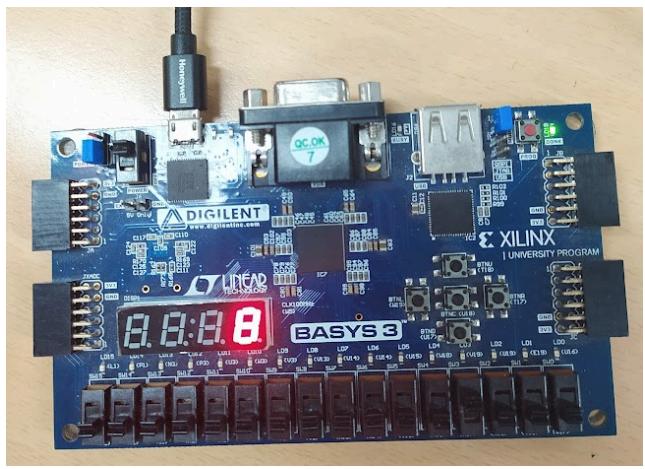
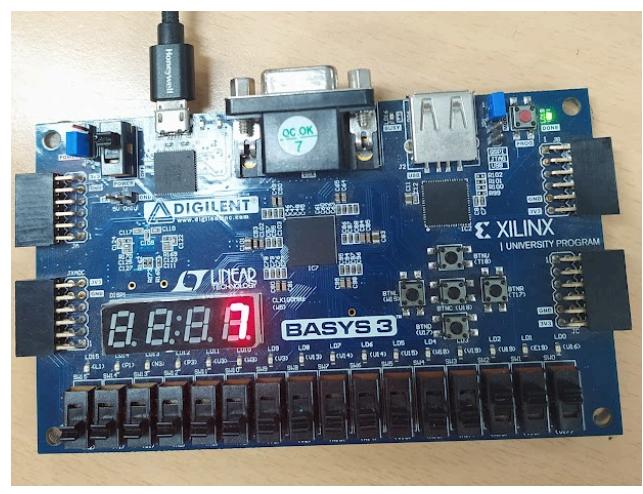
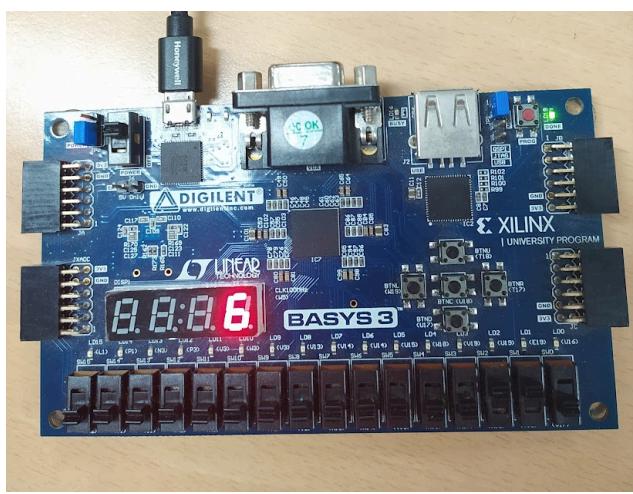
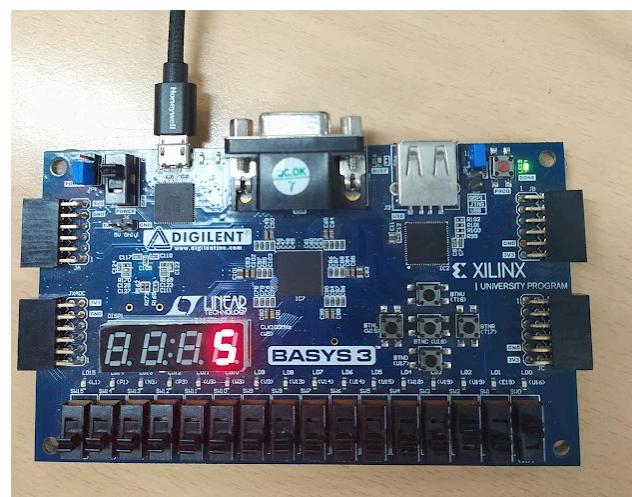
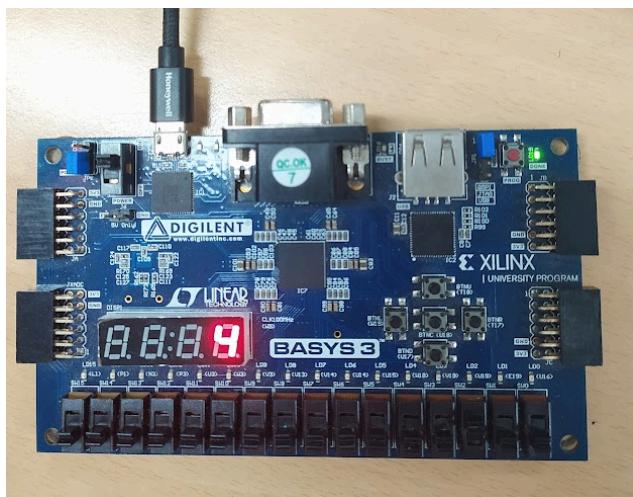
For g:

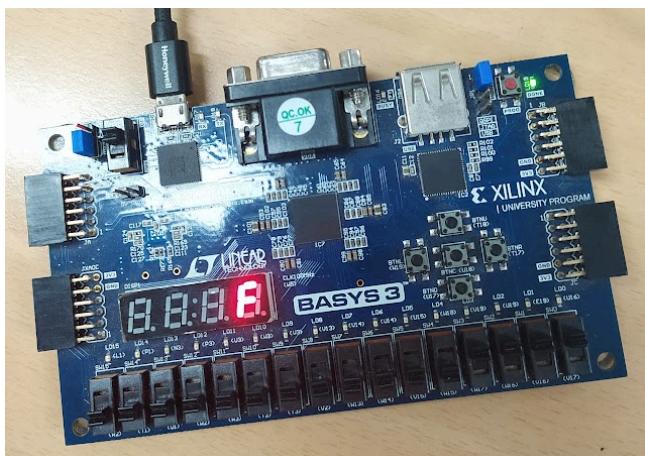
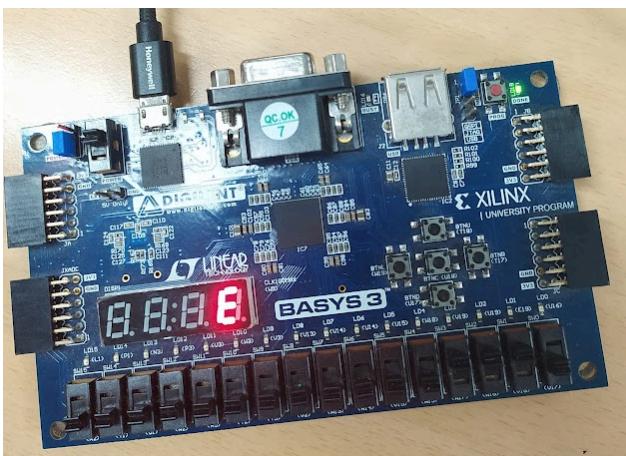
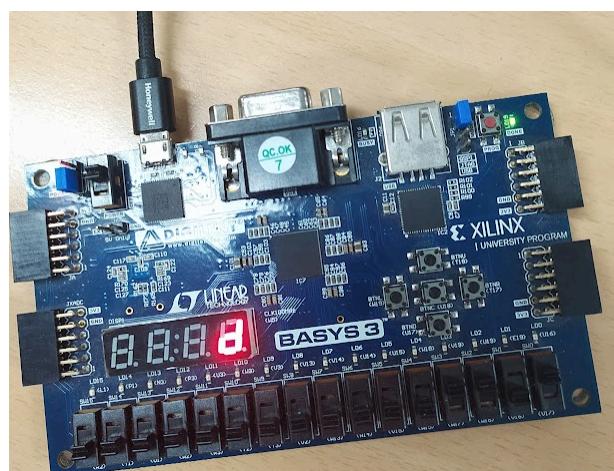
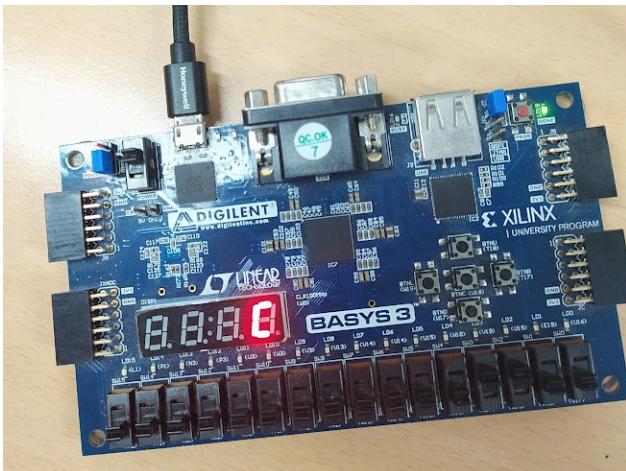
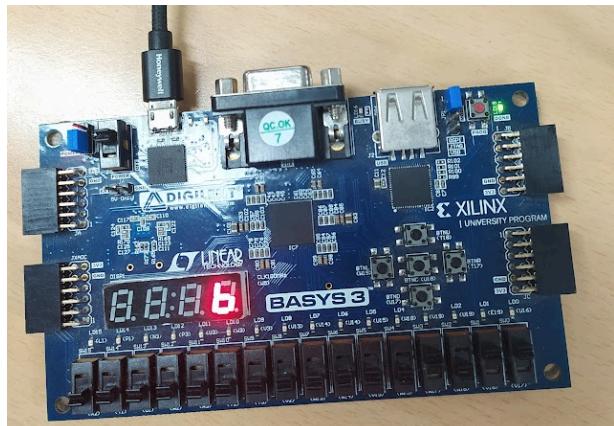
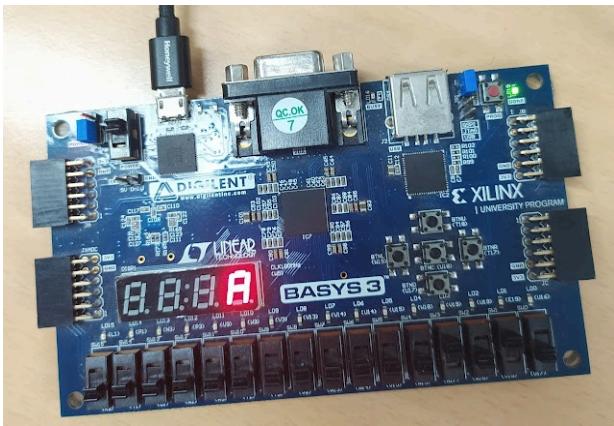


We added not condition to every statement since in the common anode configuration, cathode/anode are ACTIVE LOW pins (i.e., LOW = ACTIVE, HIGH = INACTIVE).

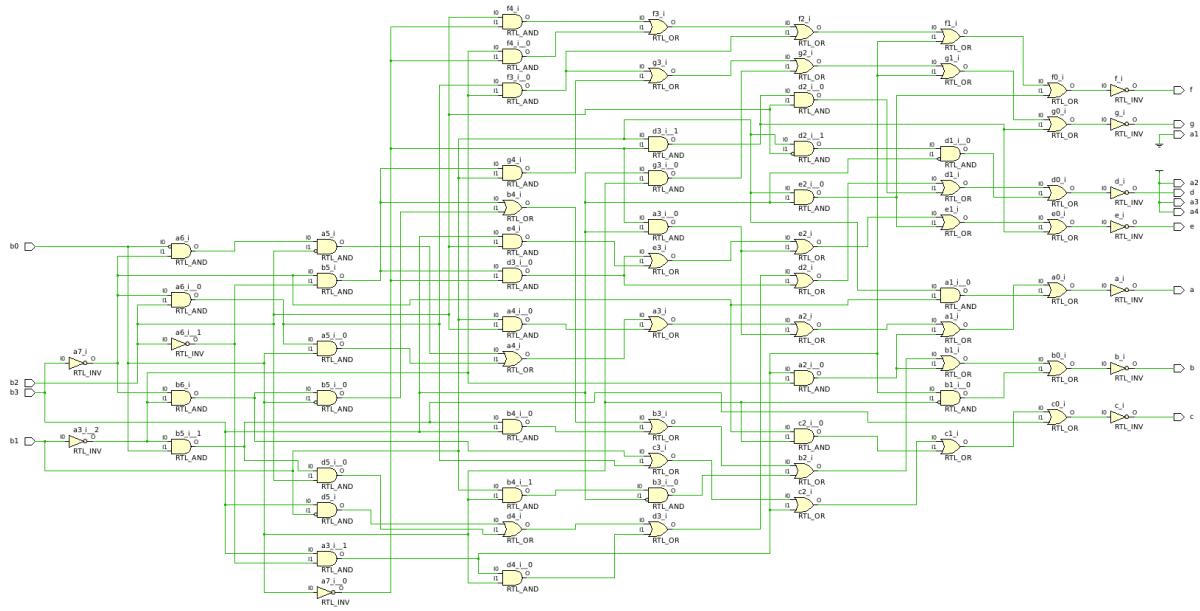
We connected pin V17 to b0, V16 to b1, W16 to b2 and W17 to b3; for 7-segment display, pin W7 to a, W6 to b, U8 to c, V8 to d, U5 to e, V5 to f and U7 to g; and for anodes pin U2 to a1, U4 to a2, V4 to a3 and W4 to a4.







Schematic:



Simulation (through testbench)

The timing diagram illustrates the digital logic levels of various signals over a period of 70,000 ps. The horizontal axis represents time, with major tick marks at 0 ps, 10,000 ps, 20,000 ps, 30,000 ps, 40,000 ps, 50,000 ps, 60,000 ps, and 70,000 ps. The vertical axis lists the signals: b0, b1, b2, b3, a1, a2, a3, a4, a, b, c, d, e, f, and g. Each signal is represented by a green bar indicating its state. The signals show the following states:

Name	Value
b0	1
b1	1
b2	0
b3	1
a1	0
a2	1
a3	1
a4	1
a	1
b	1
c	0
d	0
e	0
f	0
g	0

Resource Utilisation

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs	4	0	0	20800	0.02
LUT as Logic	4	0	0	20800	0.02
LUT as Memory	0	0	0	9600	0.00
Slice Registers	0	0	0	41600	0.00
Register as Flip Flop	0	0	0	41600	0.00
Register as Latch	0	0	0	41600	0.00
F7 Muxes	0	0	0	16300	0.00
F8 Muxes	0	0	0	8150	0.00

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	-	-	-
0	-	-	Set
0	-	-	Reset
0	-	Set	-
0	-	Reset	-
0	Yes	-	-
0	Yes	-	Set
0	Yes	-	Reset
0	Yes	Set	-
0	Yes	Reset	-

2. Slice Logic Distribution

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice	2	0	0	8150	0.02
SLICEL	2	0	0	20800	0.02
SLICEM	0	0	0	9600	0.00
LUT as Logic	4	0	0	20800	0.02
using 05 output only	0	0	0	20800	0.02
using 06 output only	1	0	0	20800	0.02
using 05 and 06	3	0	0	20800	0.02
LUT as Memory	0	0	0	9600	0.00
LUT as Distributed RAM	0	0	0	9600	0.00
LUT as Shift Register	0	0	0	9600	0.00
Slice Registers	0	0	0	41600	0.00
Register driven from within the Slice	0	0	0	41600	0.00
Register driven from outside the Slice	0	0	0	41600	0.00
Unique Control Sets	0	0	0	8150	0.00

3. Memory

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	50	0.00
RAMB36/FIFO*	0	0	0	50	0.00
RAMB18	0	0	0	100	0.00

4. DSP

Site Type	Used	Fixed	Prohibited	Available	Util%
DSPs	0	0	0	90	0.00

8. Primitives

Ref Name	Used	Functional Category
OBUF	11	IO
LUT4	7	LUT
IBUF	4	IO

2) Driving all 4 LED Displays

We defined std_logic_vectors s0, s1, s2 and s3 of length 4 for the 4 '4-bit' signals given as input and anode (an vector).

We fixed the value of N at 1000 i.e. the multiplexer value changes and the next anode is selected when 1000 cycles of the clock signal have been completed (or $200 \times 1000 \text{ ns} = 0.2 \text{ ms}$ time has elapsed). This process repeats as counter is reset to 0 when $4 \times N = 4000$ cycles have been completed.

For counter:

```

if rising_edge(clk) then
    if counter<4*N then
        counter<=counter+1;
    else
        counter<=0;
        cycle<=cycle+1;
    end if;

if counter <=N then
    mux_selectb<="00";
elsif (counter <=2*N) and counter >N then
    mux_selectb<="01";
elsif (counter <=3*N) and counter >2*N then
    mux_selectb<="10";
else
    mux_selectb<="11";
end if;

if mux_selectb<="00" then
    an<="0111"; --an[1] activated
    s<=s0;
elsif mux_selectb<="01" then
    an<="1011"; --an[2] activated
    s<=s1;

elsif mux_selectb<="10" then
    an<="1101";--an[3] activated
    s<=s2;

else
    an<="1110";--an[4] activated
    s<=s3;
end if;
```

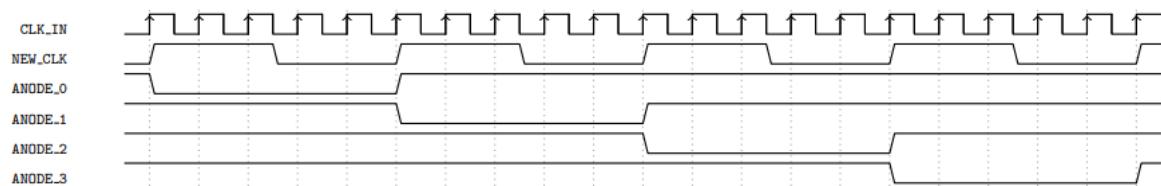
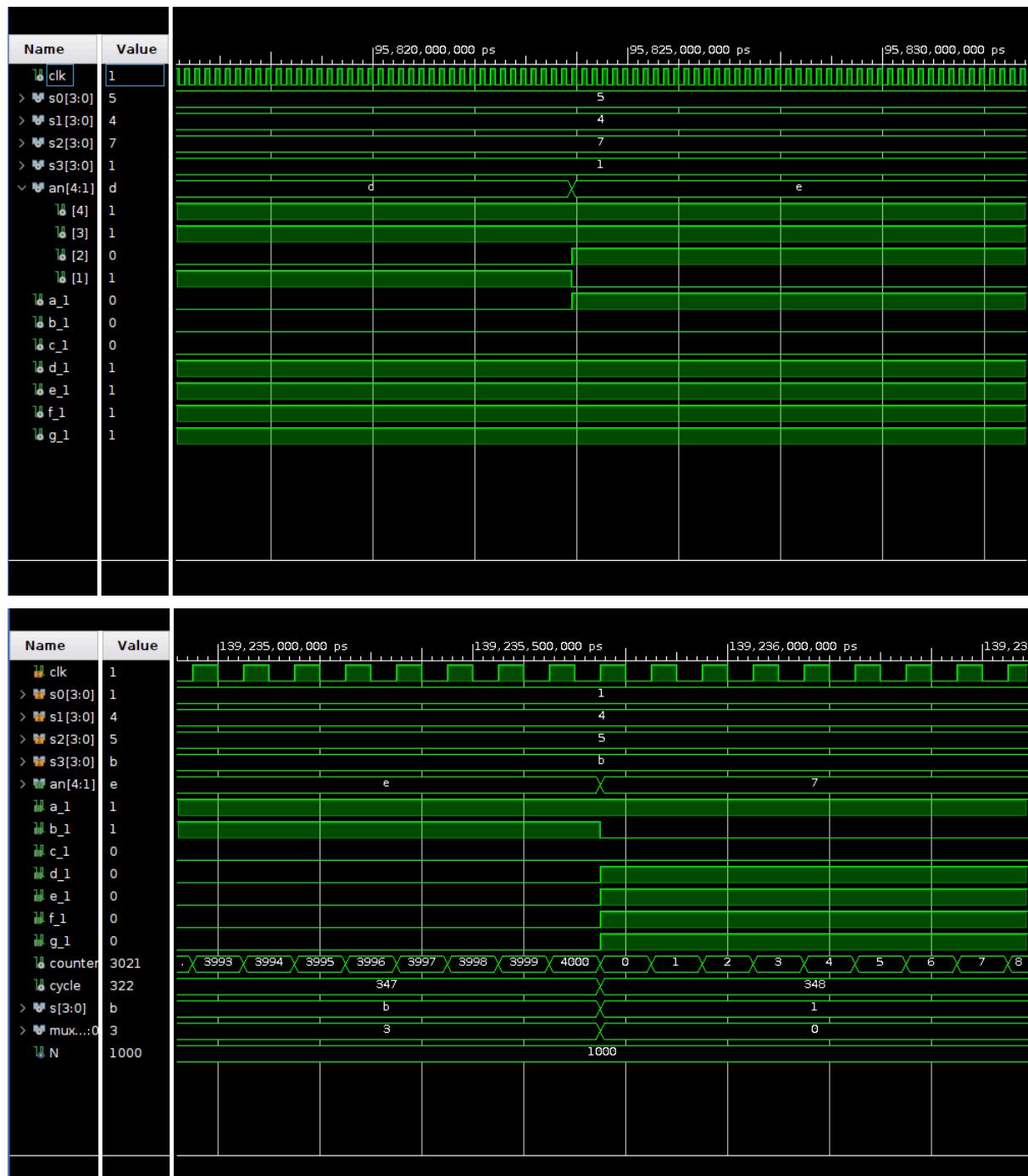
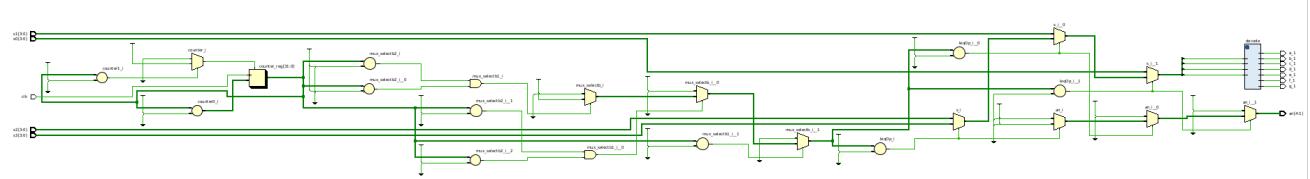


Figure 6: Illustration of refresh clock signal

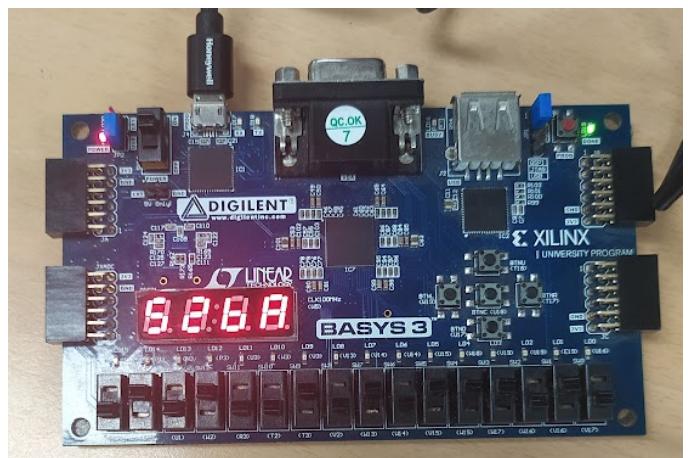
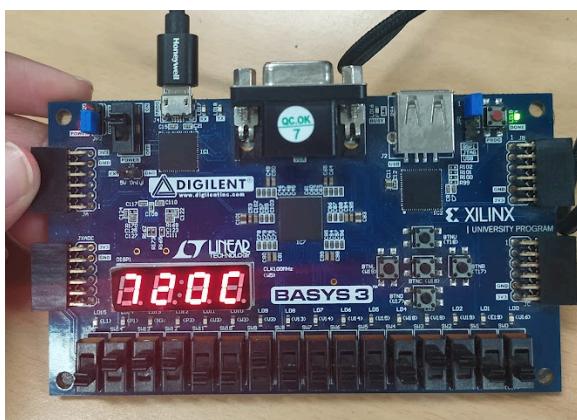
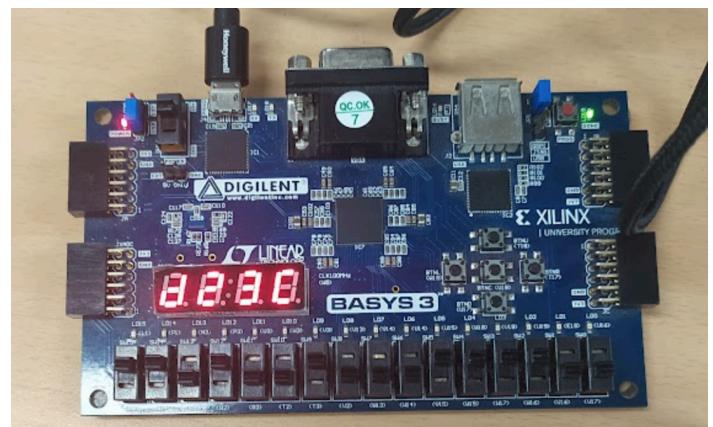
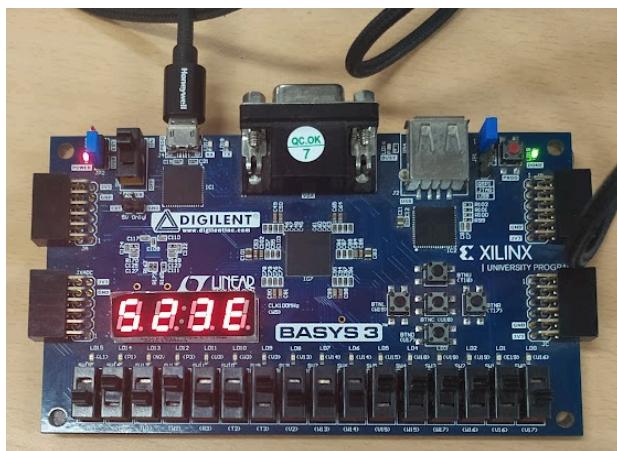
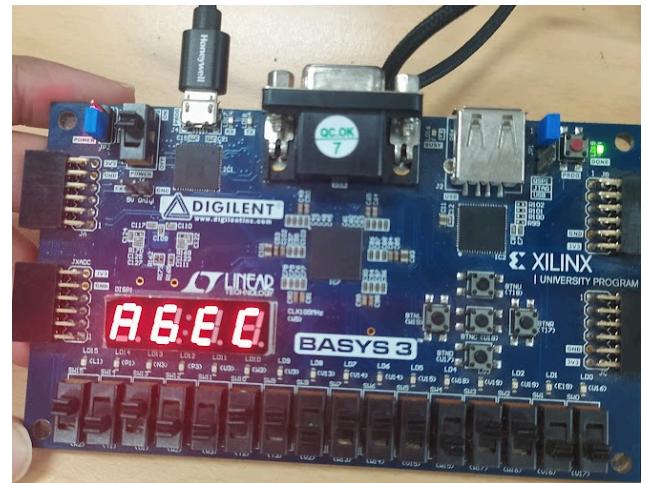
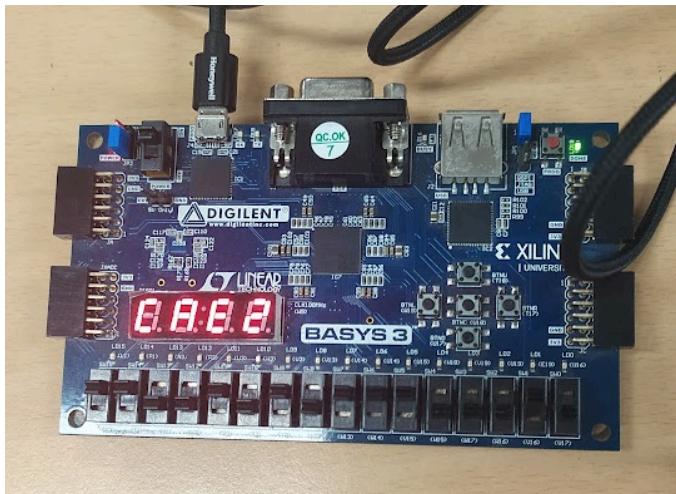
Simulation (through testbench)

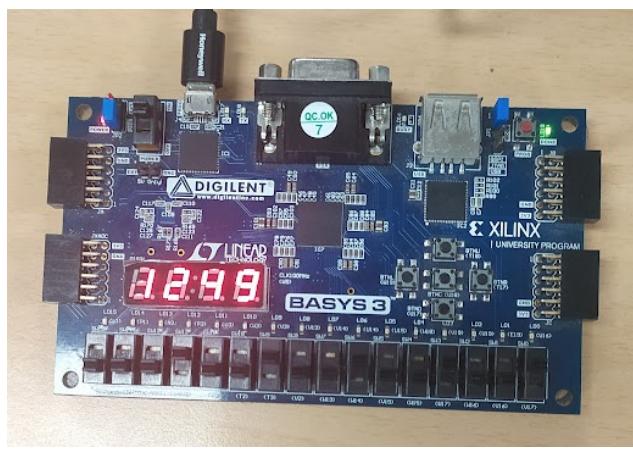


Schematic



We selected pins V17, V16, W16, W17 for s3 vector, pins W15, V15, W14, W13 for s2 vector, pins V2, T3, T2, R3 for s1 vector and pins W2, U1, T1, R2 for s0 vector; for 7-segment display, pin W7 to a_1, W6 to b_1, U8 to c_1, V8 to d_1, U5 to e_1, V5 to f_1 and U7 to g_1; and for anodes pin U2 to an[1], U4 to an[2], V4 to an[3] and W4 to an[4].





Resource Utilisation

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs	104	0	0	20800	0.50
LUT as Logic	104	0	0	20800	0.50
LUT as Memory	0	0	0	9600	0.00
Slice Registers	32	0	0	41600	0.08
Register as Flip Flop	32	0	0	41600	0.08
Register as Latch	0	0	0	41600	0.00
F7 Muxes	0	0	0	16300	0.00
F8 Muxes	0	0	0	8150	0.00

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	-	-	-
0	-	-	Set
0	-	-	Reset
0	-	Set	-
0	-	Reset	-
0	Yes	-	-
0	Yes	-	Set
0	Yes	-	Reset
0	Yes	Set	-
32	Yes	Reset	-

2. Slice Logic Distribution

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice	36	0	0	8150	0.44
SLICEL	28	0			
SLICEM	8	0			
LUT as Logic	104	0	0	20800	0.50
using O5 output only	0				
using O6 output only	55				
using O5 and O6	49				
LUT as Memory	0	0	0	9600	0.00
LUT as Distributed RAM	0	0			
LUT as Shift Register	0	0			
Slice Registers	32	0	0	41600	0.08
Register driven from within the Slice	32				
Register driven from outside the Slice	0				
Unique Control Sets	1		0	8150	0.01

3. Memory

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	50	0.00
RAMB36/FIFO*	0	0	0	50	0.00
RAMB18	0	0	0	100	0.00

4. DSP

Site Type	Used	Fixed	Prohibited	Available	Util%
DSPs	0	0	0	90	0.00

8. Primitives

Ref Name	Used	Functional Category
LUT2	128	LUT
FDRE	32	Flop & Latch
CARRY4	32	Carry Logic
IBUF	17	IO
OBUF	11	IO
LUT1	9	LUT
LUT4	7	LUT
LUT6	4	LUT
LUT5	3	LUT
LUT3	2	LUT
BUFG	1	Clock