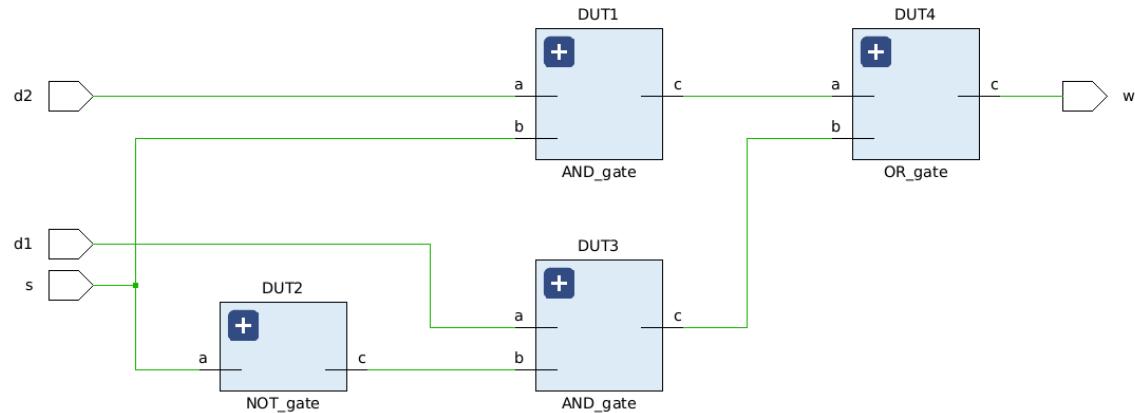


Assignment-1 Part (b)

1. 2x1 Multiplexer

This is an implementation of the 2x1 Multiplexer (Mux) i.e. $d1 \cdot s' + d2 \cdot s$

Schematic:

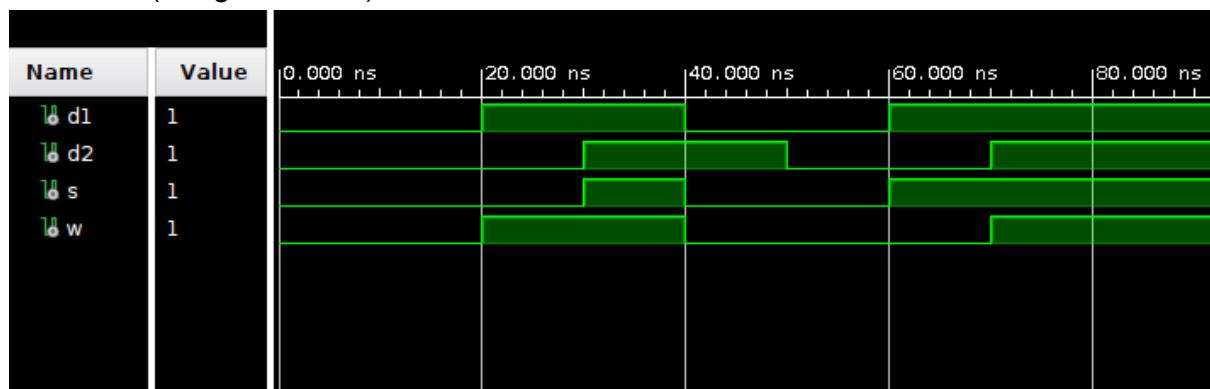


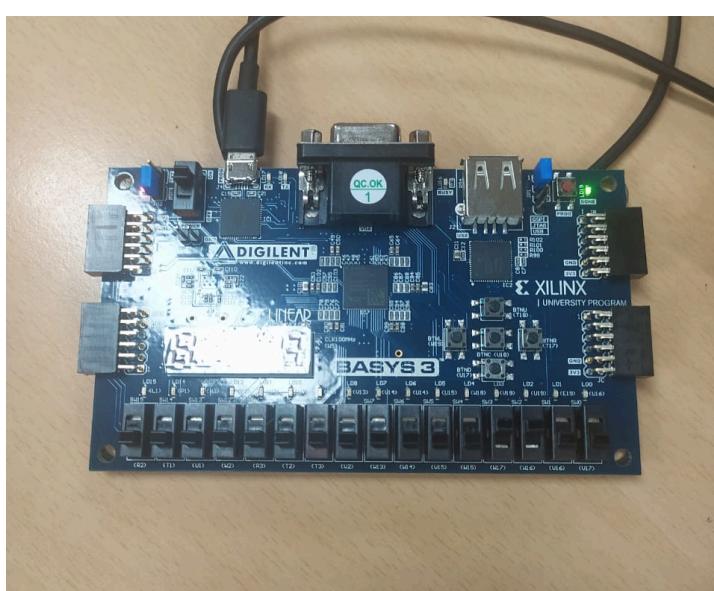
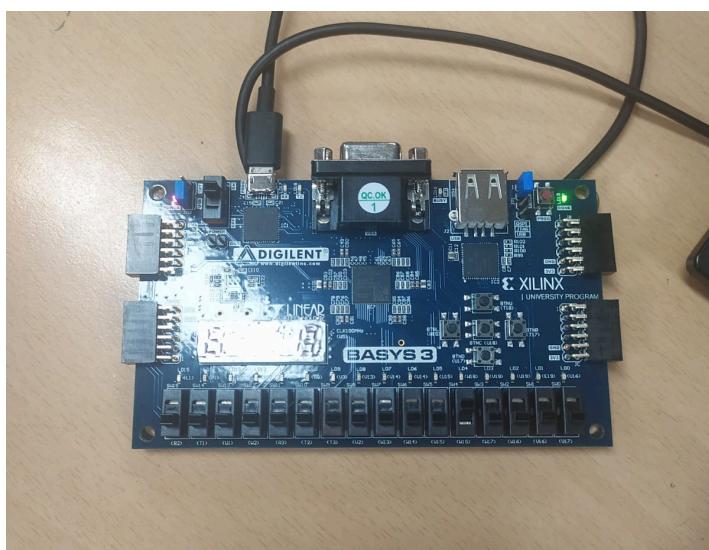
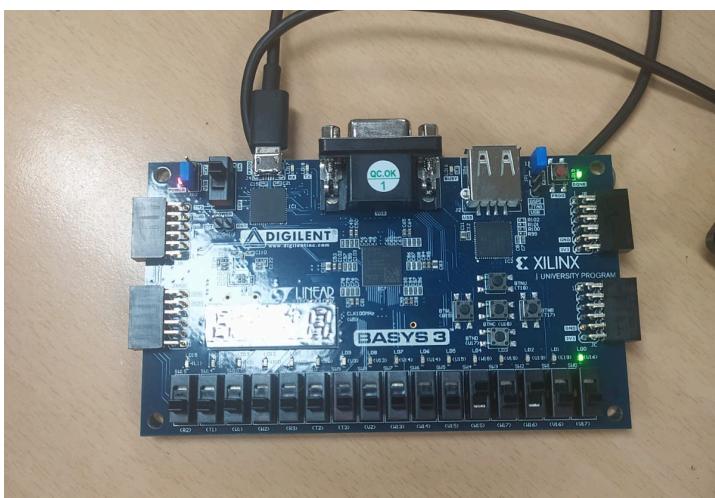
We connected switch W17 to input d1, switch W15 to input d2, switch W16 to input s, and LED U16 to output w.

The simulation and implementation on the FPGA board correlate with the truth table.

d1	d2	s	Output w
0	0/1	0	0
1	0/1	0	1
0/1	0	1	0
0/1	1	1	1

Simulation (using testbench)



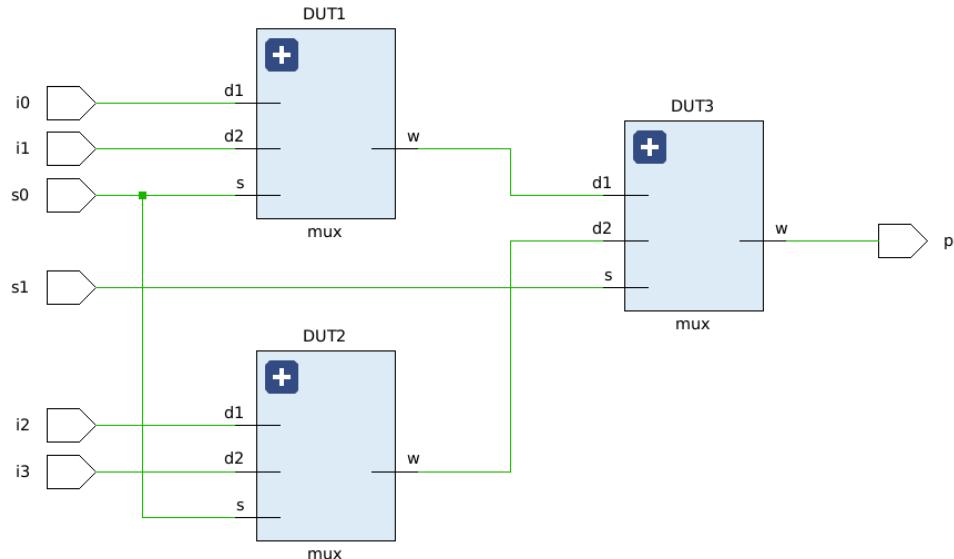


2. 4x1 Multiplexer

This is an implementation of the 4x1 Multiplexer (Mux) using three 2x1 Multiplexers.

Output: $s0'.s1'.i0 + s0.s1'.i1 + s0'.s1.i2 + s0.s1.i3$

Schematic:



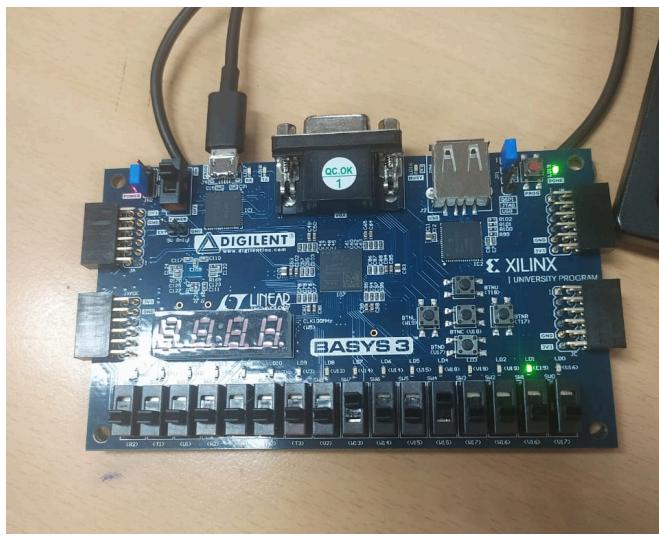
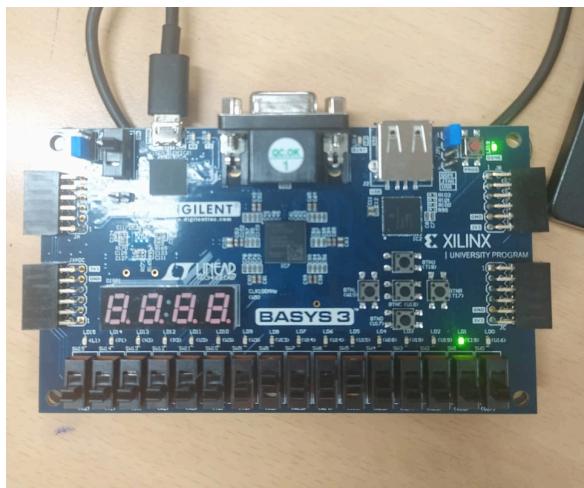
Truth table:

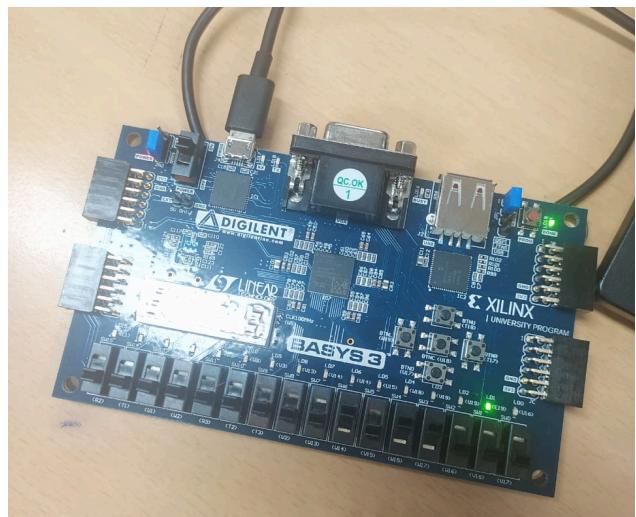
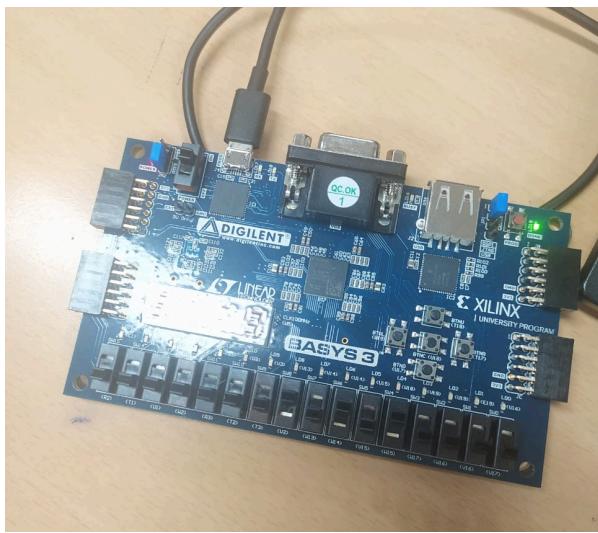
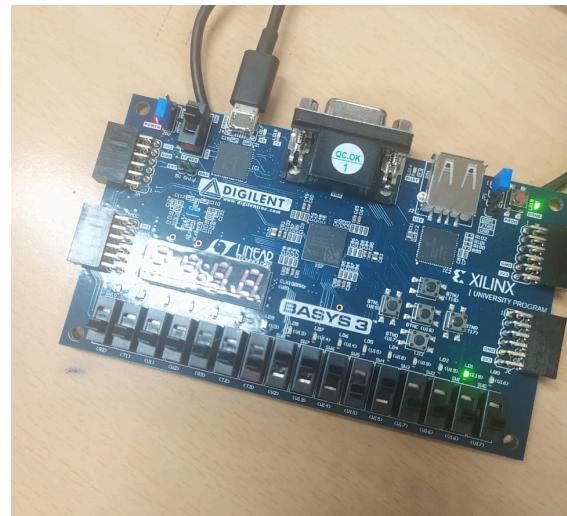
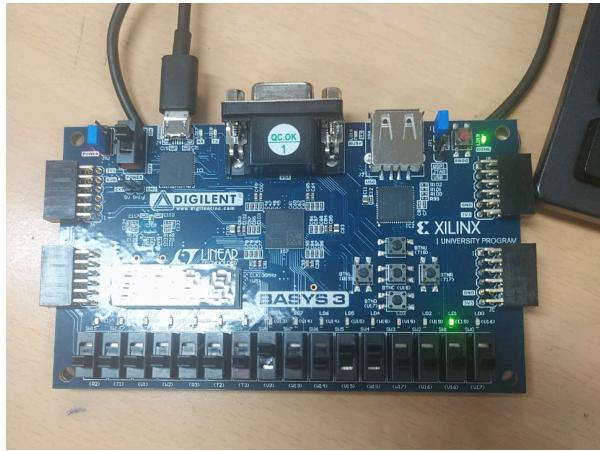
i0	i1	i2	i3	s1	s0	Output p
0	0/1	0/1	0/1	0	0	0
1	0/1	0/1	0/1	0	0	1
0/1	0	0/1	0/1	0	1	0
0/1	1	0/1	0/1	0	1	1
0/1	0/1	0	0/1	1	0	0
0/1	0/1	1	0/1	1	0	1
0/1	0/1	0/1	0	1	1	0
0/1	0/1	0/1	1	1	1	1

We connected switch W17 to input i0, switch W15 to input i1, switch V15 to input i2, switch W14 to i3, switch W13 to s0, switch V2 to s1, and LED E19 to output p.

The simulation and implementation on the FPGA board correlate with the truth table.

Simulation (using testbench):





Resource utilisation:

Site Type	Used	Fixed	Prohibited	Available	Util%
LUT as Logic	1	0	0	20800	<0.01
LUT as Memory	0	0	0	9600	0.00
Slice Registers	0	0	0	41600	0.00
Register as Flip Flop	0	0	0	41600	0.00
Register as Latch	0	0	0	41600	0.00
Block RAM Tile	0	0	0	50	0.00
DSPs	0	0	0	90	0.00