ECE 593 Fundamentals of Pre-Silicon Validation
Project Code Drop 1 Report

Team Members:
Deeksha Kamath
Ritvik Tiwari
Tanvi Patil

1. **Stimulus/Constraints-** We have added the following constraints in our testbench code.
    1. Opcode – To ensure that the randomized opcode generated after randomization of the instruction word is valid.
    2. Immediate field – To ensure that after the instruction word is randomized, the immediate field bits hence obtained don't amount to value should not cause segmentation fault.

2. **Coverage-** We have added the following covergroups and respective coverpoints in our testbench.
    a. Hazard – To check if there are any hazards with a coverpoint called hazard detection.
    b. Forward Unit – To check if forwarding has been enabled or not with coverpoint forward_EN.
    c. Mux – To observe the multiplexer output with respect to Immediate Field and Memory Read Enable with coverpoints Is_Imm and MEM_R_EN.
    d. ALU – To check for all the operations as per varying opcodes with the help of coverpoint called EXE_CMD and respective bins, to check the values of the val1, val2 signals.

3. **Testbench structure-** We have created the following components as of now:
    1. Package – It contains a typedef enum for opcodes that are valid.
    2. Transaction – Declared inputs for randomization and added constraints.
    3. Coverage – Added covergroups and coverpoints on internal signals of design.
    4. Generator – To provide constrained randomized set of instruction to the mailbox.