

## 设计图



OP	RegWrite	MemWrite	RegDst	AluSrc1	AluSrc2	AluOp	ExtOp	RegSrc	BrUnit
ADD	1	x	1	0	0	ADD	x	01	x
SUB	1	x	1	0	0	SUB	x	01	x
AND	1	x	1	0	0	AND	x	01	x
OR	1	x	1	0	0	OR	x	01	x
SLT	1	x	1	0	0	<	x	01	x
ADDU	1	x	1	0	0	ADDU	x	01	x
XOR	1	x	1	0	0	XOR	x	01	x
SRL	1	x	0	1	0	>>	imm(10:6)	01	x
SLL	1	x	0	1	0	<<	imm(10:6)	01	x
SW	x	1	0	1	0	ADD	符号扩展	x	x

OP	RegWrite	MemWrite	RegDst	AluSrc1	AluSrc2	AluOp	ExtOp	RegSrc	BrUnit
LW	1	x	0	0	1	ADD	符号扩展	10	x
BEQ	x	x	x	x	x	ADD	x	x	BEQ
ADDI	1	x	1	0	1	ADD	符号扩展	01	x
ADDIU	1	x	1	0	1	ADDU	无符号扩展	01	x
ORI	1	x	1	0	1	OR	符号扩展	01	x
LUI	1	x	0	x	x	x	imm左移16位到高位，其余0	11	x
J	x	x	x	x	x	x	x	x	J
JAL	1	x	\$31	x	x	x	x	x	JAL