设计图

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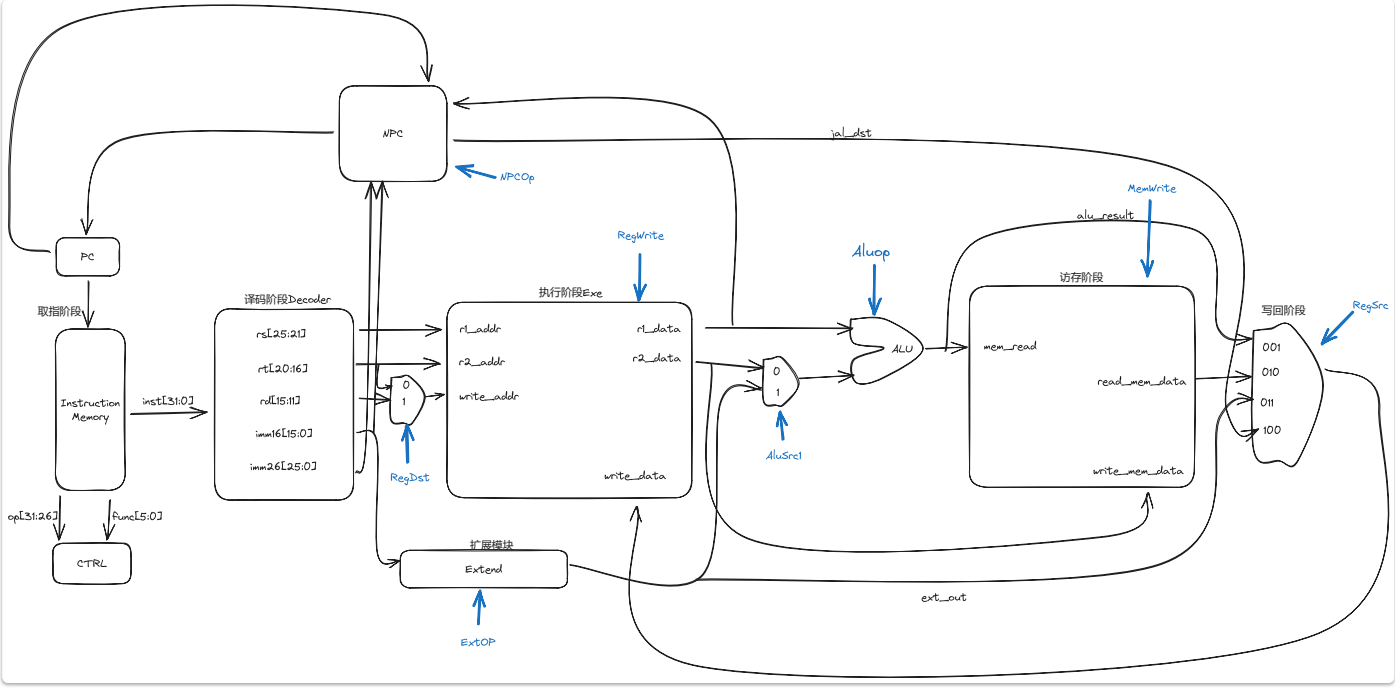
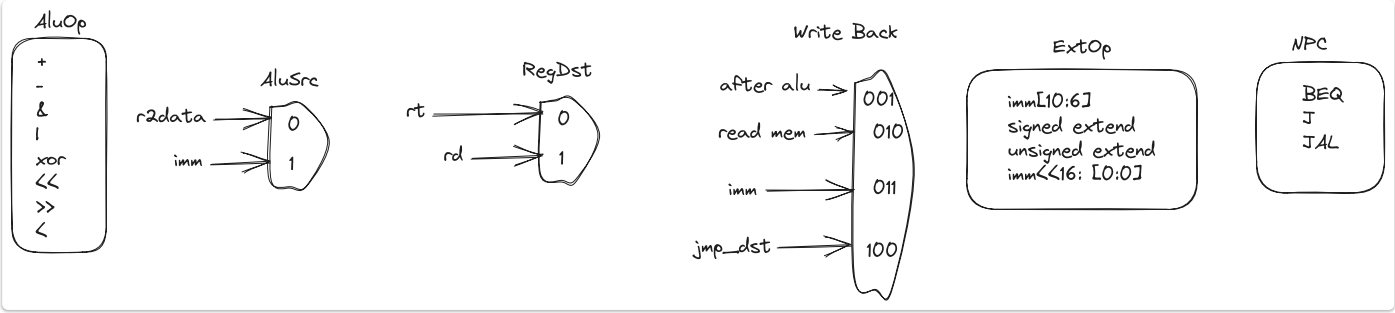


各个控制模块



控制模块信息

OP	RegWrite	MemWrite	RegDst	AluSrc1	AluSrc2	AluOp	ExtOp	RegSrc	BrUnit
ADD	1	x	1	0	0	ADD	x	001	x
SUB	1	x	1	0	0	SUB	x	001	x
AND	1	x	1	0	0	AND	x	001	x
OR	1	x	1	0	0	OR	x	001	x
SLT	1	x	1	0	0	SLT	x	001	x
ADDU	1	x	1	0	0	ADD	x	001	x
SUBU	1	X	1	0	0	SUB	x	001	x
XOR	1	x	1	0	0	XOR	x	001	x
SRL	1	x	1	1	0	>>	x	001	x
SLL	1	x	1	1	0	<<	x	001	x
SW	x	1	x	0	1	ADD	无符号扩展	x	x

OP	RegWrite	MemWrite	RegDst	AluSrc1	AluSrc2	AluOp	ExtOp	RegSrc	BrUnit
LW	1	x	0	0	1	ADD	无符号扩展	010	x
BEQ	x	x	x	x	x	SUB	x	x	BEQ
ADDI	1	x	0	0	1	ADD	符号扩展	001	x
ADDIU	1	x	0	0	1	ADD	符号扩展	001	x
ORI	1	x	0	0	1	OR	无符号扩展	001	x
LUI	1	x	0	x	x	x	imm左移16位到高位，其余0	011	x
J	x	x	x	x	x	x	x	x	J
JAL	1	x	$31	x	x	x	x	100	JAL