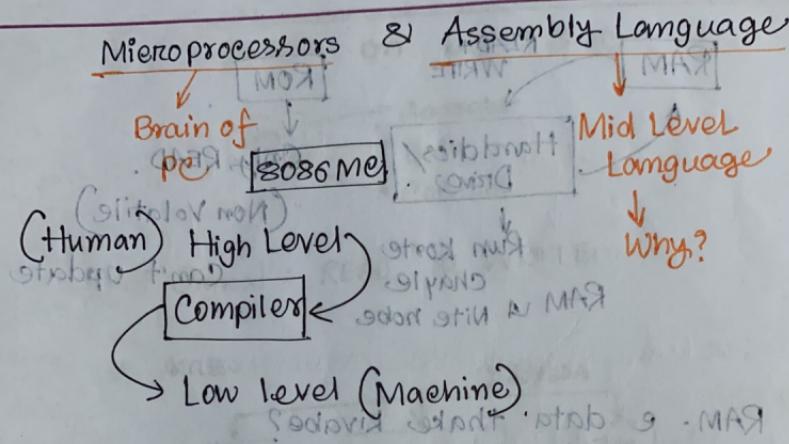
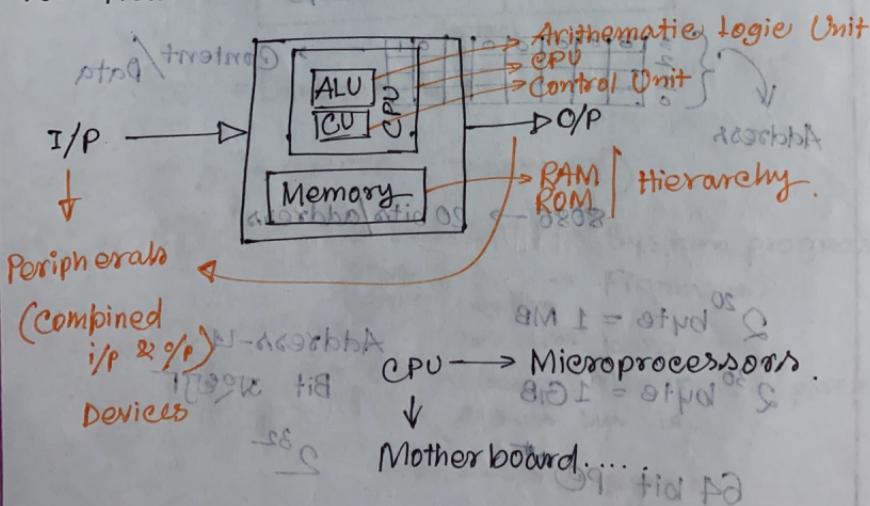


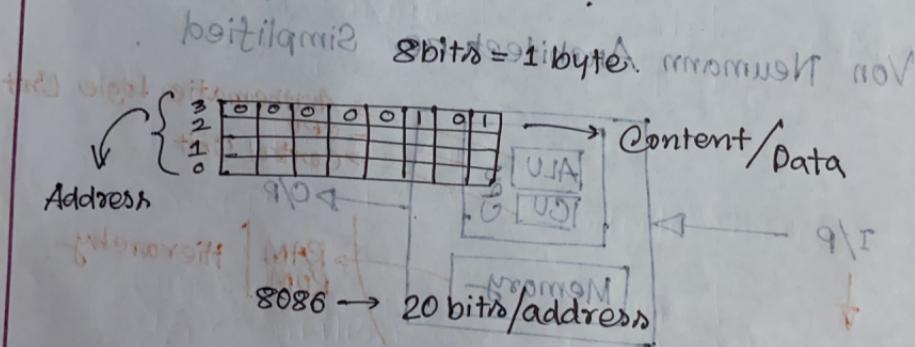
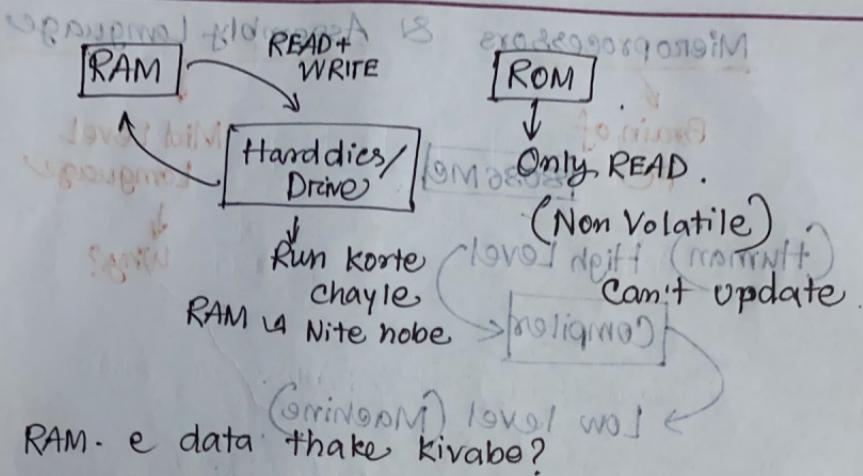
27-02-23

Week-1/3



Von Neumann Architecture Simplified





$$2^{20} \text{ byte} = 1 \text{ MB}$$

$$2^{30} \text{ byte} = 1 \text{ GB}$$

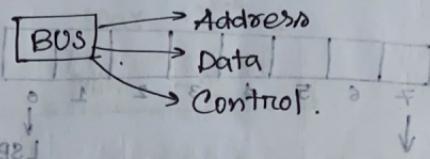
64 bit PC

Address - 14

Bit 32

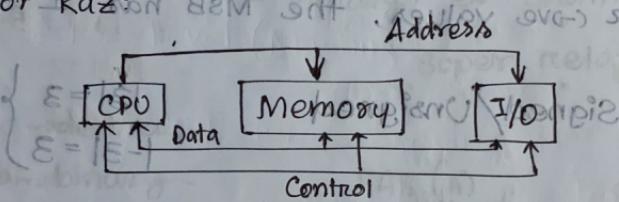
Address 2³²

Word size depends on byte size
8 bits = 1 byte



Control Signal : READ & WRITE

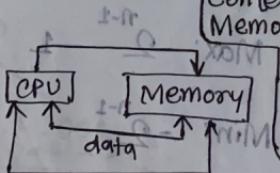
egular Kazan 8M SMT



CPU → Unidirectional

RAM - READ & WRITE. (Temporary)

ROM - READ ONLY (Permanent) → System program.



Content of Memory Location → Firmware.

READ korar jonne.

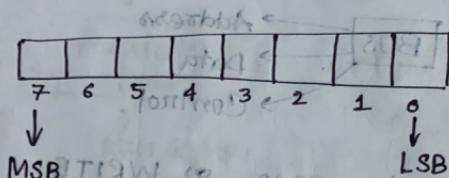
Address of Memory to be placed kore
Address bus la.

Control → READ Operation.

01 - 03 - 23

Week - 1/5

Memory size depends on number of bits



For positive values, the MSB has 0 value

Signed / Unsigned $|+3| = 3$ $| -3 | = 3 \} \text{ Magnitude}$

1s Complement (Flip)
2s complement (+1)

Unsigned Representation

Signed Representation

$2^n - 1$

Max: $2^{n-1} - 1$

Min: -2^{n-1}

All
Chapter-2
things

Unsigned

$$\text{Max } 2^n - 1$$

$$\text{Min } 0$$

Signed

$$\text{Max } 2^{n-1} - 1$$

$$\text{Min } -2^{n-1}$$

Ques. Keno Hexa Use kori?

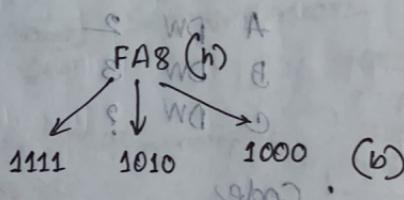
= Binary. er shathe
Super related.

$$1010d \rightarrow \text{decimal}$$

$$1010b \rightarrow \text{binary}$$

$$1010h \rightarrow \text{hexa}$$

without floating



FCB0

MAIN PROG

MSB > 8

at hole XA VOM

negative

8^FXA VOM

8.XA VOM

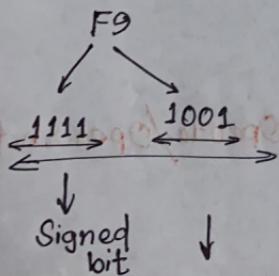
XA.8 VOM

0.8 VOM

+ 12 THI

FF FF

hexa



Signed bit

$$\begin{array}{r} 1111 \\ 1001 \\ \hline \end{array}$$

$$\downarrow$$

$$00000111 \rightarrow 7$$

$$(-7)$$

END MAIN

1000 0000
8 0

} hexa

Code in Assembly Language

Chap-4

Hello World
Subtraction

Addition

Keywords from Text

• model small

• stack 100h

A DW 2

B DW 3

C DW ?

• Code

MAIN PROC

MOV AX, varData

MOV DS, A

MOV AX, A

ADD AX, B

MOV C, AX

MOV AX, 4C00H

INT 21H

MAIN END

END MAIN

→ Stack Segment
→ Data
→ Code

→ Variable use
→ Instruction

→ Initialization

Operands
(ki kya koi operation)

OpCode / Operand.

0000 0001
0 8

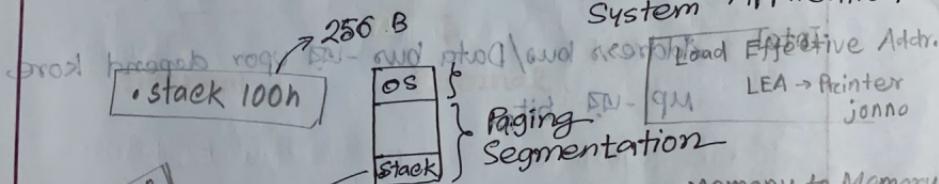
1001 1111
↓

0000 0000
F ← 11100000

• .asm extension ka file save korte hobe.

• model small → use kora hoi.

Load korte → [RAM] Software tid +



Memory to Memory
(Illegal)
MOV A, B
MOV C, D

HW
5+5 = 10
to show
2. User input A, B,
Sum C.
Subtraction D.
itive hole Stack
Segment [Local Variable]
256 B.

3. How to show 5+5 = 10
to show
2. User input A, B,
Sum C.
Subtraction D.
itive hole Stack
Segment [Local Variable]
256 B.

• data 16 bit
A dw 2
B dw 3
C dw ?

• code
main proc
MOV AX, a Data
MOV DS, AX

Base Address
dhore Rakha

• cde
main proc
MOV AX, a Data
MOV DS, AX
MOV AX, A
ADD AX, B

• Intel 8080
MOV C, AX
MOV DX, C
MOV AH, 2
INT 21H

Output
newajay na?

06-03-23

Week-2/3

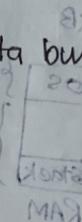
Microprocessors

Evaluation of Microprocessor: (Intel).

4 bit - microprocessors.

Address bus / Data bus - ~~MP~~ upon depend kore,

MP - 4 bit



INTEL 4004:

Clock speed 740 KHz.

4 bit MP

Dif. betw:

8085 vs. 8086

8086 vs. 8088

8 bit - microprocessor:

INTEL 8008.

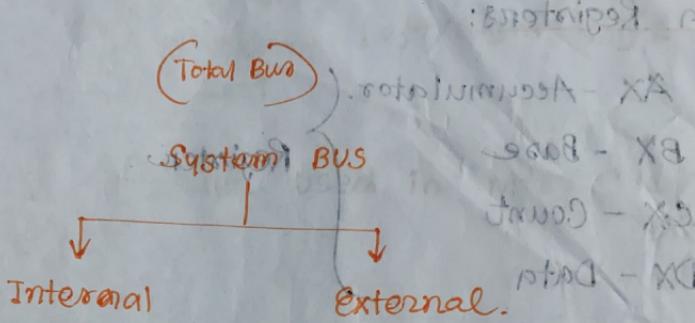
INTEL 8080

INTEL 8085*

16 bit - MP:

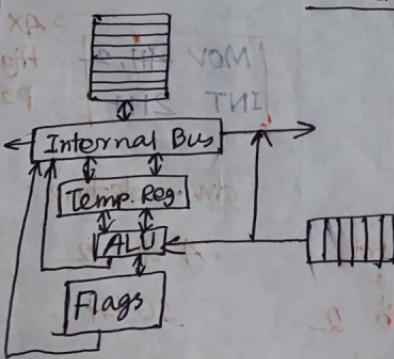
INTEL 8086.

Internal Architecture of INTEL 8086



6 byte extra instruction is stored in
Program of
Processor
Instruction Queue.

↓
Composed to stand by
Bus Interface Unit



Week - 2 / 4

Types of Registers of INTEL 8086

Data Registers:

AX - Accumulator.
 BX - Base
 CX - Count
 DX - Data

(16 bits)

Registers

Data

Registers

Registers

16 bit registers

15 —— 7 —— 0

Higher Lower

AX - Data movement

ADD A,B

Memory to Memory add kora
use jay na.

MOV AH, 1
INT 21H

AX or
Higher Part

MOV AH, 2
INT 21H

dw → define

A dw, 2

16 bit

Memory
define kora

4 db
2
MOV AL, 2

BX — Address Register :: Address store korar jomma.

CX — Loop counter.
Counter variable Left/Right shift.
store kori.

DX - data register. Used in MULTIPLICATION/
Division.

• Segment Registers:

• Code Segment:

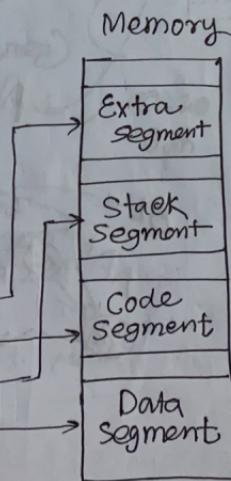
↓
অর্থাৎ/বিস্ত

অন্যকো সেগমেন্ট-এর

base address
store kore.

Registers
Four Segment in
BIU

ES 7000 H
CS 5000 H
SS 3000 H
DS 2000 H



• model small

• stack 200h

(256 b)

Temp/Variable/value

Kieku store

Korar jomma

Shurute jayga

allocate koru
hoi.

stack declare na

Korle 1KB jayga

বিহু নিবে.

Address BUS

20 bit.

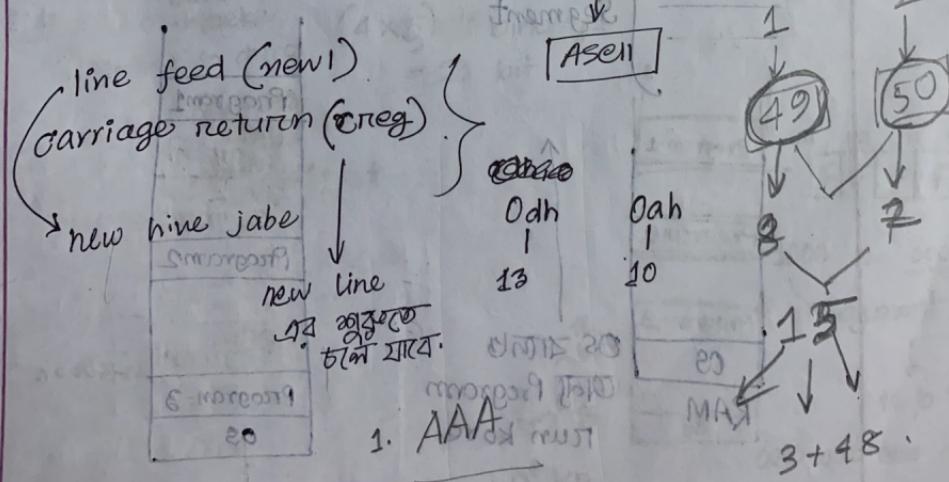
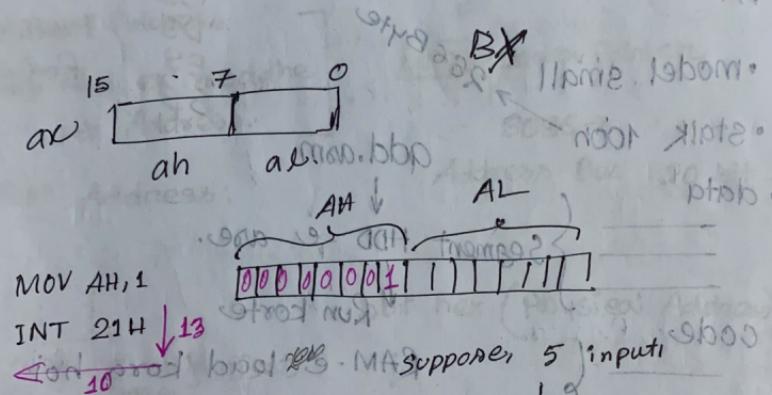
11-03-23

Lab-2

Week-3

AAA - Adjust A\$H after Addition

LEA - Load Effective Address.



14-3-23

Week - 3/4

AX
BX
CX
DX

16bit registers.

CS
DS
ES
SS

Segment Registers

• model small

X8
256 Bytes

• stack 100h

add.asm

• data

Segment HDD-e are.

• code

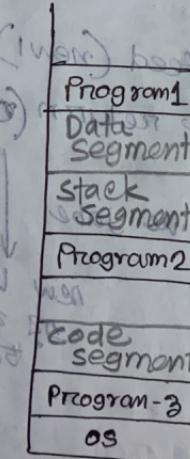
RAM-e load kora hoi

Segment

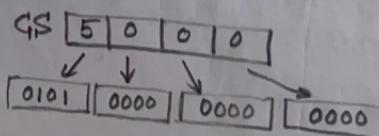
Program-1
.....
Program-2
.....
Program-3

OS

RAM
All Program
run kore



5000h

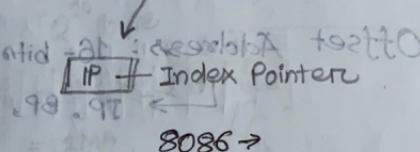


Pointers & Index Registers: pg 2

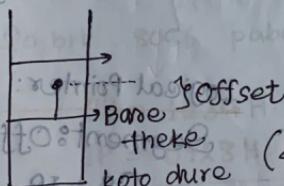
Segment Address:

Seg Reg. ex moddhe
jei Address.

23, 22, 21, 20



Offset Address:



5bit hex (Physical Address)

Address 10110
Offset 00000

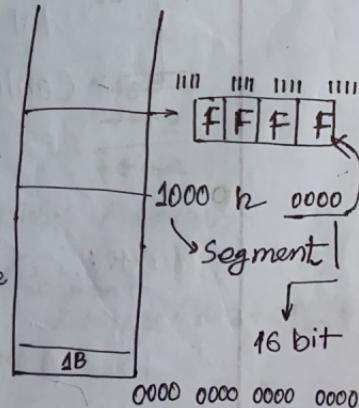
Address

10110

Offset

binary

= 20 bit.



$$2^6 \times 2^{10} B = 2^6 KB$$

location in → = 64 KB. Segment range
is Offset Address.

Segment Address: 16-bits.

↳ CS, DS, SS, ES

Offset Address: 16-bits

↳ IP, BP, SI, DI, SP.

Instruction Pointer:

Offset of next instruction in code segment.

Stack Pointer:

Logical Pointer:

Segment: Offset.

CS : IP

Stack

Base

Add.

↓

Offset

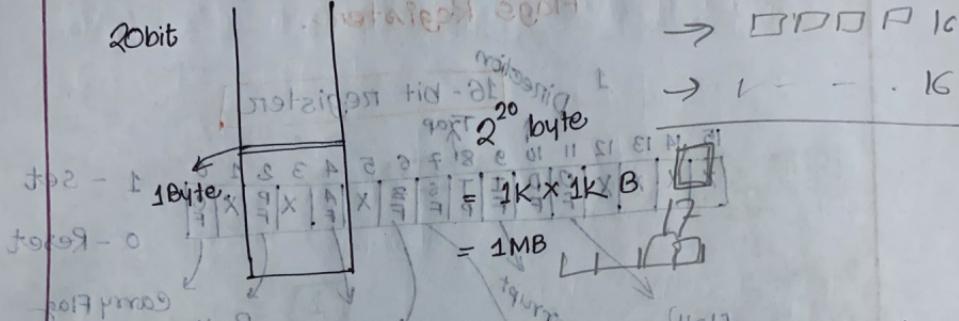
Add.

Stack Segment SS : SP → Stack
SS : BP → Base Pointer

DS:SI Source
ES:DI Index.

Destination BP er fikri
Segment er data access
korte pari.

20bit $\rightarrow \square \square \square \square 10$



Q: Segment + Offset = 16 bit + 16 bit \rightarrow 32bit Address

20 bit 8086 pabo? \rightarrow 16bit + 4 bit.

$$CS = 1234H$$

$$IP = 0128H$$

segment = 20 bits
or
 $5bit \times 4$



1100

1000

Discard na
korde -

11001



(20+16) bit
10bit \rightarrow 20 bit.

1000
0010
1000

1000
0010
1000



Physical Address

Segment Address X10

+ offset

Segment Address X10

+ offset

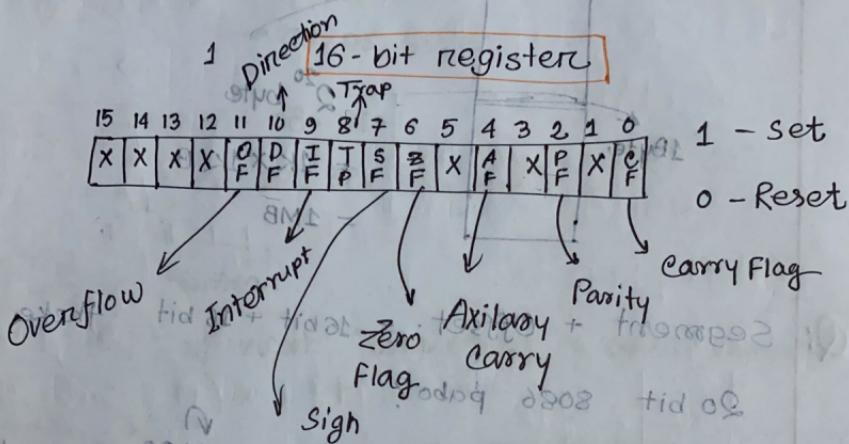
physical
address
Add.

Floux Address.

CS 3000
0000 offset.
30000 - 20 bit.

Week - 3 / 5

Flags Register.



Flags

→ Status (6) → Result or value to determine core

→ Control (3)

DF ✓
TF ✓
IF ✓

C	P	A	Z	S	C
0	2	4	6	7	11

Carry:

baki - Dont Care

zero mask

0008 2D
0000 0000
0006 1001

$AX = FFFF\ h$

$BX = FFFF\ h$

ADD AX BX \rightarrow

1 FFFE h

Chapter-1
Chapter-2
Chapter-3
Parity:

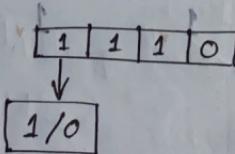
Lower 8 bit \rightarrow Even amount of 1 $\rightarrow 1$

Axiliary carry: (ONLY FOR BCD operation)

Example:

Same as carry but

considered for lower nibble.



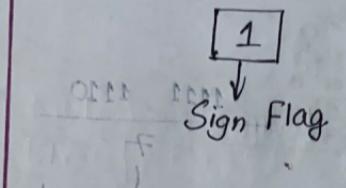
1/0

Zero : Result 0000 1 AF (Only for BCD) ①

Zero : Result 0000 0 AF (Only for BCD) ②

{ $AF(+) \rightarrow 0$
 $AF(-) \rightarrow 8$

Sign: MSB ex value.



AX = FF FF
BX = FF FF

XS YA MA

0000 0000

Sign Flag

FFFF FFFF

1

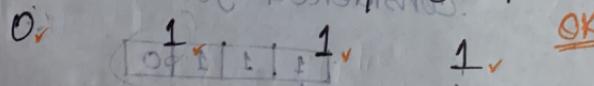
$$AX = 80 \text{ h} = 1000 \text{ 0000}$$

$$BX = 80 \text{ h} = 1000 \text{ 0000}$$

~~1 0000 0000~~

Expected different: 0

Addition: Sign equal zero Parity carry



Overflow:

① Expected sign same - no overflow.

② " " " different - overflow

0~7 (+)ve
8~F (-)ve

Subtraction La Overflow Impossible.
 /different Sign.

$$\begin{array}{r} -7 \\ +8 \\ \hline -1 \end{array}$$

$V = 0$

Chapter - 1
 Chapter - 2 } Slide.
 Chapter - 3 }

Chapter - 5

Chapter 4.



+7

-

A
 ↓
 What is it?

Topic 32 Karpoo

Object

SOURCE

SOURCE

SOURCE

SOURCE

SOURCE

18-03-23

Lab-3

Week - 4

AAA - Adjustment After Addition.

$$\begin{array}{r} f+ \\ 8+ \\ \hline 2+ \end{array}$$

MUL
DIV } Unsigned multiplication & division.

Signed or jomno:

IMUL
IDIV.

1- not good
2- not good
3- not good
Chapter 9

4- not good
5- cover
hoye
jabe

CZ signed number has different representation

kivabe use korbo:

Opcode Multiplier
IMUL source MUL BL *firiyé* *source* kivabe
MUL source ↓
DIV source Multiplier ba variable
IDIV source Multipliand

MOV AL, 2

MULTIPLICATION :

MOV BL, 83

MUL BL

$$1000 = XA$$

$$0000 = XB$$

Multiplicand.

MOV AX, 20h

MOV BX, 4h

DIV BL

After Multiplication:

$$\overleftarrow{AL \times BL}$$

$$= AL$$

Product (X)

AAM
→ Adjust

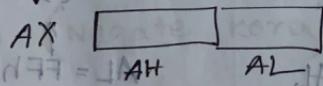
After

Multiplication

$$XA \quad ING$$

$$AL = 12 \quad DEG$$

Signed



$$@12$$

$$4$$

$$0 = 7F$$

$$0 = 70$$

Remaind



$$(8 \times 8) \text{ bit} = 16 \text{ bit}$$

Divisor

22-03-23

Week-04/05

SUB AX, BX

Chapter-5

$$AX = 8000h$$

$$BX = 0001h$$

$$\begin{array}{r} 8000 \\ -0001 \\ \hline 7FFF \end{array}$$

VOM

IUM

✓
✗

Carry flag = 0

$$PF = 1$$

$$SF = 0$$

$$ZF = 0$$

$$OF = 1$$

$$i = 5$$

++ } Incrementation.

EMU:

INC AX

INC

AL

AL = FFh

DEC

AL = 100h

Carry Flag INC-ex

যারা Affected হবে না।

Also, DEC

$$PF = 1$$

$$SF = 0$$

$$ZF = 0$$

$$OF = 0$$

$$\begin{array}{r} + \\ 0100 \\ +1 \\ \hline 0101 \end{array}$$



carry आजे ओ यह राख याह $OF = 0$ } F017
 borrow नियु आवाह (यह राख याह) $OF = 0$. } F017 MSB.

गृहीत (+)ve प्रदान (-)ve
sign (+)ve sign (+)ve

Overflow to next Carry to next

$\Rightarrow \text{Overflow} = 1$.

MOV AX, 5h : MOV Operation - 4 Flag unaffected

Example 5.5: Flag unchanged.

(Compliment to number) $0 = 11$

NEG_i (Negate kore) ~~word~~ \downarrow ~~Flag~~

AX = 5h 0005h ~~word~~ $NZFS=1$

NEG_i AX 0101 ~~word~~ $ZF = 0$
~~..... 1011~~ $PF = 0$

0005 h ~~not~~ FFFFh ~~now~~ $OF = 0$

~~CF = 0~~

NEG_i $CF = 1$
 kore/
 always

zero
thakle $CF = 0$
NEG_i
Kore

82M Trap Flag: 0 = 70 अपने की तरफ चला जाता है।

TF = 1 थोक्को Single Step Run karte जाती है।

- Interpreter line by line Before & after run of programme.

Interrupt Flag: 0 = 90 VOM : AX, BX, CX, DX, SI, DI, BP, SP

IF = 0 (Interrupt ignore)

IF = 1 (Enable, kora) ↓ NEG (negative states)

SW/HW. Interrupt

String processing higher → lower. DF = 1

lower → higher DF = 0

0 = 70
IF = 0
NEG
KORI
ALWAYS

IF = 1
NEG
KORI
ALWAYS

29-4-23

Lab-4

Week-5

WRITE PROGRAM:

Enter two number: 5 6

$$\text{Sum} = 11$$

Enter two number: 5 3

$$\text{Sub} = 2$$

Enter two number: 5 2

$$\text{Product} = 10$$

Enter two number: 8 3

$$\text{Quotient} = 2$$

$$\text{Remainder} = 2$$

Discussion: Flag er
value.

[Single
Step.]

Flag 1: 880 & 8803

Ans: VI - US

A. \rightarrow same jinsh
etnommas

objectives
definition
of objects

2-4-2023

CS-4-OS

Week-5/4

4-APR

2-APR

Chapter-4

• model small

• stack 100h

• data → Directive

msg

a

db

db

Pseudo-op

main proc → Directives

MOV AX, @data

MOV DS, AX → Instruction

.....

main endp

end main

Statementer format:

Name - operation - operand/s

comments

[name

operation

operand/s

comments]

L1:

MOV

AS, AX

;-----

INSTRUCTION

Model - er size define korte.

256 byte jayga allocate kori.

bt = code

f = data

EFER - F0000000000000000

O1 = T0000000000000000

OT

S = T0000000000000000

Chap-5

Flags

Chap-3

• G Register → 16 → 20 bit
S. " addresses

• Physical Address calc!

• Konta koto bit.

• 8086-8088 • Logical Addresses

Chap-1

• Figure!

• EU = IU • Bus Architecture

Statement:

Code लाइन

Statement
Instruction

Assemblers [Ass → Mac]

Directives.

Assembler

Ass L → Mac L.

Ass L → Mac L. [Operation हो ना]

जटिल. इत्यता. [Memory Allocation]

11:
Name

msg
Names

bdb X "Hello \$"

X1 XA VOM

main proc

Name Operation

Conversion: Character [1-31]
tid डिक्सिङ्ग ब्रॉड

std std std std std std std std

00100000 00100000 00100000 00100000

01000000 01000000 01000000 01000000

00100000 00100000 00100000 00100000

00000000 00000000 00000000 00000000

00000000 00000000 00000000 00000000

00000000 00000000 00000000 00000000

00000000 00000000 00000000 00000000

00000000 00000000 00000000 00000000

00000000 00000000 00000000 00000000

00000000 00000000 00000000 00000000

00000000 00000000 00000000 00000000

00000000 00000000 00000000 00000000

00000000 00000000 00000000 00000000

00000000 00000000 00000000 00000000

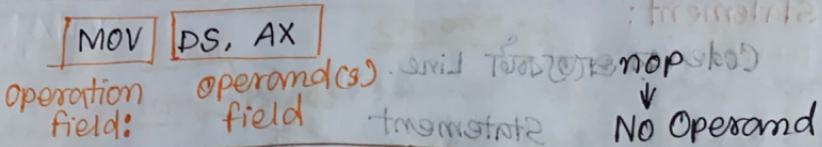
A a → Same jinish

? @ \$ - %

Hexa Num: OFFh

Name with no digit as initial.

Majhkhame
thakte parbe
OK na



Opcode → Instruction

Pseudo-opcode → Directives

Opcode → Machine code - to convert hobe

Pseudo op

Opcodes: MOV, ADD, SUB, MUL, DIV, INC, DEC, NEG

INC AX → 1 byte
MOV AX, DX → 2 byte

Comments: → ;

To increase readability.

:; ;

db - 1 byte

dw - 2 bytes

dq - 8 bytes

dd - 16 bytes [Double define]

dt - 10 bytes [Double define]

bword 2x16 bit

word 16 bit

long 32 bit

quadword 64 bit

doubleword 128 bit

octoword 256 bit

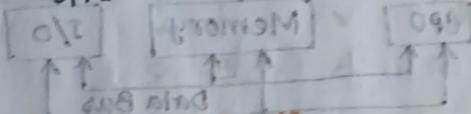
clinit emode = 0 A

Array:

int a [5]

a → base address

a+1 →



a bd 30h, 31h, 32h - ASCII

→ a a+1 a+2
→ a [0 1 2] - Decimal.

Parity 1byte 1 ↳

a bw 30h, 31h, 32h.

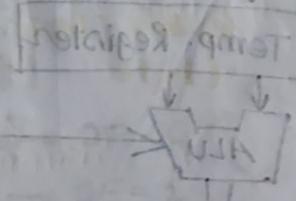
a a a+2 a+4
[0 1 2]
2byte

#define N 100

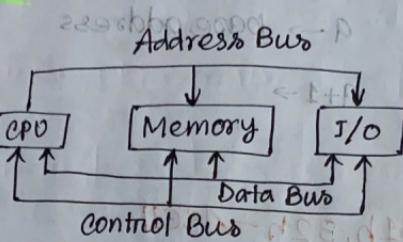
11-

EQU (Equates)

a EQU 5h

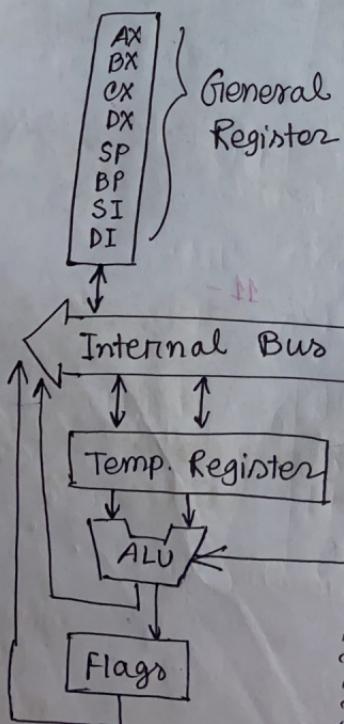


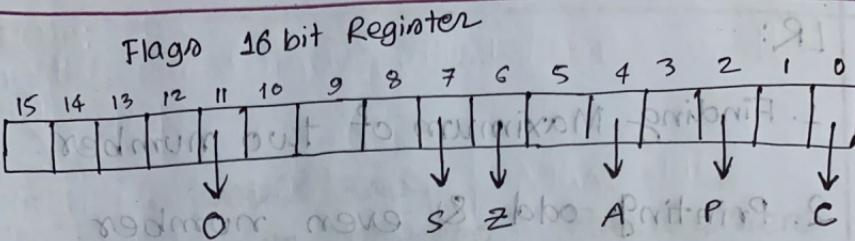
Extra:



Bus Connection of a Microprocessor.

Execution Unit





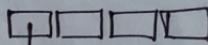
Carry: Operation ex carry.

Parity: Last 8 bit e

Amount of 1 even hole $\rightarrow 1$.

Auxiliary Carry: BCD te

lower nibbler 4 bit



A: $1/0$ XA \downarrow XA + XA, XA 9MD

XU XA - XA \leftarrow XA, XA 802

zero: 8 bit / 16 bit अव zero hole Yes $\rightarrow 1$
No $\rightarrow 0$.

Sign : Sign bit $\rightarrow 1/0$ not zero

Overflow: $+ + \rightarrow + \rightarrow OF = 0$
 $+ - \rightarrow - \rightarrow OF = 1$

\oplus - $\rightarrow + \rightarrow OF = 1$
 $\rightarrow - \rightarrow OF = 0$

6-5-23

Lab-5

Week- 1/6/1

LR:

1. Finding Maximum of two numbers.

2. Printing odd & even number.

Chap-6.

1. Conditional & Unconditional.

JMP

Conditional

Unconditional.

JUMP when zero

CMP AX, BX \rightarrow AX = AX

SUB AX, BX \rightarrow AX = AX - BX

But AX is value
compare how

JUMP

IF

Greater

JG

JL

$\downarrow = 70$

IF

JUMP

LESS

JL

$\downarrow = 70$

CMP

JG

JL

$\downarrow = 70$

G/L

6h

5h

7h

8h

9h

10h

11h

12h

20-5-25

Lab-6

Week-7/1

CMP
SUP

JZ } Jump if zero(A) ← X8, XA, DDA
JNZ } or Not zero. Flag Register ← X8, XA, FR=1

Subtract ← X8 - XA = XA ← X8, XA, DDA

BL K 16 bit ← extend kora. XA ← X8, DDA

AX ← XA ← XA, DE

AT (in 3's complement) ← XA, DE

Mov AX, AT

(most significant bit first) ← AT ← 3

3's complement of dividend ← 3's complement of divisor

	Divisor	Quotient	Remainder	SR	DR	CF	OF
Model	X	✓	✓	✓	✓	✓	✓
Small	X	✓	X	✓	✓	✓	✓
Medium	X	X	✓	✓	✓	✓	✓
Large	X	✓	X	✓	✓	✓	✓

Describes count of remainders

22-05-23

22-05-02

Week-7/3

Q-301

188-400W

942

Different Opcodes: ADD, SUB, INC, DEC, NEG

ADD AX, BX → $AX = AX + BX$ → Addition

Subtracting
SUB AX, BX → $AX = AX - BX$ → Subtraction

INC AX → $AX++$ → Increment

DEC AX → $AX--$ → Decrement

NEG AX → 2's complement.

$$AL = 3$$

$$BL = -5$$

$-2 \rightarrow AL$ (in 2's complement form)

General Segment Memory Location

SOP	POP	GR	SR	ML	Constant
GR		✓	✓	✓	X
SR		✓	X	✓	X
ML		✓	✓	X	X
Constant		✓	X	✓	X

Destination can't be constant

ek segment

theke arek

segment

register nite

parbo na.

Address fixed

MOV DS, SS X

MOV A, B1 X

MOV AX, BX

MOV AX, @data constant

MOV DS, AX



model small keno likhi?

Small

medium

compact

large

huge

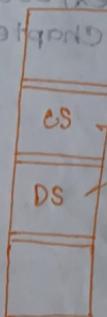
When where to use?

Next: Chap-8

N.B. Look over charts from

Textbook
Chapter-4

	Model	Description
code < 1 data < 1	Small	Code & data 64 KB - cross na kore (In one segment)
code > 1 data < 1	Medium	Code in in one segment er beshi Data in one segment
code < 1 data > 1	Compact	Code in one segment Data in more than one segment
code > 1 data > 1	Large	Code & Data more than one segment (No. array larger than 64 KB)
code > 1 data > 1	Huge	Code & Data more than one segment (Array larger than 64 KB)



Segment size - [64 KB]

Why??

→ Code conversion programme

INT 21H AH - 01 - Char input
 AH - 02 - Char output
 AH - 09 - String Output

ASCII

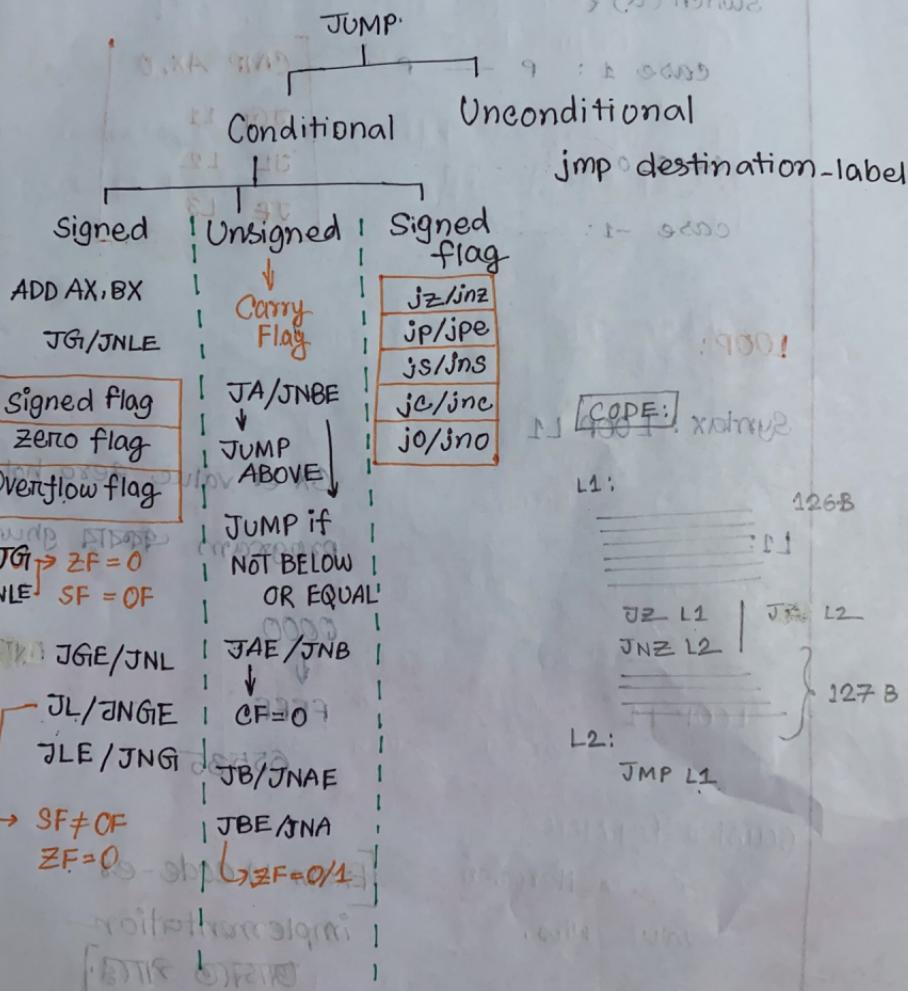
Assembly Run korar steps

Next: Chap-6.

24-May-23

Week-7/5

Chapter-6.



int a;

switch (a) {

case 1 : P + P

long fibbonacci

case 0 : mi

case -1 : ...

LOOP:

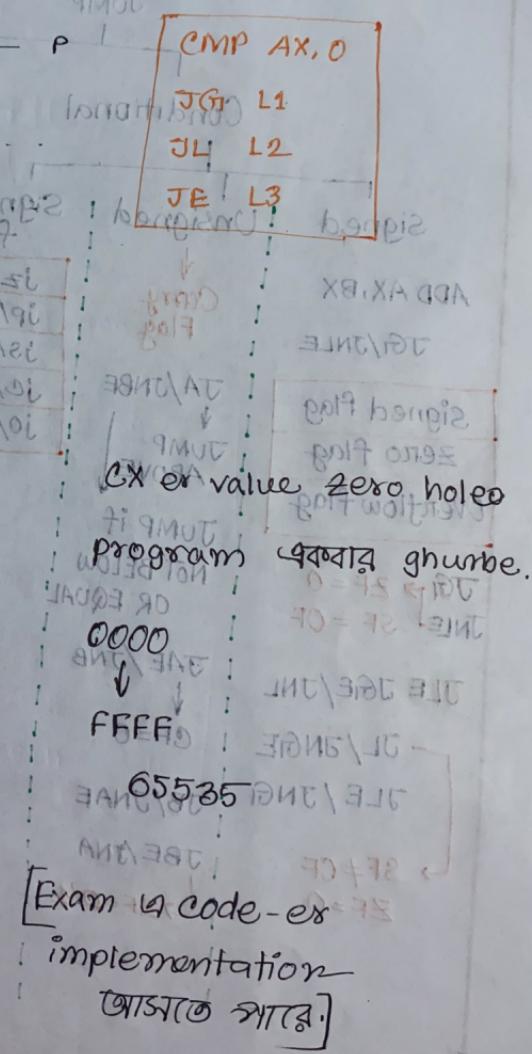
Syntax: LOOP L1

L1:

LOOP L1

Counter Register

CX → a iteration
value Nib.



29-05-23

Week-8/3

Chapter-7

Rotate Instruction, Logic, Shift

AND
OR
NOT
XOR

$$\begin{array}{lll} b \text{ AND } 1 = b & b \text{ OR } 0 = b & b \text{ XOR } 0 = b \\ b \text{ AND } 0 = 0 & b \text{ OR } 1 = 1 & b \text{ XOR } 1 = \sim b \end{array}$$

$$\begin{array}{c} 10101101 \\ \text{AND} \boxed{01111111} \\ \text{A} \end{array} \rightarrow \text{MASK}$$

jeta clear korte chay oita zero kore
baki shob 1 (one)

$$\begin{array}{c} 10101101 \\ \text{MASK} \leftarrow \boxed{11111110} \end{array} \text{ AND.}$$

jeta set korte chay oita one kore
baki shob 0 (zero).

OR

Flip korar jonno $\boxed{\text{XOR}}$

shob bit zero kore felas jomno:

AND AL, 0000 0000

SUB AL, AL

XOR AL, AL

Example:: Check

A = 97

$\hookrightarrow 01100001$

A = 65

$\rightarrow 01000001$

RESET \rightarrow AND
SET \rightarrow OR

b = 01100010
D F

B = 01000010
2 0

AL 1111 0000

BL 0000 1111

(Cores) 0 \rightarrow [V V V V]

AND AL, BL [and ex value] \rightarrow B = 0000 1111

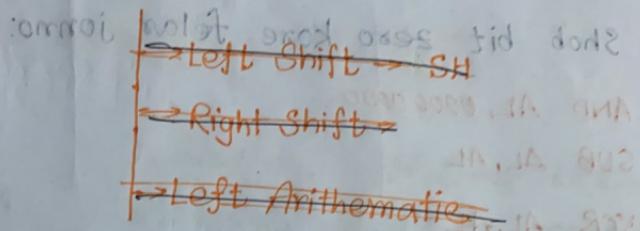
TEST AL, BL [AND ex value; alpt kaz kore]

like CMP, SUB but AL ex

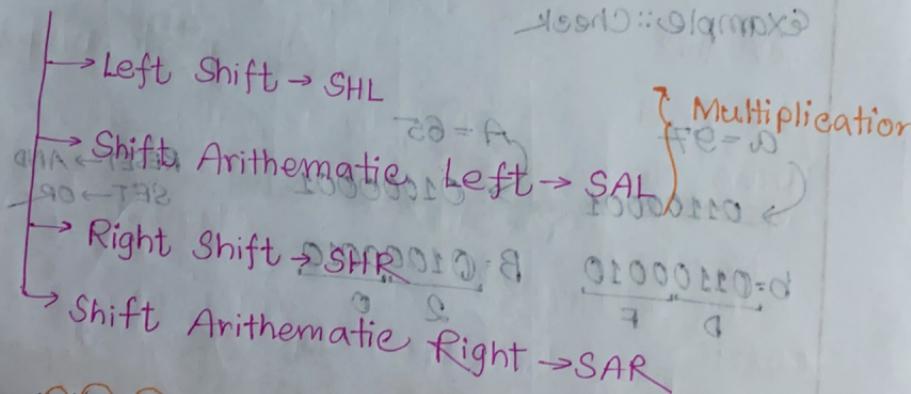
value unchanged & flag

+ AL ex value change

Shift



Shift



ekta shift
>1 shift

LSB = 0.
SHL AL, 1
SHL AL, @L 213/4 +

Shift Arithmetic Left) \rightarrow MSB : Right Shift

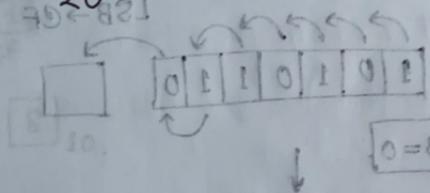
0000 0101

0000 1010 \rightarrow 10

0001 0100 \rightarrow 20

10101101
10101101

Left shift 2x
Multiply kore



Shift Right Committee

10101101
10101101

01101101

0000 1010
0000 1010

01101101
01101101

0000 1010
0000 1010

01101101
01101101

SHR AL

(Long) Right shifting: Right shift committee

0000 1010
0000 1010

01101101
01101101

0000 1010
0000 1010

01101101
01101101

SHR AL

0000 1010
0000 1010

01101101
01101101

0000 1010
0000 1010

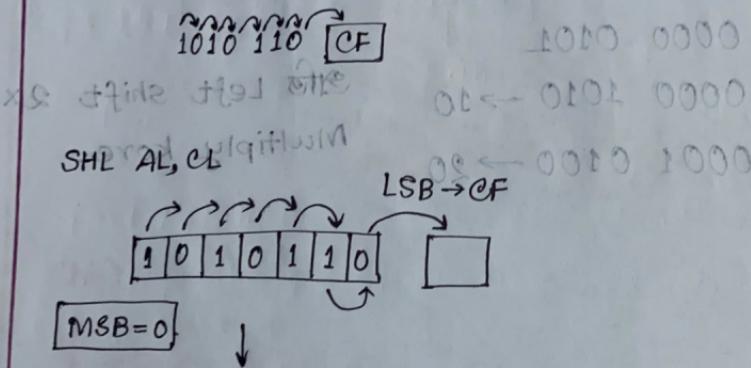
01101101
01101101

SHR AL

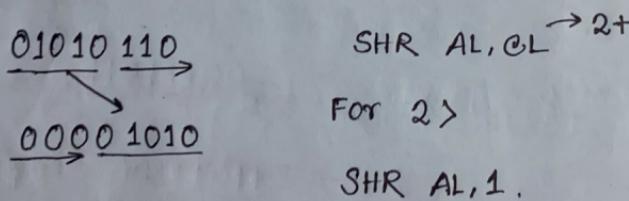
30-05-23

Week-8/4

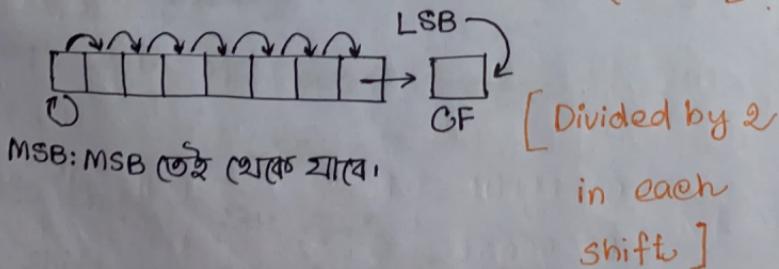
Shift Right: SHR (Unsigned)



3 times Right Shift.

01010 110 SHR AL, CL $\rightarrow 2^+$

For 2 >
SHR AL, 1.

Shift Arithmetic Right:: Division kori. (Signed)



$$(15)_{10} = [00001111]_2$$

Explain
S = 15 E = 7D

2's complement,

11A8

$$\begin{array}{r} 11110001 \\ -8 \\ \hline 11111000 \end{array} \rightarrow \boxed{1} \quad \text{CF}$$

Sign bit is omitted here

$$[00001000]_2 = \boxed{8}_{10}$$

Overflow, 1 = wolfie

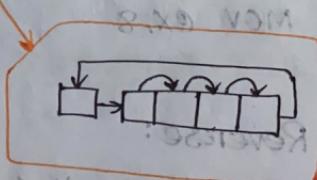
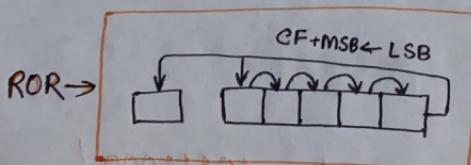
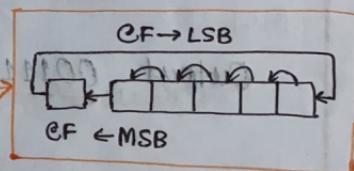
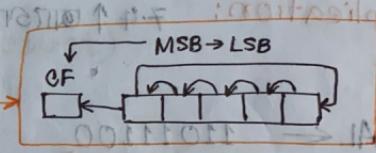
Rotate Instruction:

→ ROL: Rotate Left

→ ROR: Rotate Right

→ RCL: Rotate Carry Left

→ RCR: Rotate Carry Right



ROR AL, CL

DL
CL

Example 7.14

CF = 1 CL = 3

[1]

RCR
DH, CL

8Ah

(12)₁₀ = (00001111)

This combination

10000000

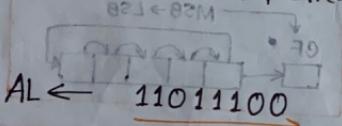
Last Rotation - e sign change huye gele

Overflow = 1, otherwise OF = 0.

Application:

7.4 ↑ AL or

Binary & Hexa input/output
Routine Implementation



ROR: Rotate Left
8/BL ← 8

ROR: Rotate Right

ROR: Rotate Left
Example #*

ROR: Rotate Right

ROR: Rotate Left
Example #*

ROR: Rotate Right

ROR: Rotate Left
Repeat.

MOV CX, 8

Reverse:

SHL AL, 1

RCR BL, 1

Loop Reverse

MOV AL, BL

1 10111000

0 10000000

GT DF

End Chap-7
Next Chap-8

31-05-23

Chapter-9 Multiplication & Division Instruction.

Unsigned & Signed Multiplication:

MUL BX

IMUL BX

(For 16 bit)

AX ← Multiplicand

BX ← Multiplier

DX:AX

32 bit (Product)

For 8 bit:

MUL BL

IMUL BL

AX → 16 bit (Product)

S Z AC P

→ Undefined for

Unsigned MUL

O C → Defined.

Unsigned ?

Carry Flag: Upper Half zero hole CF = 0

OF = 0

Signed Multiplication:

$CF/OF = 0$

habe when $MSB = 1$ hole

$DX = 111 \dots$

(tid BE stop)

$[BX \quad DX]$

$MSB = 0$

$DX = 000 \dots [AX]$

Example:

$AX \leftarrow 1$

$BX \leftarrow FFFFh$

Multiplication $\rightarrow XA$

Multiplication $\rightarrow XB$

Product		<u>DX</u>	<u>AX</u>
MUL BX	$\rightarrow FFFF$	$0000h$	$FFFFh$

$IMUL BX \rightarrow \underline{FFFF, FFFF}$ $FFFFh \times FFFFh$

(Ausbildung) tid BE $\leftarrow XA$ \leftarrow $OF/OF = 0$

Example: 9.5

$AL \leftarrow 80h$ rot $\rightarrow -128$

$MUL BL \rightarrow 7F80$

$IMUL BL \rightarrow 128$

$D = 70$

$BL \leftarrow FFh$ rot $\rightarrow -1$

$7F \quad 80$

beendet $\leftarrow 0$

ausbildung $\rightarrow 0$

10-6-23

Week-9/1

CS-601-23

CR-2023/24

DIV BL AH AL
IDIV Divide
Divisor AL
Dividend DX
DX ← AX : DX
0000
Initial
Initial
AL → 0000
DX → 0000
e → 0000

String Reverse

Binary Conversion

8bit

Divisor BX ← 16 bits

BX clear XOR (XOR)

DX → 0000
BX → 0000
DX → 0000
BX → 0000
DX → 0000
BX → 0000

	DX	AX	B	D
DIV	0000	0005	0	0
IDIV ←			1	1
			2	2

12-06-23

82-6-01

Week-9/3

DATA STRUCTURE

$$DX:AX \rightarrow DX \quad AX$$

0000

IN HH 18 VI
Status flag Undefined
↑

Factorial

$$CX \leftarrow 9$$

0000 0000
Loop A
1111 0000

Division

$$AX \rightarrow \text{Divisor} \quad CF$$

DX:AX
Quotient print2

Remainder Quotient
AH AL

$$\text{Dividend} = \text{Divisor} \times \text{Quotient} + \text{Remainder}$$

3
2
1
0
-1
-2
-3

(DX) BX

$$\text{Dividend} \quad DX \leftarrow 0000h$$

$$AX \leftarrow 0005h \quad \text{Div} \quad BX$$

$$BX \leftarrow 0002h \quad IDIV \quad BX$$

$$\begin{array}{c|c|c|c|c} & Q & R & AX & DX \\ \hline 2 & & 1 & 0002 & 0001 \\ \hline & & & 0001 & \xrightarrow{\text{DIV}} \\ & & & & \xrightarrow{\text{IDIV}} \end{array}$$

$DX:AX \rightarrow 0000 : 0005h$

$BX \leftarrow FFFE h$ (*Unsigned 05534*)
Signed -2

1110
 $0010 \rightarrow 2$

Q		R	AX	DX	
0	5		0000	0005	(DIV)
-2	1		FFFE	0001	(IDIV)

Divide Overflow:

$AX \leftarrow 00FBh \rightarrow 0000 0000 1111 1011$

$BL \leftarrow FFh \rightarrow 1111 1111 255$

Q		R	AL	AH	
0	251		00	FF	(DIV)
				0001	(IDIV)

Divide
Overflow

$\frac{-5}{2}$

CBW
CBD
Automatically DX:AX
Convert word to double word

GT-3

DIV DX:AX
 IDIV Quotient DX
 Remainder AX
 ← 0100 9:12
 CWD (extend sign to DX)
 MOV BX, 7

Byte DIV BX
 9:13 (DIV) 0000 0000 | 0000 0000 | 12 B | 0
 MOV AL, (XBYTE) 0000 0000 | 0000 0000 | 12 B | 0
 CWD
 MOV BL, -7
 IDIV BL

MOV AX, S

IMUL A : word division
 B

MOV AX, AX → XA

MOV AX, 12 → BX

IMUL B

SUB A, AX

SHL

SAL

SHR

SAR

CF

0 → CF

CF

Division
 overflow

19-06-23

Week-10/3

String Instructions

Direction flag (control Flag), private modification

DS: Segment Address

ES: Extra Segment Address

Str1 DB 'ABCDE'

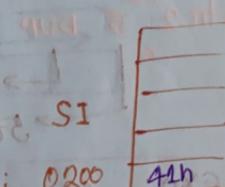
offset Address Content

ASCII chars

DS: SI → Source String

ES: DI → Destination String

offset Address	content	ASCII Char
0200	41h	A
0201	42h	B
0202	43h	C
0203	44h	D
0204	45h	E



CLD → Clear Direction Flag

SLD → Set

Source String SI H E L L O str 1

Destination String (empty) str 2

↓
destination memory DI

SI & DI depends on DF

Code: DB 'HELLO' ES:DI 5 DUP (?)

• DATA

str1	DB 'HELLO'	mask	Hex	Binary
str2	5 DUP (?)	A	HEE	0101
			HEE	0101

→ Duplicate A
I2 = 5690

Exp: SP DW 212 DUP (0)

• CODE

main proc

MOV AX, @data
 MOV DS, AX Extra Segment (এ কোনো)
 MOV ES, AX → Segment Register er Value.

LEA SI, str1

LEA DI, str2

CLD

MOVSB

MOVSB

MOVSB

PS DI

MOVSB

MOV CX, 5

REP MOVSB

ADD SI, 4

STD

MOVSB

ADD \$DI, 2

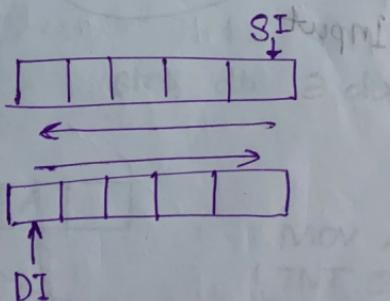
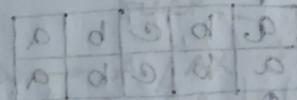
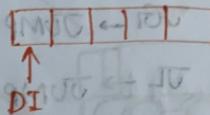
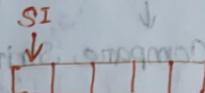
MOV CX, 5

L1:

MOVSB

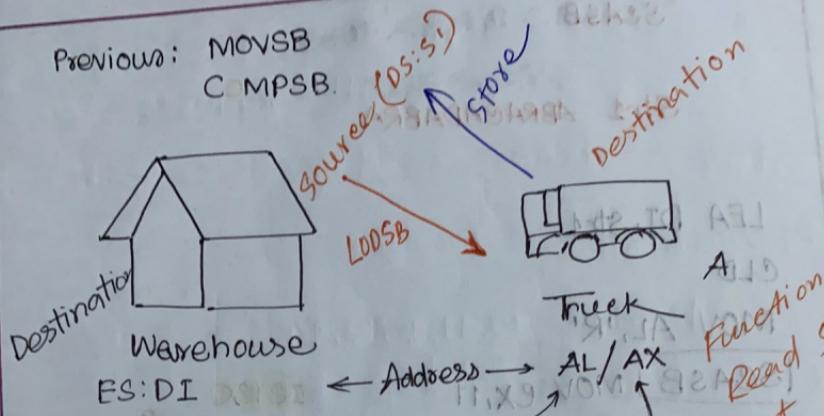
ADD \$I, 2

LOOP L1

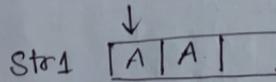


10th July
Week-10/3.

10th July
Week-10/3.



LEA DI, Str1



MOV AH, 1

INT 21H

STOSB

STOSB

L1:

STOSB

INT 21H

LOOP L1

AL ← A

MOV AX, @data

MOV ES, AX

LEA DI, Str1

CLD (left to right).

Code from Book

Character input, BX++, count, i/p.

17th July

Week-11/3.

QUESTION
EX-Address
test - ds1

Chapter-10

Arrays & Addressing Mode.

Array

Declaration

A db $\frac{10, 11, 12, 13, 14}{8}$ 8 bit

B db 5 dup (0) \rightarrow (?) uninitialized

<u>Index</u>	<u>Element</u>	<u>Symbolic Address</u>
1	A[1]	A
2	A[2]	A + Sx1
3	A[3]	A + Sx2
4	A[4]	A + Sx3
5	A[5]	A + Sx4

S = 1 \rightarrow Byte

= 2 \rightarrow Word

A[N] \rightarrow A + Sx(N-1)

$W[10] \leftrightarrow W[25]$ word
 $W+18$ $W+48$
 $XGNGI$ $W+18, W+48$ } Not Possible.

MOV AX, W+18.

XGNGI W+48, AX

MOV W+18, AX

DUP operator ଟି Nested ପାଇଁ.

At db 5,4,3 dup (2,3 dup(0), 1)

At db 5,4,3 dup (2,0,0,0,1).

5,4,3,2,1,0,0,1

Addressing Mode:

XA, XA Box

The way in which the operands are

specified.

MOV AX, BX → Register Mode.

MOV AX, 3 → Immediate Mode (constant)

MOV AX, NUM → Direct Mode.

More four types of Addressing Mode.

4. Register Indirect Mode:

[BX] [0100h]

BX → 0100h

[BX] → 35F9h.

5. Based Mode.

6. Indexed

7. Based-Indexed

[BX, SI, DI, BP] → SS

DS. ↓

Offset Address.

W DW 10, 11, 12, 13, 14 F 000, F, SS, DS

• Code

XOR AX, AX

SBBLT BX

LEAD SI, W.

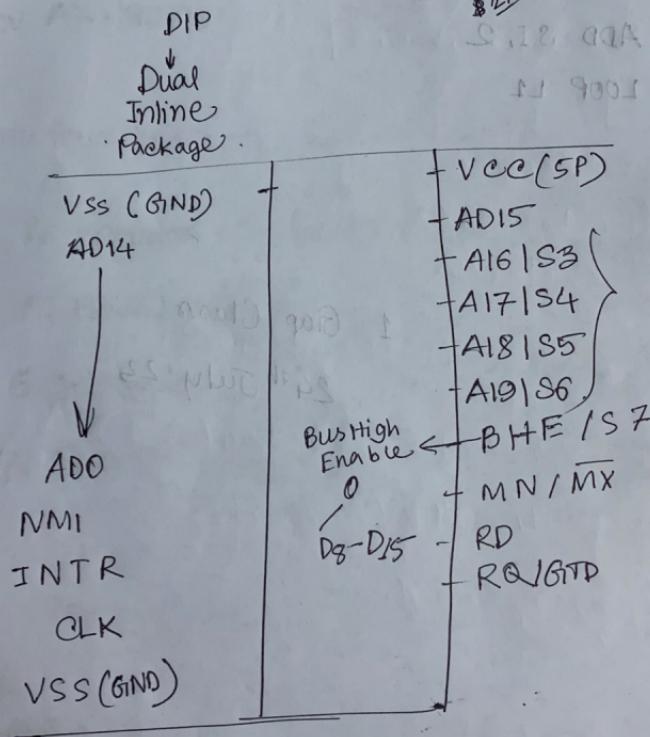
LOOP charaye content gya newar try
Korbo.

25th July '23

Week-12-

Pin Diagram of 8086.

Intel 8086. - 40 Pin



প্রচুর Signal আদান প্রদান হয় → 2^{তা} Ground