**CSC 3210 Computer Organization and Programming (Spring 2025)**
**ASSIGNMENT-1**

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1. **Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2. [40 points]**

   P1: $3 \times 10^9$ GHz/1.5 = $2 \times 10^9$ IPS, P2: $2.5 \times 10^9$ GHz/1.0 = $2.5 \times 10^9$ IPS, P3: $4.0 \times 10^9$ GHz/2.2 ≈ $1.82 \times 10^9$ IPS

   a. **Which processor has the highest performance expressed in instructions per second?**

      P2 has the highest performance expressed in instructions per second with $2.5 \times 10^9$ IPS

   b. **If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.**

      P1: $(3.0\times10^9) \times 10 = 3.0\times10^{10}$ cycles, $(3.0\times10^{10})/1.5 = 2.0\times10^{10}$ instructions

      P2: $(2.5\times10^9) \times 10 = 2.5\times10^{10}$ cycles, $(2.5\times10^{10})/1.0 = 2.5\times10^{10}$ instructions

      P3: $(4.0\times10^9) \times 10 = 4.0\times10^{10}$ cycles, $(4/0\times10^{10})/2.2 = 1.82\times10^{10}$ instructions

   c. **We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?**

      1 – 0.3 = 0.7, 1/0.7 = 1.43, (1 + 0.2) = 1.2, 1.43 × 1.2 × clock rate = 1.714

      P1: 1.714 × 3.0 = 5.14 GHz

      P2: 1.714 × 2.5 = 4.29 GHz

      P3: 1.714 × 4.0 = 6.86 GHz

2. **Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D). P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2. Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows:**

**10% class A, 20% class B, 50% class C, and 20% class D, which is faster: P1 or P2? [30 points]**

a. What is the global CPI for each implementation?

P1: Global CPI = $(0.1\times1) + (0.2\times2) + (0.5\times3) + (0.2\times3) = 2.6$

P2: Global CPI = $(0.1\times2) + (0.2\times2) + (0.5\times2) + (0.2\times2) = 3.0$

b. Find the clock cycles required in both cases.

P1: $1.0E6 \times 2.6 = 2.6E6$ cycles

P2: $1.0E6 \times 2.0 = 2.0E6$ cycles

3. **Consider the following two processors: P1 has a clock rate of 4 GHz, average CPI of 0.9, and requires the execution of 5.0E9 instructions. P2 has a clock rate of 3 GHz, an average CPI of 0.75, and requires the execution of 1.0E9 instructions. [30 points]**

   a. **One usual fallacy is to consider the computer with the largest clock rate as having the highest performance. Check if this is true for P1 and P2.**

   P1: $(5.0 \times 10^9) \times 0.9 / 4.0 \times 10^9 = 1.125$ sec

   P2: $(1.0 \times 10^9) \times 0.75 / 3.0 \times 10^9 = 0.25$ sec

   P1 has a higher clock rate while P2 is faster. The fallacy is disproven because higher clock doesn't always equal higher performance

   b. **Another fallacy is to consider that the processor executing the largest number of instructions will need a larger CPU time. Considering that processor P1 is executing a sequence of 1.0E9 instructions and that the CPI of processors P1 and P2 do not change, determine the number of instructions that P2 can execute in the same time that P1 needs to execute 1.0E9 instructions.**

   P1: $(1.0 \times 10^9) \times 0.9 / 4.0 \times 10^9 = 0.225$ sec

   I: $(0.225 \times 0.3 \times 10^9)/0.75 = 0.9 \times 10^9$

   This fallacy is disproven because P1 executes more instructions than P2 at the same time, proving that more instructions' execution does not lead to longer execution times

c. **A common fallacy is to use MIPS (*millions of instructions per second*) to compare the performance of two different processors and consider that the processor with the largest MIPS has the largest performance. Check if this is true for P1 and P2.**

P1: 4GHz → 4000MHz/0.9 = 4444.44 MIPS

P2: 3GHz → 3000MHz/0.75 = 4000 MIPS

This fallacy is disproven because even though P1 has a higher MIPS, P2 is proven to completing the task faster. Higher MIPS does not always have the best performance.