CSC 3210 Computer Organization and Programming (Spring 2025)

ASSIGNMENT-1

This is assignment 1, the due date for this assignment is 02/06/2025, 11:59pm. Please submit another pdf file for your answer. Your answer paper should include your name, session number, and email address.

1. Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2. [40 points]

a) Which processor has the highest performance expressed in instructions per second?

b) If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.

c) We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

2. Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D). P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2.
   Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which is faster: P1 or P2? [30 points]

a) What is the global CPI for each implementation?

b) Find the clock cycles required in both cases.

3. Consider the following two processors: P1 has a clock rate of 4 GHz, average CPI of 0.9, and requires the execution of 5.0E9 instructions. P2 has a clock rate of 3 GHz, an average CPI of 0.75, and requires the execution of 1.0E9 instructions. [30 points]

a) One usual fallacy is to consider the computer with the largest clock rate as having the highest performance. Check if this is true for P1 and P2.

b) Another fallacy is to consider that the processor executing the largest number of instructions will need a larger CPU time. Considering that processor P1 is executing a sequence of 1.0E9 instructions and that the CPI of processors P1 and P2 do not change, determine the number of instructions that P2 can execute in the same time that P1 needs to execute 1.0E9 instructions.

c) A common fallacy is to use MIPS (*millions of instructions per second*) to compare the performance of two different processors and consider that the processor with the largest MIPS has the largest performance. Check if this is true for P1 and P2.