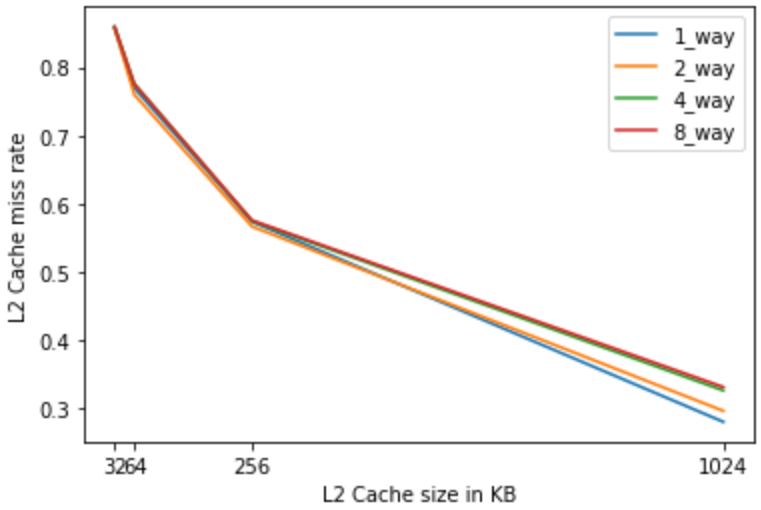
Memory size taken: 512 MB
L1 cache:
Tag latency =2
Data latency=2
Response latency =2

L2 cache:
Tag latency =10
Data latency=10
Response latency =10

System clock is 1 GHz
2(b)

memory(kB)_associativity	Miss rate
32_1	0.8579
32_2	0.8577
32_4	0.86
32_8	0.859
64_1	0.7699
64_2	0.76
64_4	0.7767
64_8	0.77537
256_1	0.573
256_2	0.566
256_4	0.5738
256_8	0.575
1024_1	0.2789
1024_2	0.295
1024_4	0.325
1024_8	0.33



2(c)

Analyzing the impact of L2 cache size:

We can clearly observe that the miss rate drastically decreases with the increase in the size of cache, from 32 to 1024 KB, be it a 1-way, 2-way, 4-way or 8-way associative cache. This can be intuitively explained by the fact that as the cache size increases, a larger number of data blocks can be stored in it at a given time, thus the probability of finding a particular block increases, leading to a greater number of successful cache hits or reduced cache misses.

Analyzing the impact of set associativity:

Coming to the comparison wrt associativity, at some places greater associativity leads to an improved miss rate, whereas for the other memory values it is the quite opposite.

1. From 1 way to 2 way
   We observe that the miss rate decreases from 1 way to 2 way for 32 KB, 64 KB and 256 KB. On the other hand it increases for 1024 KB.
2. From 2 way to 4 way
   We observe that the miss rate increases from 2 way to 4 way for all the 4 cache sizes.
3. From 4 way to 8 way
   We observe that the miss rate decreases from 1 way to 2 way for 32 KB and 64 KB. On the other hand it increases for 256KB and 1024 KB.

The miss rate is generally expected to decrease with increasing associativity, as per the graph provided in the assignment, because the conflict misses are expected to decrease as the number of addresses available in each set increases.

But as we can see, for 1024 KB as associativity increases the cache miss rate increases. Thus, we can't make any strong conclusions about the relationship between associativity and the miss rate. It is a very complex trend which is dependent on the benchmark that we are executing as the combination of memory accesses varies with the instructions listed in the program. The difference in the above graph and the graph given in the assignment could be due to the different benchmarks, memory size, latencies and mshrs.