Network-on-Chip Architectures for Signal Processing and Error Control Coding Applications

Poster · January 2017

DOI: 10.13140/RG.2.2.17576.57602

3 authors:

N. Prasad
Advanced Micro Devices
24 PUBLICATIONS **128** CITATIONS
SEE PROFILE

Santanu Chattopadhyay
Indian Institute of Technology Kharagpur
156 PUBLICATIONS **1,563** CITATIONS
SEE PROFILE

Indrajit Chakrabarti
Indian Institute of Technology Kharagpur
81 PUBLICATIONS **570** CITATIONS
SEE PROFILE

Network-on-Chip Architectures for Signal Processing and Error Control Coding Applications

N Prasad, *Graduate Student Member, IEEE*
Research Advisors: Prof. Santanu Chattopadhyay, *Senior Member, IEEE* and Prof. Indrajit Chakrabarti, *Member, IEEE*
Department of Electronics and Electrical Communication Engineering
Indian Institute of Technology Kharagpur, WB 721302, India
{nprasad,santanu,indrajit}@ece.iitkgp.ernet.in

***Abstract*—This work is based on the design and development of energy-efficient Network-on-Chip (NoC) based reconfigurable multi-core architectures for algorithms in the application areas of digital signal processing (DSP) and error control coding (ECC), such as fast Fourier transform (FFT) and Viterbi decoding (VD). Unlike previous approaches, the current work considers the graph representations of the above mentioned algorithms, such as signal flow graph (SFG) for FFT and trellis graph (TG) for VD, for mapping the applications onto the NoC. This aids in designing and synthesizing energy-efficient architectures for the same. In addition to this, a novel NoC topology, namely ZMesh, has also been proposed considering the constant geometry property of these algorithms, in order to design energy-efficient NoC architectures for the above mentioned algorithms.**

***Index Terms*—Constant geometry, fast Fourier transform, Network-on-Chip, Viterbi decoder, ZMesh.**

I. Introduction

With an increase in the global wiring density of a chip, efficient architectures that support faster communication between the processing cores in a Multi-Processor System-on-Chip (MPSoC) are being considered. In the process, the paradigm of Network-on-Chip (NoC) has emerged and is considered to be a promising solution for providing efficient communication between the processing cores in an MPSoC environment [1]. In designing multi-core architectures, Mesh based NoC topologies have been chosen as the most convenient ones due to their advantages, such as regularity. Increasing the buffer size is a method that has been generally followed to improve the performance of mesh based NoCs. Recently, to improve the performance of the mesh based regular NoC architectures, topologies with diagonal links, such as DMesh, X-Network and PDNoC, have been introduced. These topologies have shown improvement over mesh with large buffers both in terms of performance and power consumption.

On the other hand, few common properties of DSP and ECC algorithms, such as FFT and VD, are: they are highly parallel in nature, they can be represented using graphs like SFG and TG, and they become computationally intensive when the input size increases beyond moderate values. These properties facilitate implementation of the algorithms on an NoC based MPSoC platform. As algorithms with inherently high degree of parallelism can be distributed among multiple processors, graphs used to represent them can be considered as inputs in synthesizing the NoC topology.

II. Motivation

In designing NoC based architectures for FFT, many existing works have considered conventional FFT to map functions to cores on NoC. However, considering SFG of constant geometry FFT (CGFFT) for mapping FFT functions onto NoC has advantages, such as inter-PE communication for all stages becomes uniform, as the data flow pattern for all stages remains identical. This has not been explored so far. The present work extracts the advantage of this regularity property of CGFFT to implement a reconfigurable FFT architecture, with reduction in latency when mapped onto mesh based NoC.

In order to improve the performance of the considered algorithms in NoC based MPSoC systems, several novel NoC topologies, such as DMesh, X-Network, and PDNoC, have been proposed. These topologies have shown better performance metrics compared to the appropriate regular Mesh and CMesh topologies. All the mentioned topologies incorporate diagonal links, instead of huge buffers, to improve the performance. However, each of these topologies have their own disadvantages such as high radix routers, multiple routing algorithms, and poor performance for many of the traffic scenarios. Considering the above drawbacks and the algorithms to be mapped, this work aims in designing an energy-efficient NoC topology.

In many of the reported designs of NoC based architectures for VD, higher throughput values have been achieved either by improving the architecture of the sub-blocks used or by exploring the parallelism in the algorithm. However, realizing a multiprocessor architecture of VD by considering its TG has not been explored, which has advantages while mapping the algorithm to a multiprocessor platform. This work focuses on exploring this and implements an energy-efficient NoC based MPSoC architecture for the same.

III. Key Contributions of the Work

This section briefly highlights the contributions made while carrying out the present research work.

A. An Energy-efficient Constant Geometry FFT Architecture

This work reports the design and development of reconfigurable data parallel CGFFT architectures based on NoC paradigm [2], [3]. Twiddle factor multiplications have been realized using pipelined CORDIC rotators in order to ensure its

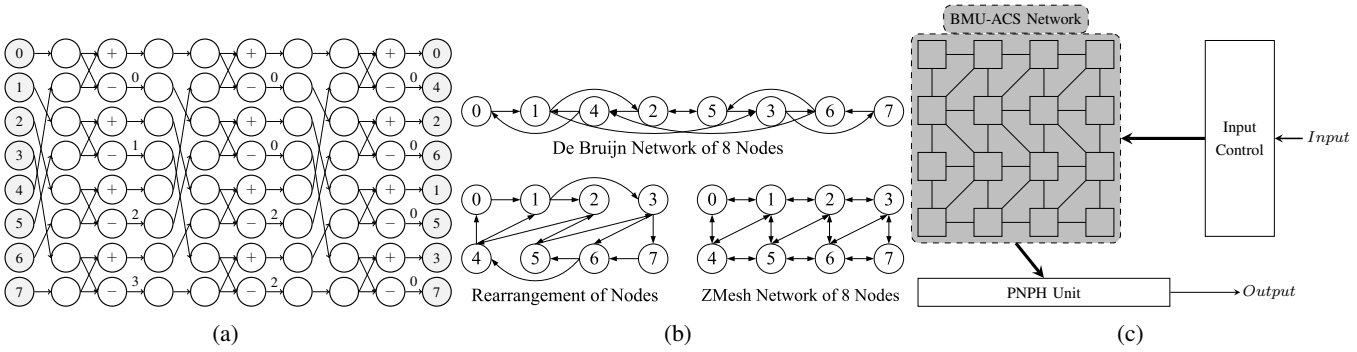

Fig. 1: (a) Proposed SFG of 8-point CGFFT. (b) DB network and its rearrangement to resemble a ZMesh. (c) Schematic of the proposed VD architecture.

high throughput. Mapping of FFT functions to cores has been done by considering the proposed SFG for CGFFT architecture (Fig. 1a), which helps in optimizing the design of network components (routers and network interfaces) and reducing the latency of FFT computation. The proposed input-size aware architecture can withstand faults in other processing elements (PEs) as it can accomplish the entire FFT computation using only one PE as well. When mapped onto mesh based NoC, the proposed architectures could achieve reduction in latency by 5×, compared to existing works. Hardware realization of the PE and the network components of the proposed architectures has been done using Xilinx Kintex-7 family FPGA device, as well as in ASIC design flow to obtain area and power results. The maximum operating frequency of a PE here meets the timing specifications of several application standards, such as DVB-T/H, DAB, 802.11a/n and UWB.

B. ZMesh: A Scalable and Energy-efficient NoC Topology

This work presents the design and evaluation of a scalable and energy-efficient Network-on-Chip (NoC) topology called ZMesh [4]. Diagonal links between the network nodes have been introduced such that they are better utilized for the applications under consideration. De Bruijn (DB) graph has been considered as the mother graph in synthesizing the proposed topology (Fig. 1b). A heuristic technique for mapping an application onto ZMesh has been proposed. Analysis of the ZMesh shows that it has better scalability than the regular Mesh topology. X-architecture layout style has been considered in implementing the proposed topology. Experimental evaluation has been carried out for ZMesh, and it has been compared with other state-of-the art topologies. ZMesh has an average improvement of 2.39× in energy consumption when compared to DMesh of similar size. It can also achieve an average improvement of 37.31% in terms of execution time, when compared to CMesh. For the class of applications with more uniform traffic, such as CG algorithms, ZMesh outperforms other considered topologies including PDNoC, in terms of energy efficiency.

C. An Energy-efficient Viterbi Decoder Architecture

This work proposes an energy-efficient NoC based architecture for realizing reconfigurable VD (Fig. 1c). The proposed architecture can support constraint lengths of 5, 7 and 9, and rates of 1/2-1/4. A modified Branch Metric Unit (BMU) with less memory requirement has been introduced. ZMesh topology has been considered for mapping the add compare select network (BMU-ACS) onto the NoC. Reconfigurable permutation networks path history (PNPH) units have been used that have the capability of being configured according to the varying constraint lengths of the Viterbi decoder. When mapped onto ZMesh, the proposed architecture can achieve reduction in energy consumption by an average of 4.39× that can be improved further for larger networks. The proposed design can achieve a maximum throughput of 20 Gbps, when run at 1.25 GHz. At its maximum frequency, the proposed design occupies an area of 3.914 mm^2 and consumes 1.54 W of power.

IV. Conclusions and Future Work

The work carried out so far in this research has proposed energy-efficient reconfigurable NoC based MPSoC architectures for DSP and ECC applications, such as FFT and VD. Graph representations of the algorithms, such as SFG and TG, have been considered in mapping the applications onto the NoC. To achieve improved energy efficiency, a novel NoC topology, called ZMesh, has also been proposed considering the CG data flow of the above mentioned algorithms. Since ZMesh inherently is a Mesh based topology, other applications can also be mapped onto it to achieve better energy efficiency. Future work aims on improving the Quality-of-Security Service (QoSS) metrics of the proposed designs to make them robust against the emerging hardware security issues.

References

[1] L. Benini and G. D. Micheli, "Networks on chips: a new soc paradigm," *Computer*, vol. 35, no. 1, pp. 70–78, Jan 2002.

[2] N. Prasad, I. Chakrabarti, and S. Chattopadhyay, "Noc based multiplier-less constant geometry fft architecture," in *Emerging Applications of Information Technology (EAIT), 2014 Fourth International Conference of*, Dec 2014, pp. 173–178.

[3] N. Prasad, S. Chattopadhyay, and I. Chakrabarti, "Reconfigurable data parallel constant geometry fast fourier transform architectures on network-on-chip," *Microprocessors and Microsystems*, vol. 39, no. 8, pp. 741–751, Nov 2015.

[4] N. Prasad, S. Chattopadhyay, and I. Chakrabarti, "Zmesh: An energy-efficient network-on-chip topology for constant-geometry algorithms," in *2015 IEEE International Symposium on Nanoelectronic and Information Systems*, Dec 2015, pp. 146–151.