Graph Model-Based Generative Layout Optimization for Heterogeneous SiC Multi-Chip Power Modules with Reduced and Balanced Parasitic Inductance

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***Abstract*—Multi-chip SiC power modules with integrated snubbers are promising for large-capacity converters with high speed and cost-efficiency. In the design stage, the parasitic inductance of module layout generally attracts the primary efforts of designers because of its severe impact on dynamic performance, e.g., voltage overshoot and transient current imbalance. However, due to the complexity of the heterogeneous layout, the solution space and development efficiency is always limited by the traditional manual design approach. Thus, this article proposes a generative method to optimize the layout autonomously. Firstly, a graph model is built to describe heterogeneous layouts with all interconnectivity and design constraints retained. Based on the model, integer programming is introduced to generate layout templates with variable geometric topologies. Then, coupled with a self-developed discrete extractor, the Pareto-front is obtained by genetic algorithm, providing a trade-off boundary for loop inductance and branch mismatch. The proposed method is systematic, flexible, and requires few designers' expertise. A 1200V/240A half-bridge module is designed and fabricated to validate its capability. The experimental results show that the loop inductance of 5.59 nH is achieved, and less than 5% of the transient current imbalance is realized under 6.2 A/ns TURN-ON in the rated condition.**

***Index Terms*—Graph theory, integer programming, layout, multichip modules, optimization methods, snubbers.**

I. Introduction

In recent years, the market expansion in electric vehicles and photovoltaics has been accelerating the substitution of silicon carbide (SiC) devices for traditional silicon devices in multi-chip power modules (MCPMs) to achieve more compact and efficient power conversions [1]. A key reason for this transition is attributed to the reduced switching time of SiC devices and the correspondingly higher switching frequency and lower losses [2]. However, the capability of SiC devices is always hindered by the parasitic inductance in module packages for two main reasons [3]–[5]. On the one hand, the inductance in the commutation loop coupled with the high *di/dt* of the SiC devices would introduce the voltage overshoot and oscillation during the switching transient [6], further affecting the electromagnetic compatibility (EMC) performance [7]. On the other hand, the unbalanced inductance among the branches of paralleled chips would lead to transient current imbalance [8]. The consequent mismatched losses and operating temperature would de-rate SiC devices in field applications [9].

To release the potential of SiC devices, innovative structures have been proposed for power modules to minimize and balance the parasitic inductance. These solutions include heterogeneous integration of snubber components [10]–[12], stacking multiple wiring layers [13]–[15], and flip-chip wire-bondless structures [16][17]. Among these techniques, heterogeneous integration of snubber capacitors is the most cost-efficient one thanks to its good compatibility with the conventional packaging technology, i.e., the single-layer direct bonded copper (DBC) substrate with wire-bonding interconnections. Since the embedded snubber can close the commutation loop in the substrate, several layout concepts are proposed as the references for designers, such as the symmetrical layout [18], double-end terminals [19], multi-loop design [20], and bonding wire compensation [21]. Moreover, considering that the integrated ceramic capacitors may encounter the reliability issue, continuous progress has been made on characterizing and improving this as in [11] and [22].

However, the module layout design is still a complicated work not only due to the high degree of design freedom but also due to its nonreusable nature for wide-range applications [23]. As a result, repetitive trials are unavoidable for variable design inputs on module rating, chip source, and substrate footprint. Designers need to keep exploring the solution space with the multiple evaluation tools [24][25]. This causes a limited solution space and a long development period that is hard to fulfill the cost and time-to-market requirements. Therefore, instead of proposing design concepts, this work discusses the design and optimization of the heterogeneous layouts in an

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TABLE I
COMPARISON AMONG STATE-OF-THE-ART WORKS ON MCPMS AUTOMATIC OPTIMIZATION

Work	Layout Generation		Performance Evaluation			Layout Optimization		
	Method	Features	Method	Parasitic Induct.	Thermal Param.	Objectives	Solver	Outcomes
Mandray et al. [26],2009	not included		Lumped thermal circuit	○	● $T_{j,max}$	min. EMC & T_j	Enumeration	2-D POF
Hingora et al. [27],2010	not included		Invoking 3rd party extractor	● L_{loop}	● $T_{j,max}$	min. $T_{j,max}$	Nonlinear programming	Sorted by $T_{i,max}$
Hammadi et al. [28],2011	Invoking 3rd party modeler	● ease of implement ○ template required	Invoking 3rd party extractor	● L_{loop}	● $T_{j,max}$	min. L_{loop}, $T_{j,max}$ & total mass	Nonlinear programming	Sorted by dimensions
Ning et al. [29],2013	Sequence pair & routing mesh	● template free ● geom. topology variable ○ DRC required	Discrete model (Magnetic vector potential)	● L_{loop}	○	max. fitness incl. L_{loop} & A_{DBC}	Evolution (GA)	Solution with the highest fit.
Ning et al. [30],2015	Element sequence model	● template free ● geom. topology variable ○ DRC required	Evaluated by path length & area	● L_{loop}	○	max. fitness incl. L_{loop} & A_{DBC}	Evolution (GA)	Solution with the highest fit.
Shook et al. [31],2013	Symbolic layout model	● quick definition ○ template required	Elec. micro-strip & lumped thermal circuit	● L_{loop}	● $T_{j,max}$	min. L_{loop}, R_{loop} & $T_{i,max}$	Evolution (NSGA-II)	3-D POF
Evans et al. [32],2019	Symbolic layout model	● quick definition ○ template required	Elec. response surface & lumped thermal circuit	● L_{loop}	● $\Delta T_{j\text{-}c}$	min. L_{loop} & $\Delta T_{j\text{-}c}$	Evolution (NSGA-II)	2-D POF
Razi et al. [33],2021	Corner stitch & constraint graph	● DRC clean ○ template required	Elec. PEEC & lumped thermal circuit	● L_{loop}	● $T_{j,max}$	min. L_{loop} & $\Delta T_{j\text{-}c}$	Evolution (NSGA-II) & Random.	2-D POF
This work	Block graph model	● DRC clean ● template free ● geom. topology variable	Full discrete model (Multi-port elec. & thermal PEEC)	● L_{loop} ● $L_{br.}$	● $R_{th,j\text{-}c}$	min L_{loop}, $\Delta L_{br.}$ & A_{DBC} with $\Delta T_{j\text{-}c}$, or min. L_{loop}, $\Delta L_{br.}$ & R_{th} for a footprint	Evolution (NSGA-II)	3-D POF

autonomous and generative way.

In recent years, there has been some research to approach the automatic design of power modules. They are respectively focusing on models and methods of layout generation, performance evaluation, and autonomous optimization. The state-of-the-art works evolving these techniques are detailly viewed and summarized in TABLE I.

The layout generation method determines the search space of the optimizer. Early work in [26] and [27] selects the layouts from a predefined library with limited options, leading to restricted solution space. By cooperating with the CAD software, the work in [28] realizes the layout optimization with the predefined template and sizing variables. But the search space is still limited by the input geometric topology of the template. The pioneering works in [29] and [30] realize the generation of different geometric topologies by procedural placement and routing process. In this method, the relative positions of the switches and terminals are described by sequences, and the traces are subsequently generated by randomizing the grid occupations, thus providing versatile candidates for the optimizer. However, due to the lack of interconnection and constraint information in layout representations, the method obtains a limited success rate and requires a tedious design rule check (DRC) process. As an improvement, the symbolic matrix in [31] and [32] saves the connected traces in the elements, thus alleviating the connectivity check process. Furthermore, the latest work from the same group in [33] realizes the constraint-aware layout generation by the corner stitch data structure with constraint graphs. However, the works in [31]–[33] still require the manual input of the layout templates.

The performance evaluation procedure takes the majority of the computation time, thus determining the efficiency of the optimizer. The works in [27] and [28] invoke the third-party tools, e.g., ANSYS and FastHenry, which generally require a long computation time due to the generalized meshing and solving strategies. To speed up the evaluation process, the works in [25], [30], and [31] employ simplified models to get the approximate solutions for electrical and thermal performance. However, the accuracy of the simplified models would be diluted when dealing with the mutual couplings among paralleled chips. Accordingly, the works in [29] and [33] develop built-in discrete extractors to handle this problem. Among the discrete models, the partial element equivalent circuit (PEEC) in [33] has the advantage of calculation speed thanks to its rectangular discretization strategy and the fast circuit solver. However, the existing PEEC methods mainly focus on extracting the single-port loop parasitics, and few works include the fast-solving strategy considering multi-port branch inductance. Moreover, there is lack of the discrete thermal model in layout optimization.

At last, considering the large search space of the problem, the heuristic solvers as genetic algorithm (GA) are dominant as [28]–[32]. However, the solution quality of GA is subject to objective functions. In [29] and [30], though the multiple objectives as footprint area and loop parasitics are involved, these objectives are degraded to a single cost function, resulting in a subjective solution. As an improvement, the works in [30]–[32] employ a series of optimal solutions, i.e., the Pareto-front (POF), to illustrate the trade-off boundary between conflicting objectives, thus providing flexible options for designers. But the existing works only optimize the loop inductance. There is

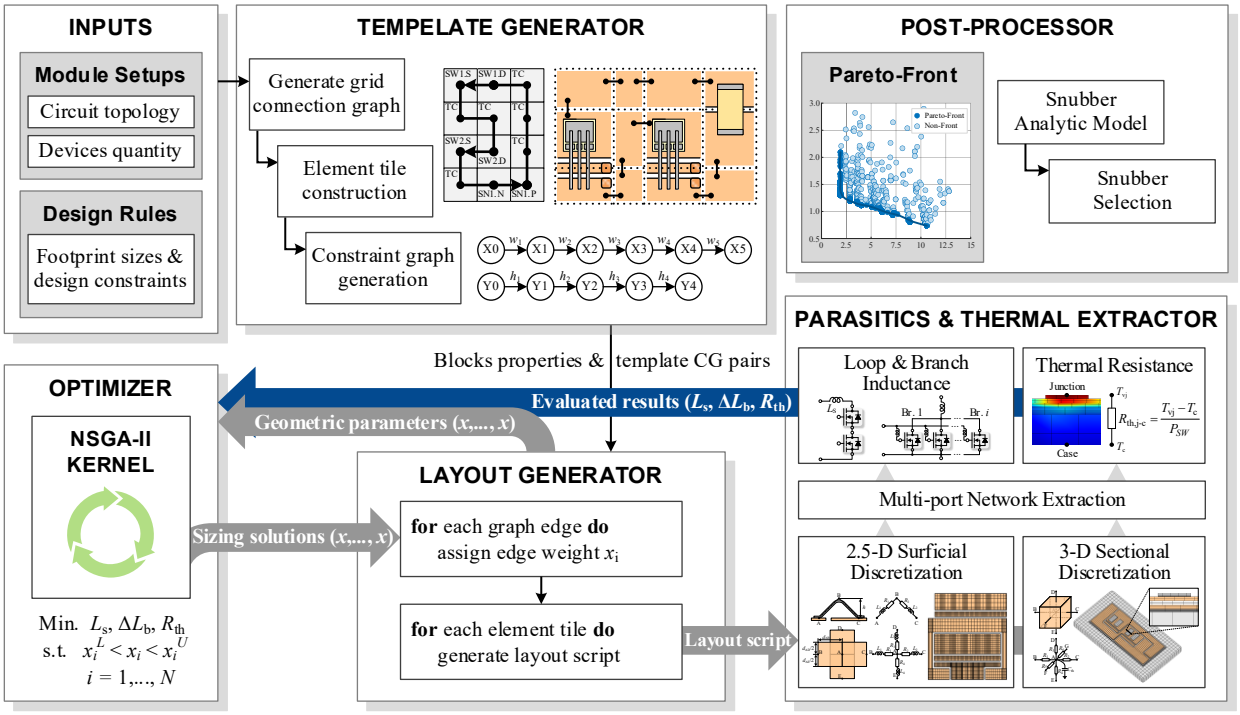


Fig. 1 Workflow of the proposed optimization method.

still a lack of an optimization method considering both the loop and branch inductance.

As the improvements of the authors' previous work in [34], and with the objective to reduce the loop inductance and branch mismatch among paralleled chips, the proposed MCPM layout optimization method for the first time combines the following:

1) A graph representation of heterogeneous layouts is proposed with all interconnection relationships and design constraints involved. The integer programming method and corresponding algorithms support the high-quality layout generation with variable geometric topologies and sizes, providing an extended search space for layout optimization.
2) A built-in discrete extractor is developed to evaluate both the electrical and thermal performance of the candidate layouts. The modified 2.5-D discrete strategy coupled with the multi-port solving process realizes the fast and accurate loop and branch inductance calculation.
3) The heterogeneous SiC MOSFET multi-chip layout prototype selected from the optimal boundary is fabricated and tested by comprehensive simulations on commercial software and hardware experiments. Thus, both the evaluation model and optimized solution are well-validated.

The rest of the article is arranged as follows. Section II overviews the workflow of the proposed method. Section III describes the graph-based layout representation and generation algorithms. Section IV and Section V provide the details about the discretization and solving strategies of the built-in evaluator. Section VI demonstrates the implementation results of the proposed method. In Section VII, simulations and experiments are conducted to verify the performance of the optimized results. Finally, Section VIII concludes the paper and describes future work.

II. Proposed Optimization Flow

The workflow of the proposed method is illustrated in Fig. 1. The optimization process is divided into three steps: constructing the layout templates from module setups, and then evolutionary extending and sizing the layout according to the evaluation results. As a result, the Pareto-front is provided, and heterogeneous components are selected according to the front solutions. The functions and features of each setup are explained as follows.

A. Template Generation

The layout template defines the relative position and interconnectivity of the module components, e.g., the semiconductor devices and passive snubbers. To handle the heterogeneous layouts, the template generator works on the block graph model as described in Section III-A, where blocks refer to the different substrate regions classified by components. According to the circuit topology in input, the generator would create the corresponding component blocks, and then solve the trace paths that connect these blocks in a grid graph. In the end, the solution graph is taken as the template for layout construction.

Multiple basic blocks are provided in Section III-A to support the layout setups with body-diode or Schottky barrier diodes (SBD), common-source or Kelvin sources, as well as traditional non-snubber configurations. Moreover, since the integer programming algorithm in the generator supports the multi-net pathfinding, the method is well compatible with different circuit topologies, as half-bridge, 3-level TNPC, etc. Further details of the block graph model and the generation algorithm are provided in Section III.

B. Evolutionary Layout Extension & Sizing Loop

After generating the template, the compliant layouts are iteratively optimized by the evolutionary optimizer, in which the block sizes are taken as the variables. Besides, considering the advantage of multi-loop design on inductance reduction, the template would also be shifted or mirrored to generate the multi-loop layout as in Section III-C. The elitist non-dominated sorting genetic algorithm (NSGA-II) kernel is employed to carry out the whole optimization process. Depending on the designers' requirements, the objectives are set to minimize the loop and branch inductance under multiple constraints as the manufacturing rules, module footprints, and thermal considerations. The branch inductance includes both the drain and source inductance among paralleled chips. By obtaining the maximum difference in two kinds of inductance, the worst situation for inductance mismatch is considered in the optimization process.

The built-in discrete extractors evaluate the candidate layouts during the optimization process. The extractors are built on the PEEC model in the electrical and thermal domain, which can well include the coupling effects. Aimed to balance the evaluation accuracy and efficiency, the modified discretization and solving strategies are employed and detailed in Section IV for the parasitic extractor and Section V for the thermal evaluator.

C. Post-Processing & Output

After iterative searching in the candidate layouts, the Pareto-front of solutions is provided as the trade-off boundary among objectives. The front treats the objectives with equal importance. Therefore, no designers' preference is engaged before the output. The snubber selection is also provided in this step by analysis model in [35], which closes the design loop for the heterogenous layouts.

The proposed method is systematic and flexible to different module setups. Since the inputs need only module setups as circuit topology, component quantities, and design rules, few designers' expertise is required to perform the optimization. Different design scenarios are implemented in Section VI, with validations provided in Section VII.

III. Graph-based Layout Generation

This section provides further details on layout generation: first, the layout representation, followed by the generation algorithm.

A. Block Graph Layout Representation

The layout representation model employed in this paper is demonstrated in Fig. 2. As in Fig. 2(a), the layout can be partitioned into different blocks according to the module components as devices, snubbers, and traces. Accordingly, the relative position of the components is described by a gird graph $\boldsymbol{G} = (\boldsymbol{N}, \boldsymbol{E})$ in Fig. 2(b), where the nodes $\boldsymbol{N}$ correspond to blocks and edges $\boldsymbol{E}$ to the interconnection relationships of their traces. Thus, the grid graph is taken as the layout template in the template generator. As for the block sizes, a pair of constraint graphs (CGs) in Fig. 2(c) is generated by scanning of the template grid, where the nodes strands for the vertical or horizontal scanlines, and the edge weights stand for the size of blocks in the row or column. The layout optimization loop takes the weights of the edges as the sizing handles.

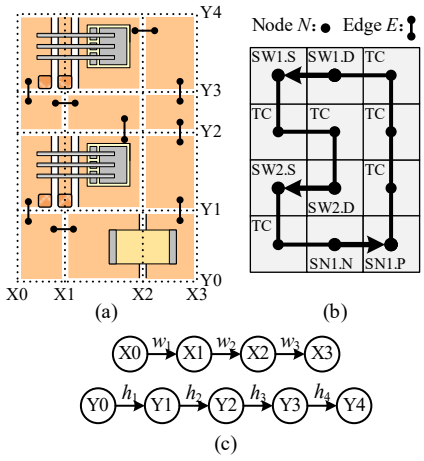


Fig. 2 Representation for an example layout: (a) block partition, (b) block graph model, and (c) constraint graph pairs of the blocks.

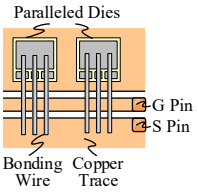
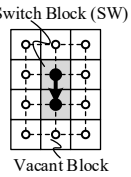
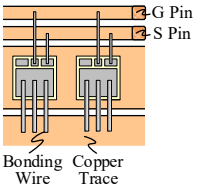
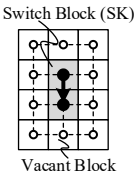
In the block graph model, the design rules are followed by a bottom-up mechanism. At first, the blocks are well defined by the constraints and variables according to the input manufacturing rules and components sizes. Then, the blocks in the same row or column of the template would be evaluated in CGs generation, where the maximum constraints among the blocks would be taken as the lower bound for the edge of CG. Moreover, if the module footprint is defined in the input, an additional edge would be created between the head and the tail nodes of CGs, which is treated as the summation bound for block sizes. With the assistance of this mechanism, the layout model includes both the interconnectivity and geometric rules, thus supporting the DRC-clean generation in the subsequent algorithms.

To work with different module configurations, multiple types of basic blocks are defined as follows.

1) Switch Blocks: The switch block contains the paralleled transistor chips that can form a switch in circuit topology, as well as the wires and traces for power and gate interconnections. Since the gate inductance has a minor influence on current imbalance than the power-related one [21], the gate traces are built with a predefined pattern in the block. By referring to the gate setups in mainstream power modules, two types of switch blocks are defined as in TABLE II.

In the common-source block, the gate traces are set beneath the power source wires, which would help to minimize the gate loop and thus the gate inductance. As for the power traces, since the power traces in this setup are able to connect adjacent blocks in three directions, the corresponding vacant edges are provided in the graph element as the path options for their nodes. In the block with Kelvin source, the drive traces are placed on the other side of the power source traces to decouple the power and gate paths. As a result, the node for the power drain trace loses the north edge in the graph elements. Besides, the chips in both setups are aligned in the drain trace to balance the inductance

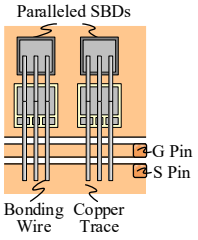
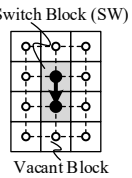
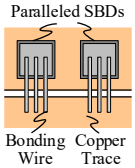
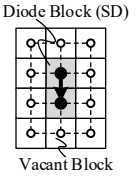
TABLE II
SWITCH BLOCK AND ITS GRAPH DEFINITIONS

Type	Block Geometry	Graph Element	Sizing Variables
Common source			Chip distance & trace size
Kelvin source			Chip distance & trace size

on bonding wires. The sizes of the power traces and the chip distance are taken as the variable for block sizing.

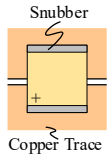
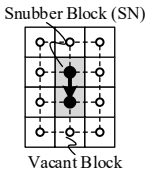
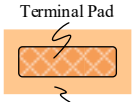
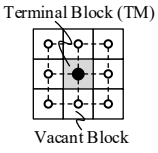
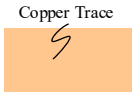
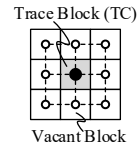
2) Diode Blocks: The Schottky barrier diodes (SBD) are recognized in industrial modules owing to their excellent reverse recovery performance. Therefore, two kinds of diode blocks are defined in TABLE III to support the SBD layout generation. As in TABLE III, the switch-based setup refers to the typical commercial modules in which the SBD chips are placed along with the transistors [36]. This setup would achieve a minimized block size and locally balance the parasitic inductance for both devices. The graph model for this block is identical to the transistor one, and it would directly replace the transistor block if enabled. On the other hand, the cell-based diode block only contains the SBD chips, which may occupy larger layout space but provide more freedom for layout generation. For instance, with a proper netlist setup, the separated diode block would support the P-cell and N-cell layouts with transistor block as in [37]. This layout concept may help to reduce the loop inductance. In the input, options would be provided for designers to choose whether to use SBD, and which type of SBD block is employed for layout generation.

TABLE III
DIODE BLOCK AND ITS GRAPH DEFINITIONS

Type	Block Geometry	Graph Element	Sizing Variables
Switch-based			Chip distance & trace size
Cell-based			Chip distance & trace size

3) Other Blocks: In addition, the blocks for snubber and power terminal components are defined as in TABLE IV. The power terminals refer to the module electrodes that conduct the power current from/to DBC, e.g., DC+, DC−, and AC terminals. Since the power terminals of the multi-chip module generally conduct high current and occupy large mounting areas on DBC, an independent block is built to model these regions. The trace block is defined to connect the component blocks according to the path solution as in Section III-B. Considering that the snubbers have two electrons, two nodes are set in its graph element for their traces. The terminal block and trace block only have one graph node.

TABLE IV
OTHER BLOCK AND ITS GRAPH DEFINITIONS

Type	Block Geometry	Graph Element	Sizing Variables
Snubber block			Trace length & width
Terminal block			Trace length & width
Trace block			Trace length & width

B. Integer Linear Programming-based Template Generation

In template generation, in order to generate diverse results, the graph elements of the switch and snubber blocks are randomly placed on a vacant grid at first. And the terminal blocks are optional to be placed randomly or in specific locations. At last, the nodes that belong to the same circuit net need to be connected by trace blocks, which is a multi-net pathfinding problem in the graph. This problem is solved by the integer linear programming model as follows, with an example in Fig. 3.

For each $net \in Netlist$, define the path options in the grid graph $\boldsymbol{G}$ as Boolean variables

$$x_{net_k} = \begin{cases} 1, \text{the path option } k \text{ for } net \text{ is used} \\ 0, \text{otherwise} \end{cases} \tag{1}$$

and their length $l_{net,k}$ as the integer variables. The objective of the ILP is set to minimize the total length of the commutation path as

$$\min. \sum_{net \in Netlist} l_{net_1} \cdot x_{net_1} + \ldots + l_{net_k} \cdot x_{net_k} \tag{2}$$

which subjects to two types of constraints: first, each net must select one single path as

$$\text{s.t. } x_{net_1} + \ldots + x_{net_k} = 1, \forall net \in Netlist \tag{3}$$

and second, each node in graph $\boldsymbol{G}$ obtains one path at most, as

$$\text{s.t.} \sum_{net \in Netlist} x_{net_1} + \ldots + x_{net_k} \le 1, \quad \forall net_k \text{ that use the node at } \boldsymbol{G}(i,j), \quad 0 \le i \le W-1, 0 \le j \le H-1. \tag{4}$$

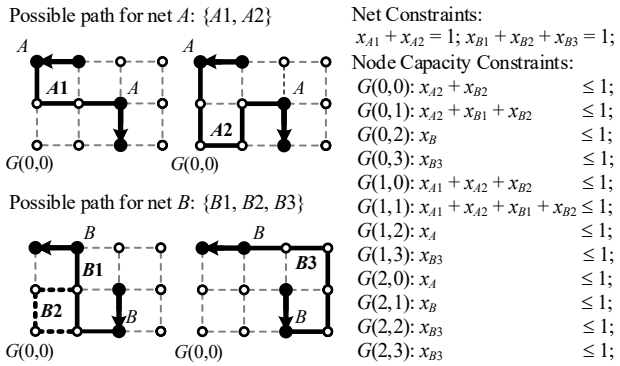


Fig. 3 Integer linear programming model for all-net pathfinding.

The pseudocode for template generation is illustrated in Algorithm 1. At first, a blocklist is created according to the netlist components, and the design constraints are simultaneously initialized as the block properties. Afterward, a grid graph is created with each block element placed randomly. To form a minimized commutation loop, the path options for each net are found by the depth-first traversal algorithm [38], and then the ILP model is solved. Once the path solution for all nets is found, a template is generated after excluding the empty nodes and creating CGs.

Algorithm 1 Template Generation

input: *Nelist*, *Constraints*
output: *Blocklist*, *TemplateGraph, ConstraintGraphs*

Create *Blocklist* for all components in the *Netlist*
Create an empty *TemplateGraph*
for *each block* in the *Blocklist* **do**
  Place block element by input or randomly
for *each net* in the *Netlist* **do**
  PathOptions = list of commutation path by depth-first traversal
  for *each path* in the *PathOptions* **do**
    Generate Boolean variables $x_{net,k}$ and length variables $l_{net,k}$ for ILP solver
Find the optimal commutation path by ILP solver
for *each net* in the *Netlist* **do**
  Find shortest terminal paths by depth-first search
Create trace blocks by path and add to *Blocklist*
Exclude empty nodes and create *ConstraintGraphs*
return *Blocklist*, *TemplateGraph*, *ConstraintGraphs*

C. Layout Generation

According to the intermediate solutions of the optimizer, the template is modified by two operations in layout generation: parallel extension to generate the multi-loop layout and assign weights for layout sizing. According to the number of paralleled loops, the extension operation would modify the chip number in switch blocks and extend the template with its CGs by offsetting or mirroring transformation. At last, the original footprint constraints are added to the head and tail nodes of the new CGs. For demonstration, the mirror extension of the layout is illustrated in Fig. 4. The weights of mirrored edges are inherited from the original ones to control the quantity of the solution variables and obtain the symmetric layouts.

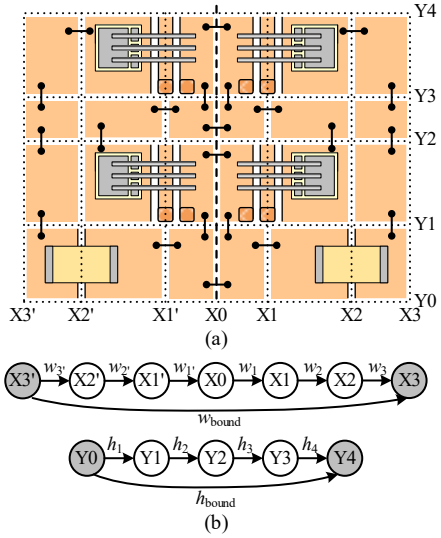


Fig. 4 Mirror extension of layout: (a) extended layouts, (b) extended constraint graph pairs.

After extending the template, the CGs are evaluated with sizing variables from the optimizer. In this operation, the block and footprint constraints are modeled as the lower and the summation bound, respectively. Afterward, the trace size and the component coordinate of every block are determined hierarchically. The pseudocode for layout generation is illustrated in Algorithm 2. Finally, the generated layouts are output in the structured script and transferred to the parasitics evaluator for inductance extraction.

Algorithm 2 Layout Generation

input: *Blocklist*, *TemplateGraph, ConstraintGraphs, SizingSolutions*
output: *LayoutScript*

Extend the *Blocklist* and *ConstraintGraphs* by *ExtensionVariables* in the *SizingSolutions*
for *each SizingVariables* in the *SizingSolutions* **do**
  Assign edge weights of *ConstraintGraphs*
for *each block* in the *Blocklist* **do**
  Assign traces sizes and components coordinates
for *each edge* in the *TemplateGraph* **do**
  Merge traces for edge-connected blocks
return convert *Blocklist* to *LayoutScript*

IV. Loop and Branch Inductance Evaluation Based on Discrete Circuit Method

Due to the prohibitive execution time of commercial tools, a discrete circuit-based build-in extractor is developed to evaluate the layout inductance. To increase the efficiency for loop and branch inductance, a 2.5-D discretization method and multi-

loop solving method are proposed considering the nature of multi-chip layouts.

A. 2.5-D Discretization Strategy

The layout substrate with the large-area copper traces and bonding wires is naturally a 2.5-D structure, where the current is distributed on the layout plane and uniaxially flows through the wires. Accordingly, the bonding wires are discretized by two cross filaments and traces by rectangle plane filaments, as shown in Fig. 5.

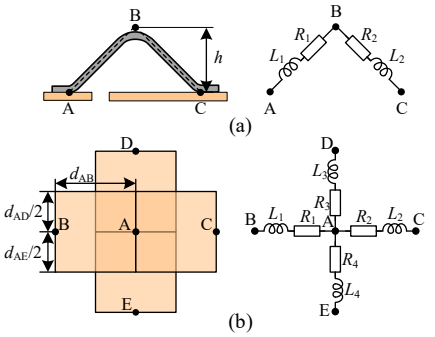


Fig. 5 Units for 2.5D discretization: (a) wire unit, (b) trace unit.

Furthermore, since the current distribution in traces is dominated by the skin effects and injection of bonding structures [39], a non-uniform discretion strategy is employed for traces as in Fig. 6.

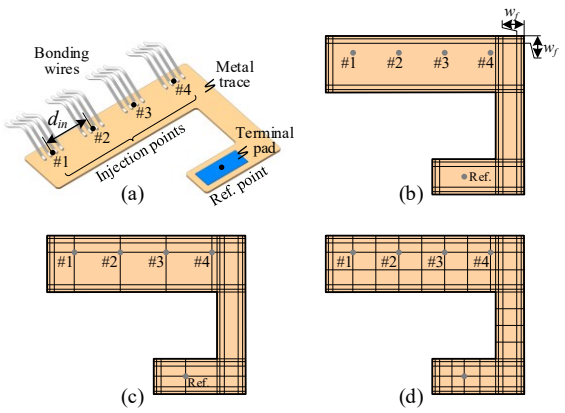


Fig. 6 Trace discretization process with current pre-calculation.

As in Fig. 6(b), the filaments are at first densified in the edge area within w_f to capture the skin current. The refinement is based on the exponential distribution of skin current as

$$J = J_s \exp\left(-\frac{x}{\delta}\right) \tag{5}$$

where J_s is the surface current density, x is the distance to the surface, and δ is the skin depth of the trace.

For a good approximation, filaments are set at the current density with 20% attenuation. The current density of the i filament is $J_i = (101\%-i\cdot 20\%)J_s$, $i\in[1,5]$. Thus the width of the edge filaments can be calculated by

$$d_i = \delta\left(\ln\frac{J_{i-1}}{J_S} - \ln\frac{J_i}{J_S}\right) \tag{6}$$

As for the off-edge area, the circuit nodes are initially set at the bonding point of wires and terminals as in Fig. 6(c). Then, the node positions in the rest of the area are determined by the maximum discretization distance d_{max} in Fig. 6(d), which is set as the 1/2 distance between the bonding point to model the potential difference between the bonding points.

B. Multi-port Fast Solving Method

Extraction of the loop and branch inductance employs the different excitation ports and chip status. For loop inductance, the excitation source needs to be placed between the snubber's DC+ and DC− ports, and with all semiconductor devices set at on-state to form the commutation loop. As for branch inductance, paralleled devices need to be set at off-state to apply the excitations on their electrodes. Accordingly, the different discrete circuits are formed for loop and branch extraction, which would result in a long computation time for inductance evaluation.

To alleviate this problem, a multi-port network model is employed here as the intermediary for two kinds of inductance. As an example, the multi-port model of a half-bridge module is illustrated in Fig. 7. By treating the chip electrons, e.g., D1*x*, S1*x*, D2*x*, and S2*x*, as net ports, the discrete circuit is firstly solved to extract the impedance matrix of the multi-port network. Then the loop and branch inductance are obtained by reduction of the matrix.

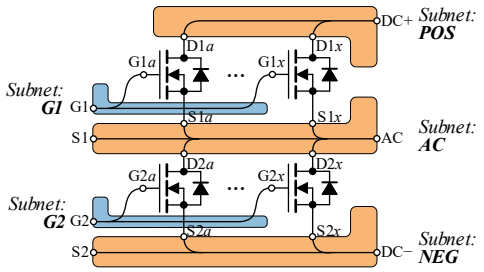


Fig. 7 Multi-port network model of a multichip half-bridge module.

Since the multi-port model keeps the discrete circuit constant, the solving process is conducted by single-time pre-decomposition of the discrete circuit [40], as

$$\begin{bmatrix} \boldsymbol{Z} & -\boldsymbol{A}^T \\ \boldsymbol{A} & \boldsymbol{0} \end{bmatrix} = \boldsymbol{L}\boldsymbol{U} \tag{7}$$

$$\boldsymbol{L}\boldsymbol{y} = \begin{bmatrix} \boldsymbol{0} & \boldsymbol{I}_S \end{bmatrix}^T \tag{8}$$

$$\boldsymbol{U}\begin{bmatrix} \boldsymbol{I}_b & \boldsymbol{V}_n \end{bmatrix}^T = \boldsymbol{y} \tag{9}$$

where the impedance matrix $\boldsymbol{Z}$ and incidence matrix $\boldsymbol{A}$ of the discrete circuit are firstly decomposed to the lower and upper triangle matrices $\boldsymbol{L}$ and $\boldsymbol{U}$. Thus, the unknown filament current $\boldsymbol{I}_b$ and node voltage $\boldsymbol{V}_n$ under source $\boldsymbol{I}_S$ can be quickly solved by $\boldsymbol{L}$ and $\boldsymbol{U}$ with an intermediate matrix $\boldsymbol{y}$. At last, the port impedance is deduced by the voltage response at the chip electrons under different port sources.

Based on the extracted multi-port model, the commutation loop inductance is obtained by solving the snubber's DC port response with the modified port status, in which the incidence matrix can be represented as

$$\boldsymbol{A}_m = \left[diag(\boldsymbol{A}_{POS}, \boldsymbol{A}_{AC}, \boldsymbol{A}_{NEG}) \;\vdots\; \boldsymbol{A}_{DS} \right] \tag{10}$$

where the left part is the incidence matrix of the power subnets, and the right part $\boldsymbol{A}_{\mathrm{DS}}$ describes the new branch introduced by semiconductor chips.

Similarly, the network impedance is modified with new elements as

$$\boldsymbol{Z}_{\mathrm{m}}=\left[\begin{array}{cccc:c} \boldsymbol{Z}_{\mathrm{D1}x} & \boldsymbol{Z}_{\mathrm{D1}x\text{-}\mathrm{S1}x} & \boldsymbol{Z}_{\mathrm{D1}x\text{-}\mathrm{D2}x} & \boldsymbol{Z}_{\mathrm{D1}x\text{-}\mathrm{S2}x} & \boldsymbol{0} \\ \boldsymbol{Z}_{\mathrm{S1}x\text{-}\mathrm{D1}x} & \boldsymbol{Z}_{\mathrm{S1}x} & \boldsymbol{Z}_{\mathrm{S1}x\text{-}\mathrm{D2}x} & \boldsymbol{Z}_{\mathrm{S1}x\text{-}\mathrm{S2}x} & \boldsymbol{0} \\ \boldsymbol{Z}_{\mathrm{D2}x\text{-}\mathrm{D1}x} & \boldsymbol{Z}_{\mathrm{D2}x\text{-}\mathrm{S1}x} & \boldsymbol{Z}_{\mathrm{D2}x} & \boldsymbol{Z}_{\mathrm{D2}x\text{-}\mathrm{S2}x} & \boldsymbol{0} \\ \boldsymbol{Z}_{\mathrm{S2}x\text{-}\mathrm{D1}x} & \boldsymbol{Z}_{\mathrm{S2}x\text{-}\mathrm{S1}x} & \boldsymbol{Z}_{\mathrm{S2}x\text{-}\mathrm{D2}x} & \boldsymbol{Z}_{\mathrm{S2}x} & \boldsymbol{0} \\ \hdashline \boldsymbol{0} & \boldsymbol{0} & \boldsymbol{0} & \boldsymbol{0} & \boldsymbol{0} \end{array}\right] \tag{11}$$

where the non-zero elements are the impedance at the chip electrons, and the other all-zero parts describe the chip connections.

Accordingly, the commutation inductance is calculated by solving the snubber port response V_{p} under the excitation current I_{p}, as

$$L_{\mathrm{loop}}=\frac{\mathrm{Im}(V_{\mathrm{p}}/I_{\mathrm{p}})}{2\pi f} \tag{12}$$

As for the branch inductance, the power port inductance of paralleled chips is considered and extracted from (11), with the upper chips as

$$\boldsymbol{L}_{\mathrm{D1}x}=\frac{\mathrm{Im}\left(diag\left(\boldsymbol{Z}_{\mathrm{D1}x}\right)\right)}{2\pi f} \tag{13}$$

$$\boldsymbol{L}_{\mathrm{S1}x}=\frac{\mathrm{Im}\left(diag\left(\boldsymbol{Z}_{\mathrm{S1}x}\right)\right)}{2\pi f} \tag{14}$$

Thus, the mismatch value is calculated by the maximum branch difference among the upper and lower chips, as

$$\Delta L_{\mathrm{br.}}=\max(\Delta L_{\mathrm{D1}x},\Delta L_{\mathrm{S1}x},\Delta L_{\mathrm{D2}x},\Delta L_{\mathrm{S2}x}) \tag{15}$$

This extraction process is based on a small-size multi-port matrix, thus requiring less computation time than repetitive solving the discrete circuits. The numerical results show that the calculation error of the method is less than 5%. And the calculation time is reduced by over 85% compared with the ANSYS Q3D software, making the method suitable for fast extraction of layout inductance.

V. Thermal Performance Evaluation Based on Discrete Circuit Method

Thanks to the similarity between the heat transfer and electricity conduction process [41], the discrete circuit model can be further expanded to the thermal domain for thermal resistance evaluation. This section presents the discretization and solving method of the thermal model. A 3-D discretization strategy is employed to capture the thermal coupling effects among paralleled chips.

A. 3-D Discretization Strategy

The heat flux in a power module is mainly generated in switching devices, then transferred through the solder and DBC layers, finally dissipated by the baseplate. This process consists of both the vertical conduction and lateral spreading effects [42], which is naturally a 3-D problem. Accordingly, cubic units in Fig. 8(a) are employed to discrete the structures on the heat path. Meanwhile, considering the multi-layer structure of the power module, a top-down discretization flow is employed, as in Fig. 8(b). In this flow, the top structures are firstly discretized. Then the meshes in the contact area are transferred to the bottom structure with the contact nodes set at temperature equivalent. This process helps generate a high-fidelity contact in both geometry and temperature field, which contributes to an accurate temperature distribution in the contact area. As for the structure internals, at least three layers of the cubes are generated in cross-sections as in Fig. 8(c), where the nodes in the middle layers would model the temperature gradient in the vertical direction.

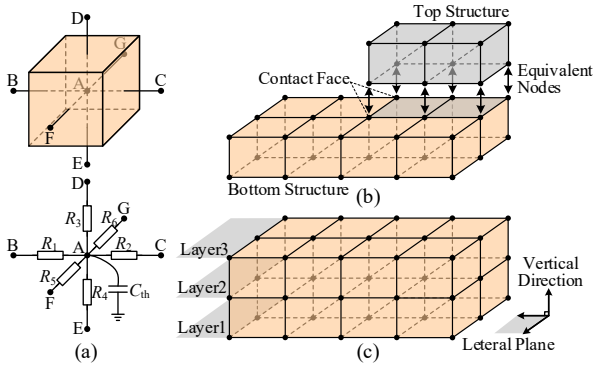


Fig. 8 Discretization strategy for the thermal model: (a) cubic discrete unit, (b) contact face processing, and (c) vertical layer processing.

B. Solving Method

The circuit components as the resistors and capacitors can be calculated by the cubic sizes and the material's thermal properties. Since this work focuses on steady-state analysis, only the thermal resistances between nodes are calculated.

The thermal evaluator employs the same solver as the electrical extractor in (7)–(9). According to the thermal resistance definition [43], a baseplate and the DBC solder are added beneath the DBC. And the bottom nodes of the baseplate are set at a fixed voltage for a constant case temperature. To solve the thermal resistance, the chip nodes in the switch are set as the excitation ports with current injections, i.e., heat generations.

Thus, the thermal resistance for the switch n is calculated as

$$R_{\mathrm{th}n,\mathrm{j\text{-}c}}=\frac{T_{jn,\max}-T_{\mathrm{c}}}{P_{\mathrm{tot},n}} \tag{16}$$

where the $T_{jn,\max}$ is the maximum node temperature in the junction of the chips, T_{c} is the case temperature set at the baseplate bottom nodes, and $P_{\mathrm{tot},n}$ is the total heat power applied on the chips.

As the evaluation result fed back to the optimization system, the thermal resistance of the module is obtained by the maximum value among all switches as

$$R_{\mathrm{th,j\text{-}c}}=\max\left\{R_{\mathrm{th}n,\mathrm{j\text{-}c}}\right\} \tag{17}$$

The above method supports the accurate and fast evaluation of the thermal resistance of the generated module. Since all paralleled chips contribute to the maximum temperature of the

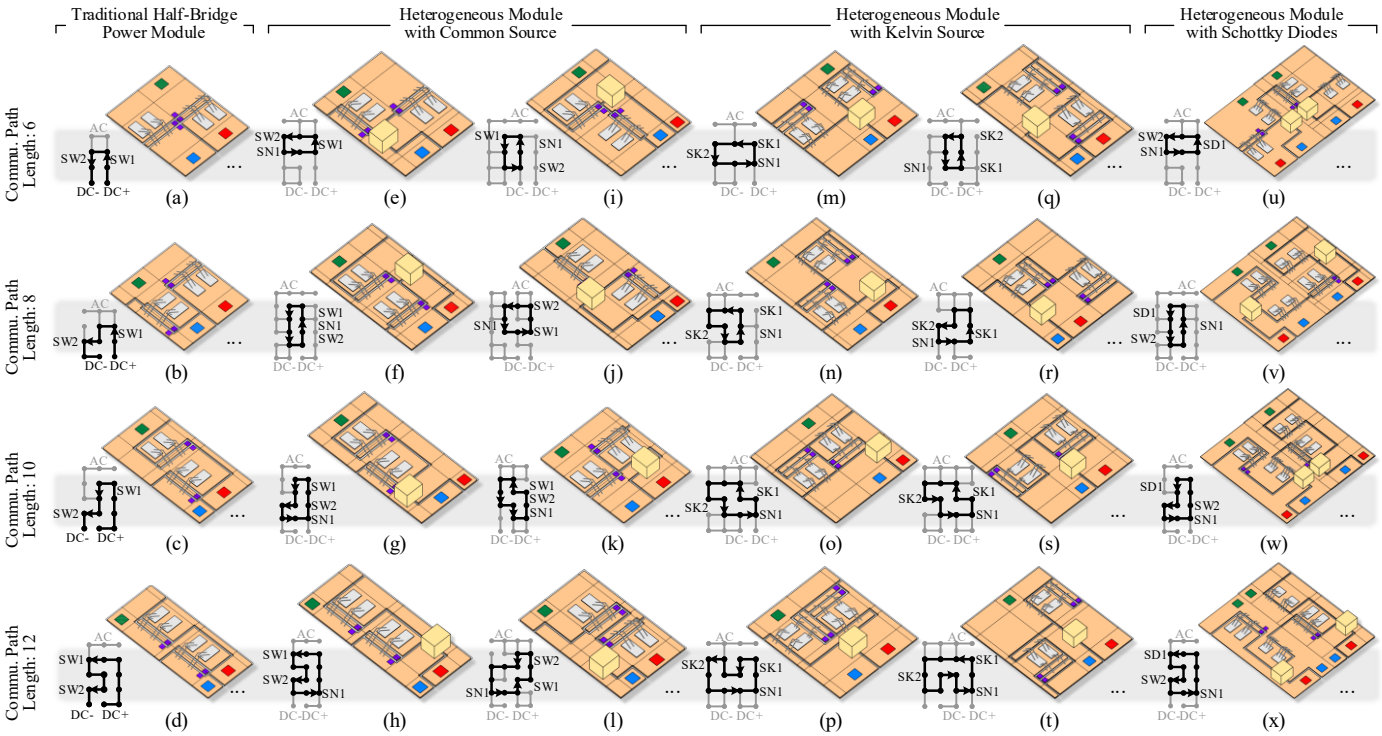


Fig. 9 Generated half-bridge templates and their minimum layouts under different configurations: (a)–(d) setups without heterogeneous components, (e)–(l) setups with snubbers and common-source connections, (m)–(t) setups with snubbers and Kelvin-source connections, and (u)–(x) setups with snubbers and Schottky diodes.

switch, the thermal resistance includes the thermal coupling among these chips. The numerical results show that the calculation error of the method is less than 3% compared with the ANSYS Thermal Tool, making it suitable to work with the optimization system.

VI. Implementation and Results

The overall optimization program has been implemented in MATLAB and is here tested on an Intel® Core™ i7-11700K CPU with 32 GB RAM. To show its potential, the half-bridge module with the system input in TABLE V is considered.

TABLE V
System Input of the Design Example

Category	Parameter	Unit	Value
Module setups	Circuit topology	-	Half-bridge
	Number of paralleled chips	-	4
	Chip size ($l \times w \times h$)	mm	5.90 × 3.10 × 0.25
	Snubber size ($l \times w \times h$)	mm	6.00 × 5.00 × 5.00
Design & manufacturing constraints	Terminal pad size	mm	≥ 3.00 × 3.00
	Trace width	mm	≥ 1.00
	Trace distance	mm	0.70
	Trace thickness	mm	0.30
	Wire height	mm	3.00
	Wire diameter	mm	0.36
	Wire distance	mm	1.20
	Bonding clearance	mm	≥ 1.00
	Soldering clearance	mm	≥ 1.00
	Soldering thickness	mm	(SAC305) 0.15
	Ceramic thickness	mm	(Al_2O_3) 0.38
	Baseplate thickness	mm	(Cu) 4.00

A. Template Generation

To demonstrate the method's capability to work with different configurations, four categories of templates are generated, with their grid graphs and the minimum-sized layouts (all design variables are set to the lower bond, and only two paralleled chips are included) depicted in Fig. 9.

In Fig. 9(a) to (d), the templates for standard half-bridge modules are generated, which include no heterogeneous components inside. This setup is implemented by removing the heterogeneous components from the netlist of the input circuit. By Line 1 in Algorithm 1, only the switch and terminal blocks are obtained for template generation. Then, the templates are obtained by solving the optimized paths for these blocks. This example demonstrates the method's capability to work with the non-snubber configurations.

As for the heterogeneous layout with integrated snubbers, the templates for the common-source setup are generated in Fig. 9(e) to (l), and those for the Kelvin-source configuration are in Fig. 9(m) to (t). The templates for the two setups are different because of their variant graph elements. These examples provide abundant templates for layout generation.

In Fig. 9(u) to (x), four heterogeneous templates with SBD are generated, in which the cell-based blocks are employed to form the P/N-cell configurations. In the generation process, the templates of the N-cell are firstly come out by Algorithm I. Then, the complementary P-cell are formed by mirroring the N-cell templates and transforming the switch blocks. This process generates symmetrical cell layouts and thus helps to obtain the balanced parasitic inductance for two cells. The above examples demonstrate the capability of the proposed method to work with SBD layouts.

In the above executions, the generation speed is 2 seconds per template. As for results, the generated templates for each configuration obtain different commutation paths in the grid

graph, which means the diversified geometric topologies of layout blocks.

B. Optimization Scenario 1: Design a Brand-New High-Density Power Module

In this scenario, a brand-new power module is designed for maximized layout density, where the baseplate and frames are flexible to accommodate the layout design. Accordingly, minimum-sized solutions are first generated by the input templates, and the rest of the candidates are generated by randomizing the chip distances, which would provide enlarged solution space. Both the thermal and electrical parameters would be evaluated, and the A_{DBC}–L_{loop}–$L_{br.}$ results would be offered to designers.

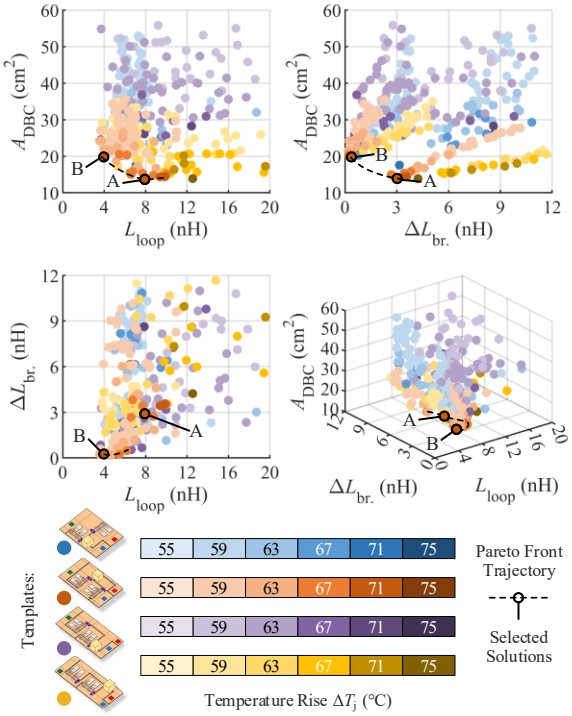


Fig. 10 A_{DBC}–L_{loop}–$L_{br.}$ solution space for the optimization Scenario 1. The temperature rises ΔT_j evaluated under the 300-W power dissipations. And the templates are from the generation results in Fig. 9(e) to (g).

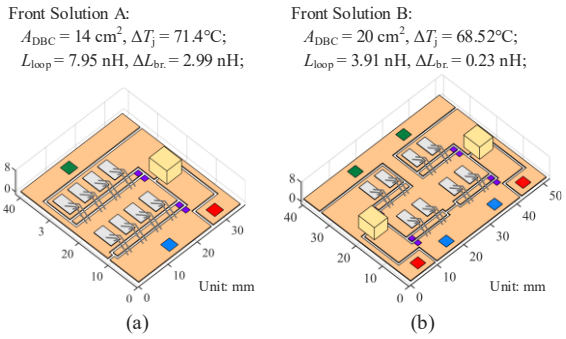


Fig. 11 Layouts and performance of the labeled front solutions in Fig. 10: (a) selected solution A, (b) selected solution B.

The templates with the common-source configuration in Fig. 9(e) to (g) are considered for demonstration. For each template, 80 candidates are generated, including the single-loop and extended layouts. The execution time for a candidate is less than one minute. The resulted solution space is depicted in Fig. 10. In this setup, the solutions from the template in Fig. 9(f) dominate the Pareto-front, which attribute to the paralleled arrangements of the upper and lower switches. Two front solutions are selected and depicted in Fig. 11. Compared with the candidates from other templates, they obtain the minimized DBC size with smaller temperature rises. Due to the single loop design in solution A, the substrate is more compact than the solution B. On the other hand, owing to the extended commutation loop in solution B, the loop inductance and branch mismatch are significantly reduced than solution A. Moreover, since the candidates are classified by thermal performance, different front solutions can be provided for designers according to their specified temperature rises.

C. Optimization Scenario 2: Design a Substrate to Fit the Existing Module Footprint

In this scenario, the layouts are designed and optimized under a given footprint. This is a realistic requirement from designers because it could save the costs of baseplate molding and corresponding fabrication fixtures. In the optimization process, thermal resistance is taken as the third criterion along with the loop and branch inductance. The chip distance is considered as a design variable to enlarge the search space. For demonstration, a footprint with 60.0×45.0 mm^2 is set in system input. And the templates from Fig. 9(e) to (h) are fed into the GA loop.

After a total of 900 populations evaluated in 30 iterations, the $R_{th,j\text{-}c}$–L_{loop}–$L_{br.}$ solution space is obtained as shown in Fig. 12. In this case, the template from Fig. 9(f) dominates the front solutions. To illustrate the results, two intermediate solutions from the template in Fig. 9(e) and (f) with a front solution are labeled and depicted in Fig. 13. According to the results, the template for solution A obtains excellent performance for thermal resistance and loop inductance. This is attributed to the vertical placements of the lower and upper switches. On the one hand, the switches obtain the minimized commutation loop, and on the other hand, the paralleled chips can be distributed placed along with the footprint edges. However, this configuration obtains the worst branch mismatch due to the enlarged branch paths. As for the intermediate solution B, due to the horizontal constraint of the footprint, only one loop is formed in its layout; thus, the advantage of the multi-loop design cannot be put to good use as in Section VI-B. Moreover, the footprint also limits the chip distribution, leading to low DBC utilization and small solution space, as in Fig. 12. In the end, thanks to the vertical placements of both the paralleled chips and switches, the template in Fig. 9(f) forms the dual-loop layouts as in Fig. 13(c). As a result, the thermal performance and the branch mismatch are improved by the symmetrical structure with a proper chip distance. And the loop inductance is reduced by the parallel of two commutation loops.

The above examples demonstrate the capability of the proposed method on layout optimization, where the diverse templates coupled with the layout extension method enlarges the design space and provides more flexibility and applicability for the generated layouts.

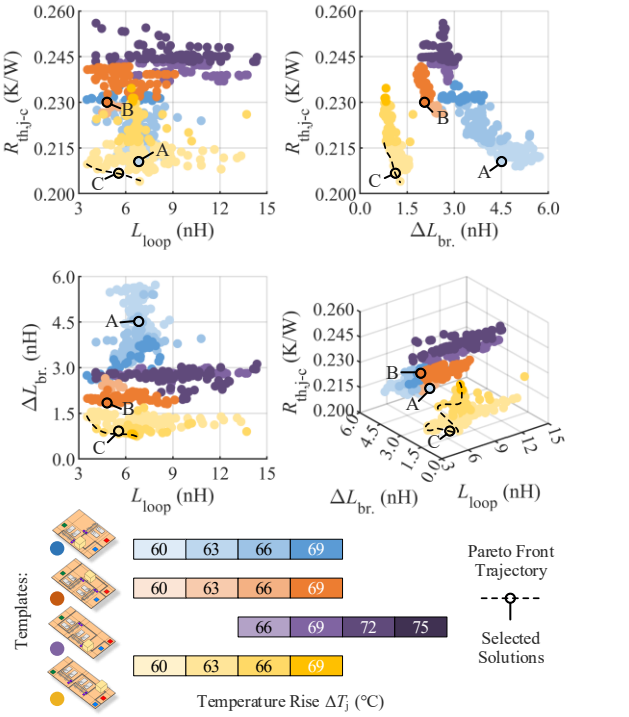


Fig. 12 $R_{th,j-c}$–L_{loop}–$L_{br.}$ solution space for the optimization Scenario 2. The temperature rises ΔT_j evaluated under the 300-W power dissipations. The templates are from the generation results in Fig. 9(e) to (h).

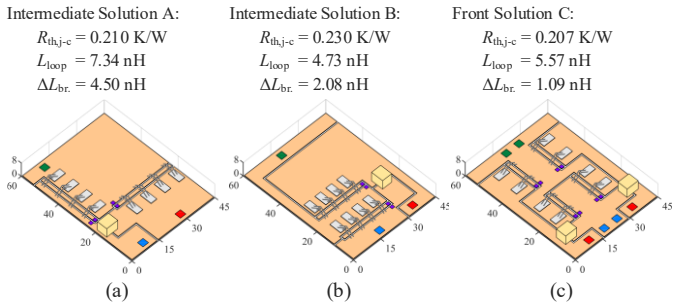


Fig. 13 Layouts and performance of the labeled solutions in Fig. 12: (a) intermediate solution A, (b) intermediate solution B, and (c) front solution C.

VII. Simulation and Experiment Verification

To validate the performance of the proposed methods, the parasitics and the switching performance of the solution in Fig. 13(c) are evaluated by both the simulation and hardware experiments.

A. Fabrication Setup

The bare dies of 1.2 kV SiC MOSFETs from CREE® (CPM2-1200-0040B, 40 mΩ, [44]) and the MLCC capacitors from TDK® are employed as the paralleled chips and the snubbers in the prototype. The sizes of dies and snubbers are identical to the component setups in TABLE V. The dies are selected from the same production batch to minimize the mismatches of the device parameters. The prototype uses the Al_2O_3 direct bond copper substrate and 380 μm aluminum bonding wires for power interconnection. As shown in Fig. 14, the size of the fabricated substrate is 60.0×45.0 mm. The current rating of the prototype is 240 A.

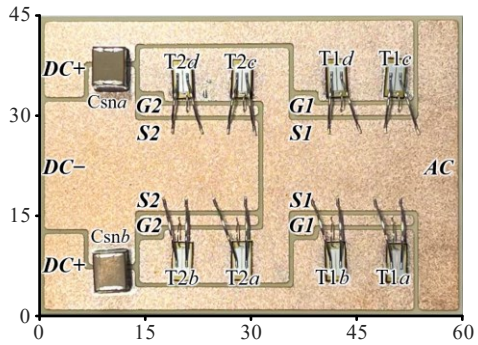


Fig. 14 Fabricated half-bridge substrate (60 mm × 45 mm).

B. Simulation Verifications

1) Thermal Evaluator: To verify the integrated thermal evaluator, the temperature distribution of the prototype is simulated by both the integrated evaluator and the ANSYS Thermal Tool. A 200-W heat flow is applied on the upper and lower switches in sequence, and the baseplate temperature is set at 25 °C. The evaluated results are depicted in Fig. 15. According to the results, the upper chips obtain a one-degree centigrade higher junction temperature than the lower chips due to the narrower mounting area. And the maximum junction temperatures evaluated by the integrated tool are 65.24 °C for the lower switch and 66.39 °C for the upper switch. These values obtained by ANSYS are 65.15 °C and 66.66 °C, respectively. Accordingly, the absolute error of the evaluated temperatures is less than 1 °C, which validates the accuracy of the integrated thermal evaluator.

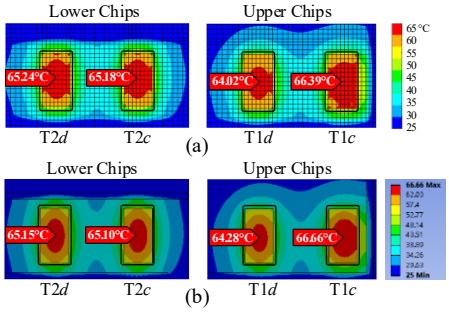


Fig. 15 Simulated temperature distribution among paralleled chips: (a) results by the integrated thermal evaluator, (b) results by the ANSYS software.

2) Parasitic Extractor: To verify the integrated parasitic extractor, the loop and branch inductance of the substrate is extracted by ANSYS Q3D software. The loop inductances extracted by Q3D is 5.61 nH at 10 MHz. Thus, the relative error of the results by the integrated extractor is less than 0.8%. The maximum difference among branch inductance calculated by Q3D is 1.14 nH. The relative error of the branch inductance results is 4.3%, showing a good accuracy of the integrated extractor.

3) Switching Performance: To evaluate the switching performance of the layout, a circuit-level simulation is performed in Cadence Pspice under the conditions in TABLE VI. The parasitics of the layout are extracted by Q3D and transferred to the multi-port module in Pspice. Consequently, the mutual inductance inside the substrate is modeled and

included in the simulation.

TABLE VI
SIMULATION CONDITIONS

Parameter	Value
DC voltage	450 V
Load current	240 A
Load inductance	180 μH
Gate voltage	+15/−3 V
Gate resistance	3 Ω
Device model	CREE Wolfspeed CPM2-1200-0040B

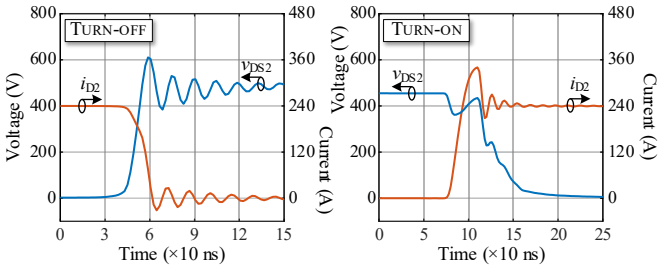


Fig. 16 Simulation waveform of drain-source voltage and drain current of the lower switch at switching transient: (a) TURN-OFF, (b) TURN-ON.

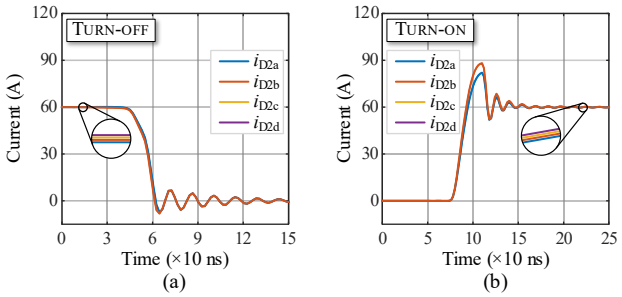


Fig. 17 Simulation waveform of drain current of lower chips at switching transient: (a) TURN-OFF, (b) TURN-ON.

The simulated drain-source voltage is depicted in Fig. 16. According to the results, the prototype obtains a low voltage overshoot of around 160 V and a mild oscillation at 56 MHz under 30 A/ns TURN-OFF. The simulated dynamic current of paralleled chips is shown in Fig. 17. Thanks to the symmetrical design, the devices in symmetric positions obtain an identical current distribution as T2*a*-T2*c* and T2*b*-T2*d*. As a result, the imbalance current occurs on the device T2*a* and T2*b*, where T2*b* obtains a faster switching speed due to the smaller loop than T2*a*. According to the simulation results, the maximum current mismatch among paralleled devices is 6.0 A (3.6% of the average) during the TURN-ON process, suggesting a balanced switching performance of the prototype.

C. Experiment Verifications

1) Thermal Performance: To verify the thermal performance of the prototype, a test setup with heat power control and infrared (IR) measurement is built, as in Fig. 18(a). The dissipated power of the switches in the prototype is controlled by the ITECH 220 A current source. And the temperature of the baseplate bottom is kept at 25 °C by the Julabo CF41 circulator system. The infrared measurement employs the Fluke Ti450 IR camera with 640×480 resolution. In the test, two sets of experiments are conducted with 200-W heat power applied on the upper and the lower chips, respectively, which is the same condition as the simulations. The IR images in Fig. 18(b) depict the detailed temperature distribution in heat source areas. Considering the accuracy of the IR camera is ±2 °C, the maximum temperatures for both switches correspond well to the simulation results, thus validating the thermal performance of the prototype.

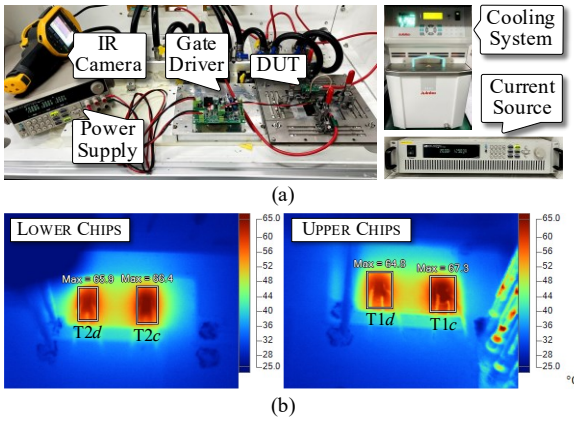


Fig. 18 Experimental validation on thermal performance of the prototype: (a) platform setup, (b) measured temperature distribution.

2) Parasitics and Switching Performance: To validate the fabrication precision of the substrate prototype, the loop inductance of a chip-less substrate is at first measured by the Keysight E4990A impedance analyzer as in Fig. 19. The measurement result at 10 MHz is 5.59 nH, and the relative error of the results by Q3D is 0.36%, showing a good fabrication precision.

Fig. 19 Measurement of the layout inductance: (a) test setup, (b) test kit.

A double pulse test bench is then built up to validate the switching performance. As shown in Fig. 20(a), the voltage sensors employ the high voltage differential probes with 100 MHz bandwidth, and the current sensors are Rogowski coils from PEM with 30 MHz bandwidth. The oscilloscope is Lecroy HDO6054A with 500 MHz bandwidth. To access the terminal pads and test points on DBC, a substrate tester with movable spring pins is developed as shown in Fig. 20(b). In the test, the lower switch acts as the device under test (DUT). Since the maximum current imbalance occurs on the devices T2*a* and T2*b*, the drain current of these two devices is measured to illustrate the current mismatch. The test points for drain-source voltage and device current are illustrated in Fig. 20(c). The substrate is immersed in silicon oil for electrical isolation.

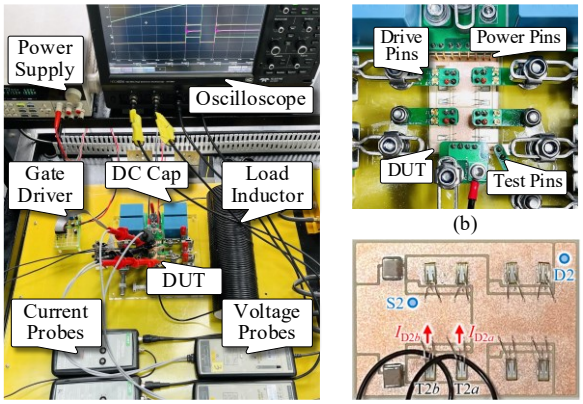


Fig. 20 Double pulse test setup for layout validation: (a) platform setup, (b) substrate tester setup, and (c) test points.

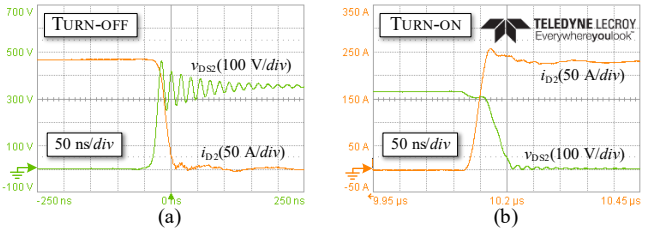


Fig. 21 Experimental waveform of drain-source voltage and drain current of the lower switch at switching transient: (a) TURN-OFF, (b) TURN-ON.

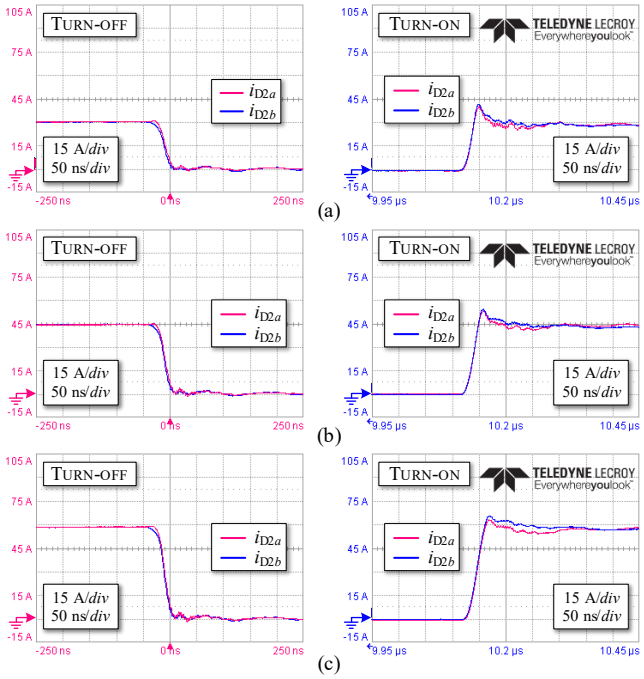


Fig. 22 Experimental waveform of drain current of lower chips T2*a* and T2*b* at switching transient: (a) I_{load} = 120 A, (b) I_{load} = 180 A, and (c) I_{load} = 240 A.

To comprehensively evaluate the switching performance of the prototype, a set of experiments are conducted when the bus voltage is 350 V, the gating resistance is 3 Ω, and the load current increases from 120 A to 240 A. The drain-source voltage and the total drain current of the devices in the lower switch are at first measured under load current of 240 A. According to the experimental waveform in Fig. 21, the drain-source voltage overshoot is 137.2 V, and the oscillation frequency is 55.3 MHz under 25 A/ns TURN-OFF, revealing a good match to the simulation results.

As for the current distribution, experiment waveforms of the drain current of the T2*a* and T2*b* are depicted in Fig. 22. The steady-state current mismatch is less than 1 A, revealing a good consistency of two current sensors. Furthermore, as shown in Fig. 22(a) to (c), with the load current increased from 120 A to 240 A, the switching speed of T2*b* is invariably faster than T2*a*, which corresponds well to the simulation results. Finally, the maximum transient current mismatch that occurs on the rated load condition is less than 5 A (3.3% of the average) under the TURN-ON speed of 6.3 A/ns, thus validating the current balance performance of the proposed method.

3) EMI Characteristics: Considering that the EMI issue is essential for high-speed SiC power modules, further experiments are conducted to illustrate the EMI characteristics of the generated prototype, where a commercial module from ROHM® (BSM400D12P3G002, 1200V/358A/10.5nH, [45]) is taken as the benchmark.

As the main EMI path in power modules [46], the middle-point to ground capacitor C_M is evaluated by the impedance analyzer. The measured C_M is 795 pF for the benchmark module and 585 pF for the prototype, revealing an approximate EMI path impedance for two modules.

As for the EMI sources, the spectra of the noise voltages and the near-field radiations are evaluated by the same setup in Fig. 20. The operation conditions are set as a standard PWM buck converter [46], where the DC voltage is 350 V, the load current is 120 A, and the duty cycle is 50% under 25 kHz switching frequency. In the experiments, the switching voltage of the lower devices is taken as a noise source and measured by high voltage differential probes with 100 MHz bandwidth. Meanwhile, the near-field radiations are measured by the near-field probes from ETS-Lindgren with 790 MHz bandwidth. The evaluated spectra are depicted in Fig. 23. According to the results, the benchmark module obtains an oscillation peak at 32 MHz, which corresponds well to the resonance frequency of the commutation loop. Owing to the reduced loop inductance, the oscillation peak of the prototype moves to 55 MHz with lower magnitudes in both noise voltage and near-field radiations. Besides, the spectrum magnitudes on the rest of the frequencies are approximate for two modules. These results validate that the EMI noises of the generated layout are well compatible with the commercial SiC power module.

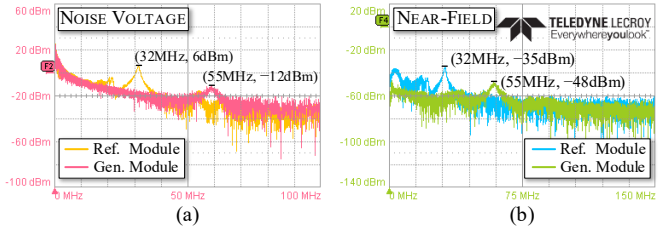


Fig. 23 Spectra of the measured EMI noises: (a) noise voltage, (b) near-field radiations.

VIII. Conclusion

This article proposes a systematic approach to optimize the heterogeneous SiC MOSFET multi-chip power modules in a generative and autonomous way. Specifically, by combining the template generation, inductance evaluation, and layout optimization, the method searches the optimized layouts with reduced loop and balanced branch inductance iteratively. For the first time, the graph-based method is introduced to model and generate the heterogeneous layout with variable geometric topologies. Moreover, the design constraints and connectivity information are well included in the generation process, thus improving the design quality. The proposed method is compatible with different module setups and fabrication constraints, thus requiring less expertise from designers. Promising results from both the simulations and hardware experiments validate its capability. In the design example, a commutation loop inductance of 5.59 nH is achieved, and the mismatch of branch inductance is less than 1.2 nH. The experiment results on the rated load condition show that the voltage overshoot is 137.2 V under 25 A/ns TURN-OFF, and the maximum transient current mismatch is less than 5 A (3.3% of the average) under 6.3 A/ns TURN-ON.

Since the design of power modules is a system engineering, there are limitations and prospects for future work to produce better solutions. The primary limitations include: 1) the generator is incompatible with the non-Manhattan layout; and 2) due to the lack of the semiconductor models, the impacts of the parasitic inductance on switching performance, e.g., current imbalance and oscillations, are not included in the optimizer, thus resulting in a posterior evaluation process. In the future work, aiming to complete the design flow, the chip planning and the vertical structure optimization methods with the power capacity evaluation will be investigated and integrated as a former process before the layout optimization.

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