Brac University

Department of Electrical & Electronic Engineering

Semester Summer-24

Course Number: EEE101L

Course Title: Electrical Circuits I Laboratory

Section: 06

Lab Report

Experiment no. 01

Name of the experiment: Verification of KVL and KCL (Software Simulation)

Prepared by:

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Group Number: **02**

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Electrical Circuits I Laboratory

EEE 101L

Department of Electrical & Electronic Engineering (EEE)

Brac University

Experiment No. 1

Verification of KVL and KCL

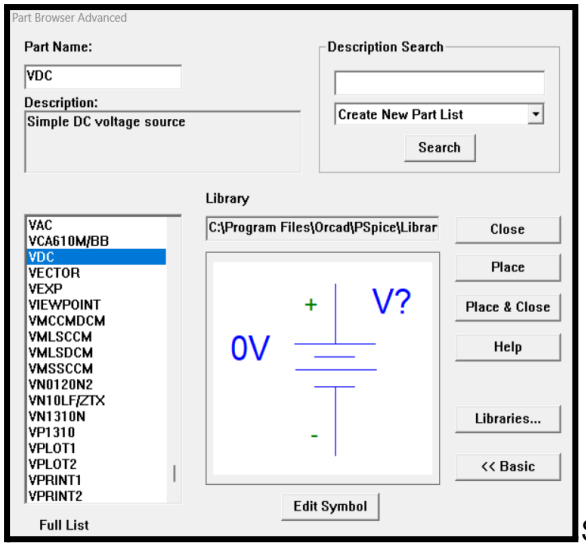
Part-A: Verification of KVL

1. **Objective:** This experiment is intended to verify Kirchhoff's voltage law (KVL) with the help of series circuits.

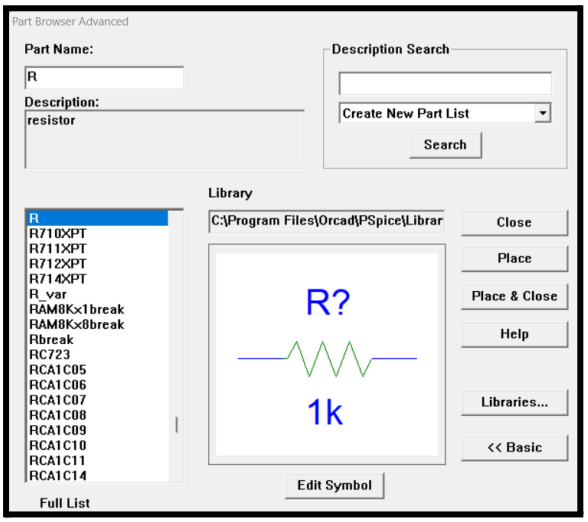
2. **Theoretical Background:** KVL states that around any closed circuit the algebraic sum of the voltage rises equals the algebraic sum of the voltage drops.

3. **Equipment:**

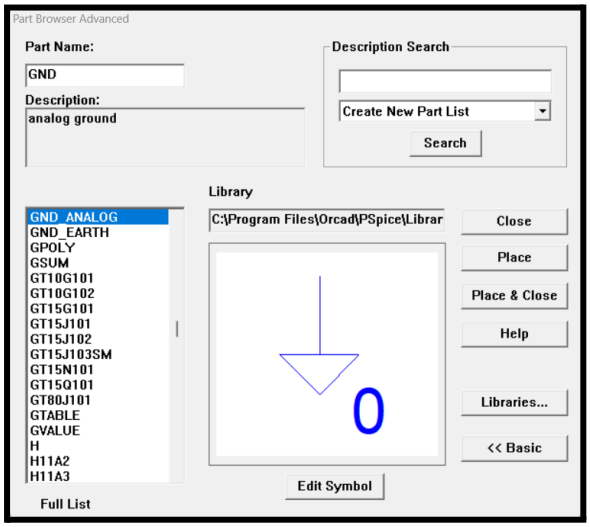
    - One multimeter
    - Three Resistors
    - One DC power supply



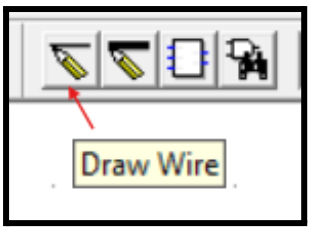
Selection of Voltage Source



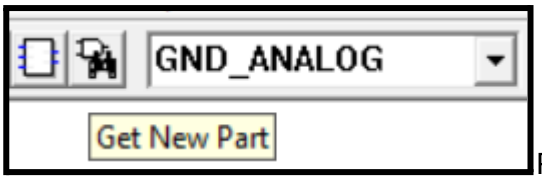
Selection of Resistor



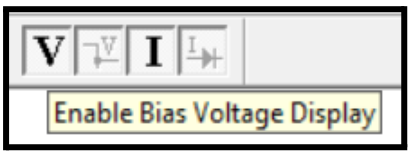
Selection of Ground



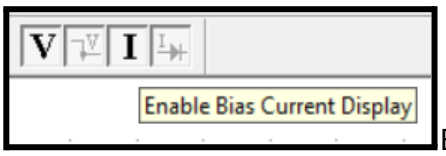
Wire tool



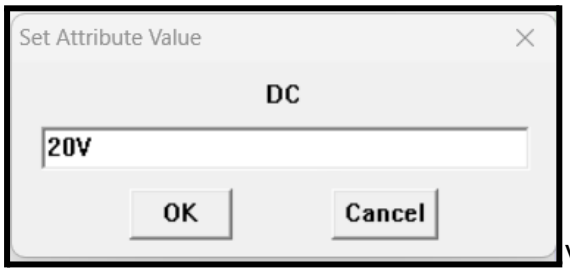
Parts menu



Bias Voltage



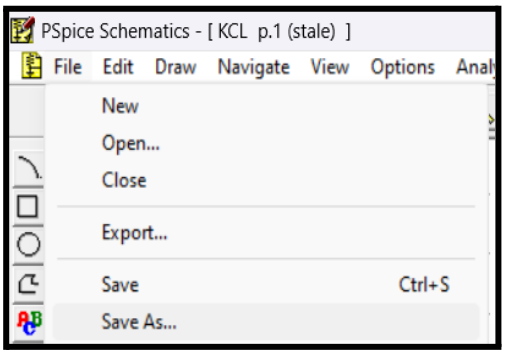
Bias Current



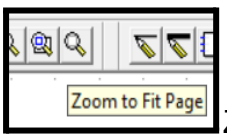
VDC Set (Voltage source value set)

Resistor set (R value set)

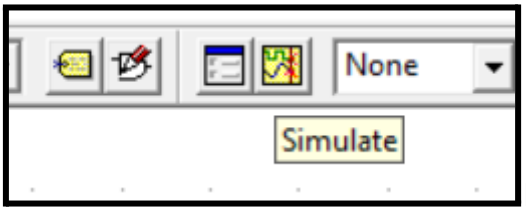
Text tools



File saving



Zoom



Begin Simulation

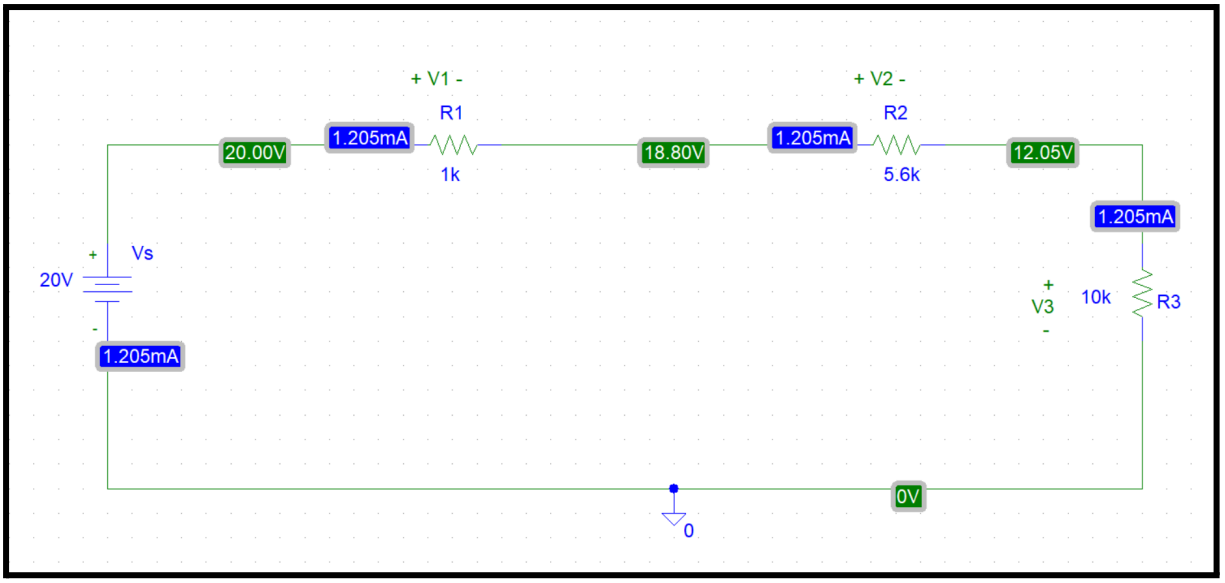


Figure: Verification of KVL simulated in PSpice Schematics

4. Circuit Diagram:

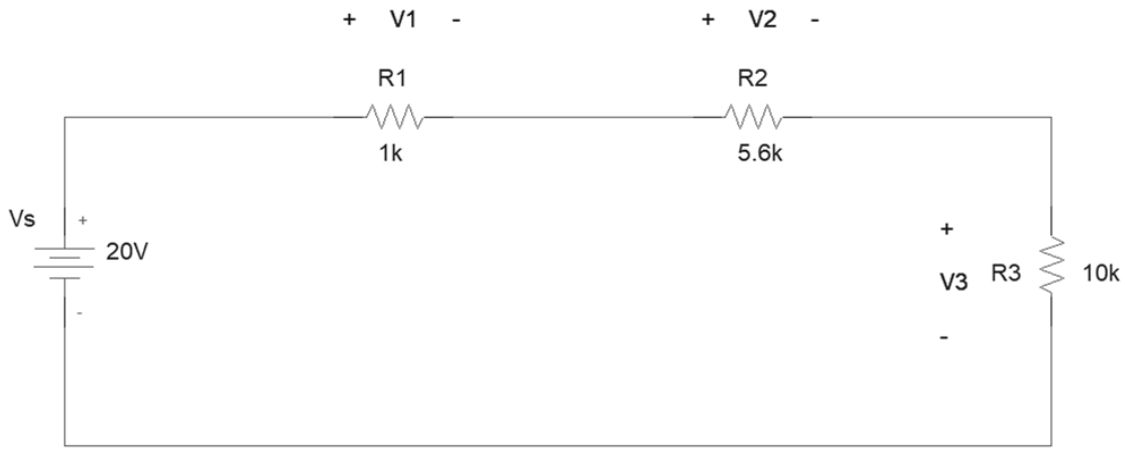


Fig. 1: Series circuit to demonstrate KVL

5. Procedure:

i. Connect the resistors R_1, R_2 and R_3 in series to a DC power supply as shown in Fig. 1.

ii. Take readings of V_1, V_2, V_3, V_s using a multimeter.

iii. Verify KVL as $V_S = V_1+V_2+V_3$.

6. Data Table:

Verification of KVL:

V_S (V)	V_1 (V)	V_2 (V)	V_3 (V)	$V_1+V_2+V_3$ (V)
20V	1.2	6.75	12.05	1.2+6.75+12.05 = 20

Faculty Signature and Date

7. Lab report directions:

1. State the rules of connecting voltmeter and ammeter in the circuit.
2. How do you calculate the power dissipation of a resistor?

Part-B: Verification of KCL

1. Objective: This experiment is intended to verify Kirchhoff's current law (KCL) with the help of a series-parallel circuit.

2. Theoretical Background: KCL states that the algebraic sum of the currents entering any node equals the sum of the currents leaving the node.

3. Equipment:

- Three resistors
- One multimeter
- One DC supply

4. Circuit Diagram:

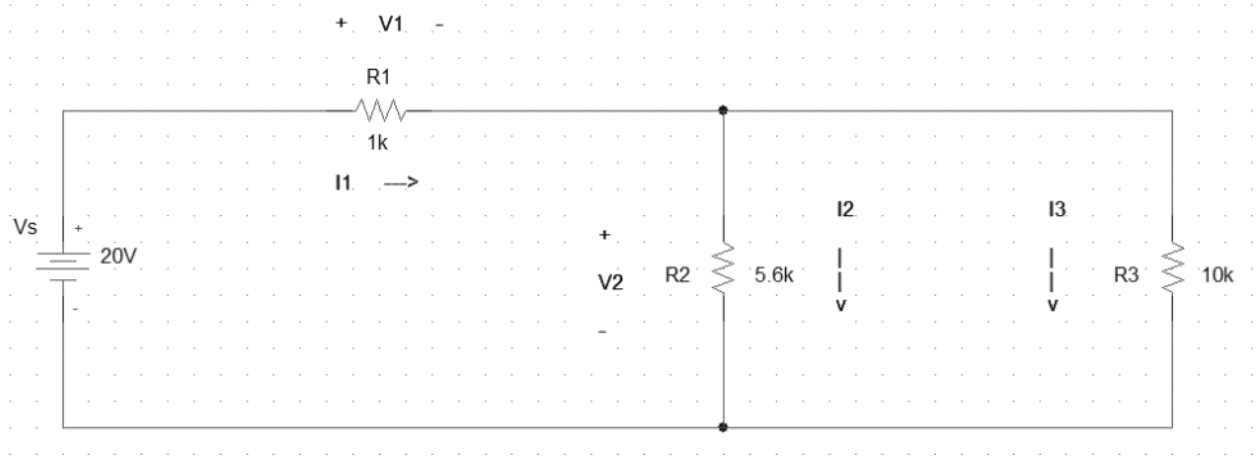


Fig. 2: Verification of KCL

5. Procedure:

i. Connect the resistors in series-parallel across the power supply as shown in Fig. 2.

ii. Measure the voltage drop across the resistors.

iii. Calculate the currents I_1, I_2 and I_3 by using $I_1 = V_1/R_1$, $I_2 = V_2/R_2$ and $I_3 = V_2/R_3$ as given above and prove that $I_1 = I_2+I_3$.

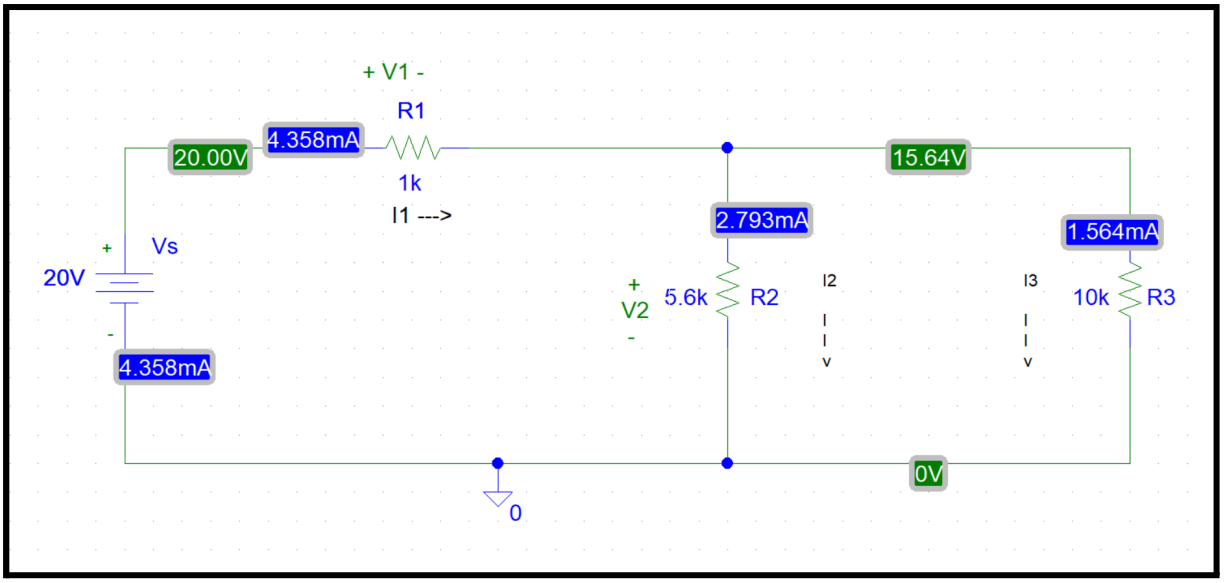


Figure: *Verification of KCL simulated in PSpice Schematics*

6. Data Table:

Verification of KCL:

R_1 (kΩ)	R_2 (kΩ)	R_3 (kΩ)	V_1 (V)	V_2 (V)	$I_1=V_1/R_1$ (mA)	$I_2=V_2/R_2$ (mA)	$I_3=V_2/R_3$ (mA)	I_2+I_3 (mA)
1	5.6	10	4.36	15.64	4.358	2.793	1.564	4.358

Faculty Signature and Date

7. Lab report directions:

1. Calculate the total power supplied by the source and power absorbed by each of the resistor.
2. Is the supplied power equal to total power absorbed?

Discussion of the software simulation

Equipments required:

1. PSpice Schematics software
2. Suitable device (PC or Laptop)

Simulation procedure:

Part-A: Verification of KVL

1. Open PSpice Schematics software.
2. Open the parts menu (click on the icon).
3. Search the necessary parts for the KVL experiment (VDC, GND, R).
4. Place the parts on designated places following the provided diagram and close the parts menu.
5. Using the wire tool connect all the parts in a series circuit.
6. Set the values of all the parts.
7. Rename all the parts for easier identification (VDC=Vs)
8. Use the Draw Text and Text Box tool to mark necessary information.
9. Enable Bias Voltage and Current display.
10. Use the zoom to fit page tool.
11. Save the file with a suitable name.
12. Begin circuit simulation.
13. Attach a screenshot of the circuit in the report document.
14. Fill out the data tables with necessary information and verify KVL using the given formula (Vs= V1+V2+V3).

Part-B: Verification of KCL

1. Open PSpice Schematics software.
2. Open the parts menu (click on the icon).
3. Search the necessary parts for the KCL experiment (VDC, GND, R).
4. Place the parts on designated places following the provided diagram and close the parts menu.
5. Using the wire tool connect all the parts in a series-parallel circuit.
6. Set the values of all the parts.
7. Rename all the parts for easier identification (VDC=Vs)
8. Use the Draw Text and Text Box tool to mark necessary information.
9. Enable Bias Voltage and Current display.
10. Use the zoom to fit page tool.
11. Save the file with a suitable name.
12. Begin circuit simulation.
13. Attach a screenshot of the circuit in the report document.
14. Fill out the data tables with necessary information and verify KCL using the given formula (I1=I2+I3).