# EEE205L

**Electronic Circuits I Laboratory**

# Lab Report

Section: 05

Group No:**04**

## Experiment no: 04 (Software)

Name of the experiment: *Investigation of Transfer and Output Characteristics of N-Channel Enhancement MOSFET (PSPICE Simulation)*


*Prepared by:*

**Name: Tanzeel Ahmed** **ID: 24321367** **Signature** *Tanzeel*

*All Group members:*

| Sl. | Name | ID | Signature |
|---|---|---|---|
| 1. | **Esrar Ul Hossain Rafin** | **24121187** | *Esrar* |
| 2. | **Tasmiya Tahsin Roza** | **24121339** | *Tasniya* |


Date of Submission: 26/08/2025

## Objective:

To investigate the transfer and output characteristics of an N-channel enhancement MOSFET in PSPICE.

## Theoretical Background:

A Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is a voltage-controlled semiconductor device used in both switching and amplification. In an enhancement-type N-channel MOSFET, no conductive channel exists at zero gate-source voltage (VGS). When VGS exceeds a certain threshold voltage (VTH), electrons are attracted towards the channel region, forming a conductive path between drain and source. The drain current (ID) increases with VGS beyond VTH in a nonlinear fashion. The transfer characteristics describe the relationship between VGS and ID at constant drain-source voltage (VDS), allowing determination of VTH. The output characteristics describe ID variation with VDS for fixed VGS. In the ohmic (linear) region, ID increases proportionally with VDS. Beyond pinch-off, the MOSFET enters the saturation region where ID remains nearly constant, making it useful for amplification. Understanding these characteristics is crucial for designing and biasing MOSFET circuits.

In modern circuit analysis, simulation is widely used to predict and study the behavior of electronic circuits before actual implementation. Simulation provides a time efficient way to test different circuit configurations and verify theoretical calculations.

PSPICE is one of the most commonly used circuit simulation tools. It allows users to design electronic circuits on a computer, apply test signals, and visualize the circuit response through graphs and plots. By simulating diode enhancement circuits in PSPICE, we can understand its characteristics without any kind of practical loss.

## Problem Statement-1:

To determine the transfer characteristics (VGS vs. ID) of an N-channel enhancement MOSFET at constant VDS = 20 V.

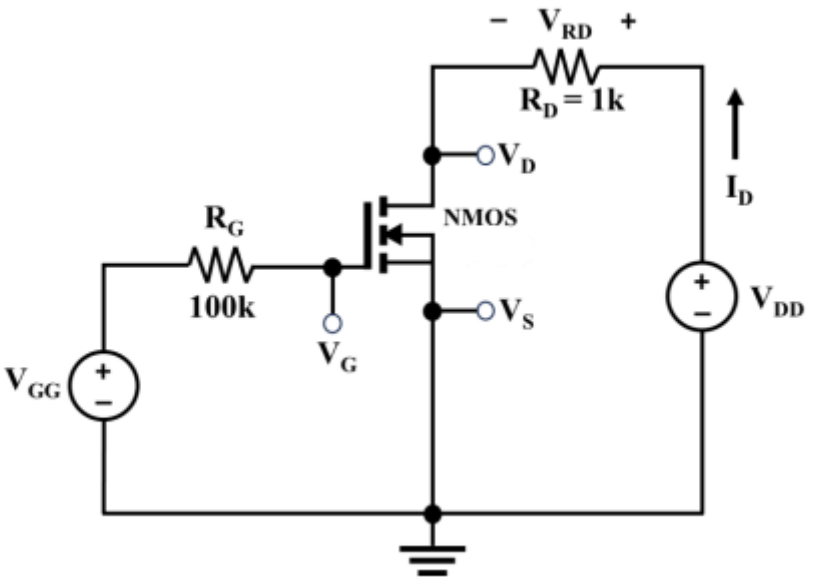
## List of equipments:

1. Suitable computer or laptop that meets the minimum requirements
2. ORCAD Pspice Schematics software

## List of equipments required in simulation:

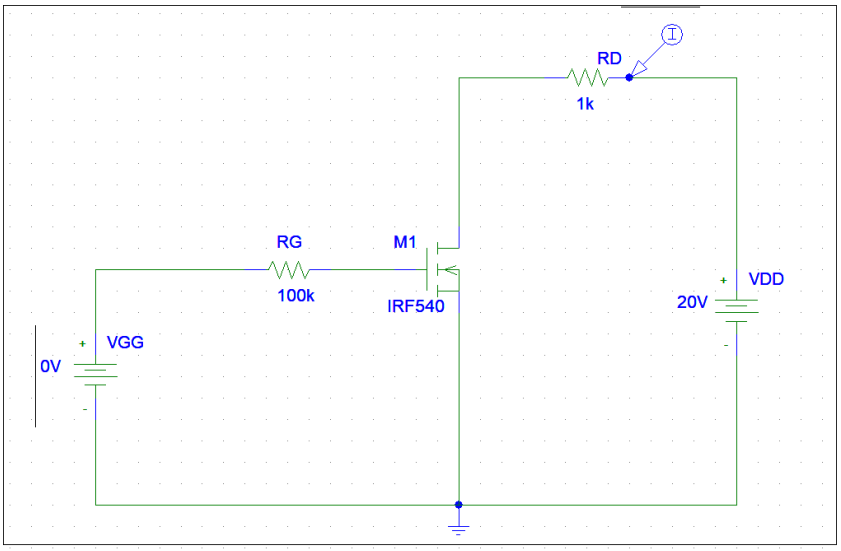
1. Resistor (R) - 1K-ohm - 1x, 100K-ohm - 1x
2. MOSFET IRF540 - 1x
3. DC Voltage source -2x
4. Current level markers

## Circuit diagram (from manual):




*Common source configuration of N-Channel MOSFET Circuit*

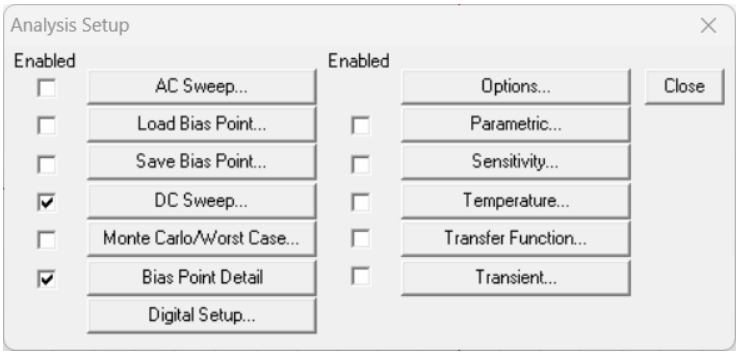
## PSPICE Schematic diagram:



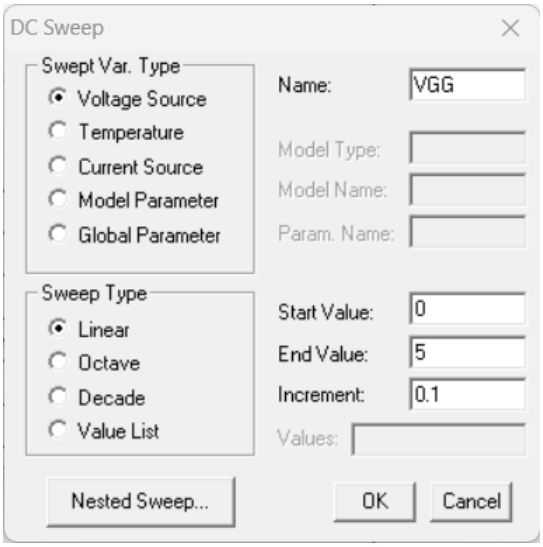

*Common source configuration in simulation*

# PSPICE Simulation settings:

## Analysis setup menu:

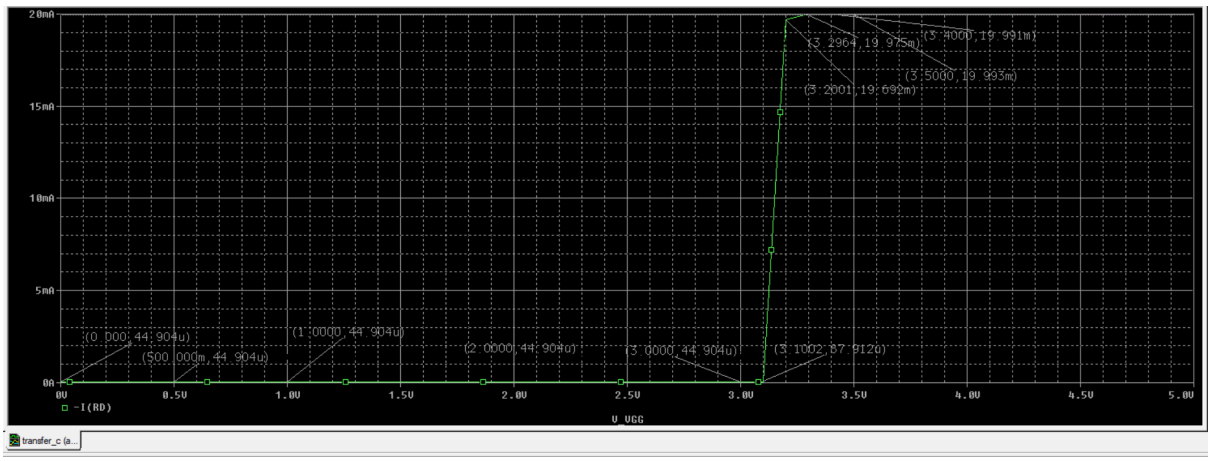



## DC Sweep:




*Name: VGG, Start value: 0, End value: 5, Increment: 0.1*

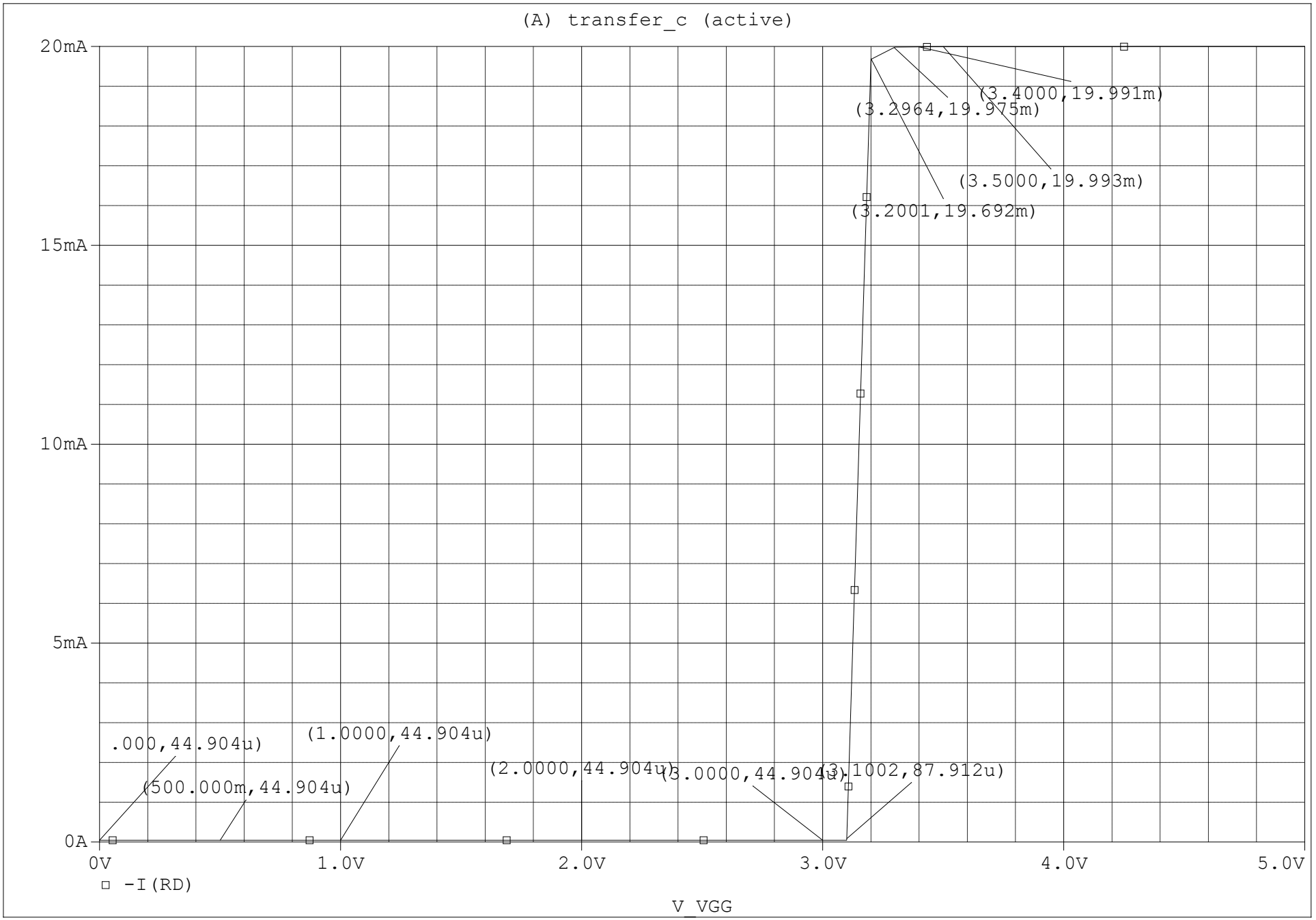
# Output waveforms:




*Transfer characteristics simulation plot*

* D:\BracU\5. Fifth Semester (SU-25)\EEE205L\SW EXP\ex4\transfer_c.sch

Date/Time run: 08/24/25 19:51:44 Temperature: 27.0



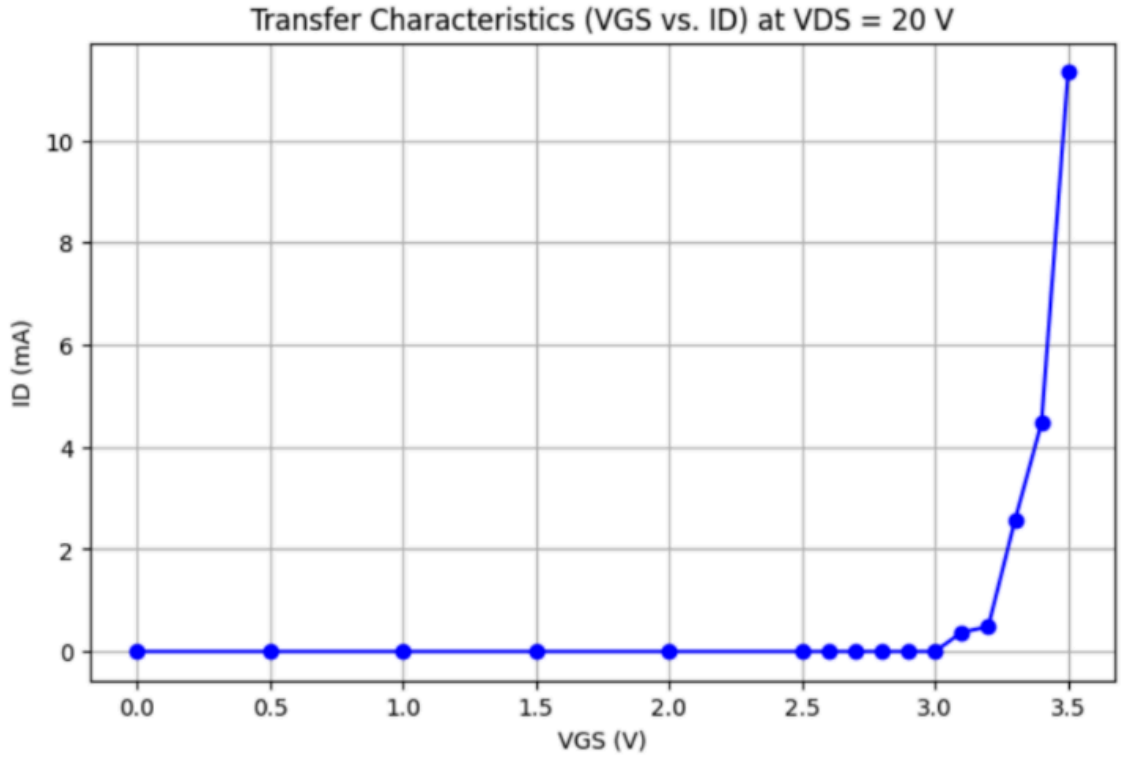
Explanation: The transfer characteristics graph shows the relationship between the gate voltage and the drain current of the transistor. At lower gate voltages, the drain current stays very small in the microampere range, which represents the cut-off region of operation. Once the gate voltage crosses a threshold of around 3.1 V, the drain current increases sharply, reaching nearly 20 mA, which indicates the transistor has entered its active or saturation region. This curve highlights how the input gate voltage effectively controls the output current, demonstrating the transistor's switching behavior.

## Data table (Simulated):

| VGS (V) | $I_D$ |
|---|---|
| 0 | 44.904uA |
| 0.5 | 44.904uA |
| 1 | 44.904uA |
| 2 | 44.904uA |
| 3 | 44.904uA |
| 3.1 | 87.912uA |
| 3.2 | 19.692mA |
| 3.3 | 19.975mA |
| 3.4 | 19.991mA |
| 3.5 | 19.993mA |

## Data table and graph (From hardware experiment):

| $V_{GS}$ (V) | $V_{RD}$ (V) | $I_D = \frac{V_{RD}}{R_d}$ (mA) |
|---|---|---|
| 0 | 0 | 0 |
| 0.5 | 0 | 0 |
| 1.0 | 0 | 0 |
| 1.5 | 0 | 0 |
| 2.0 | 0 | 0 |
| 2.5 | 0 | 0 |
| 2.6 | 0 | 0 |
| 2.7 | 0 | 0 |
| 2.8 | 0 | 0 |
| 2.9 | 0 | 0 |
| 3.0 | 0 | 0 |
| 3.1 | 0.37 | 0.374 |
| 3.2 | 0.48 | 0.485 |
| 3.3 | 2.53 | 2.56 |
| 3.4 | 4.42 | 4.47 |
| 3.5 | 11.23 | 11.34 |




## Comparison:

Simulated activation voltage 3.1V = 87.912uA
Hardware activation voltage 3.1V = 0.347mA
Difference = (0.347mA - 87.912uA) = 0.259mA

---

Simulated end voltage 3.1V = 19.993mA
Hardware end voltage 3.1V = 1.34mA
Difference = (19.993-11.34) = 8.653mA

## Discussion:

From the plotted graph, it is evident that the MOSFET remains off until VGS reaches approximately 3.1 V. Beyond this threshold voltage (VTH ≈ 3.0 V), ID increases sharply with VGS, showing the enhancement-mode behavior. The nonlinear rise is due to the increasing number of carriers in the channel. The difference between hardware and simulated activation point current is minimal but the 3.5V point current has a huge difference because in the lab we have external factors such as loose wiring and heat which contributes to error. Overall the simulation follows theoretical ideas so it has been successfully completed.

## Problem Statement-2:

To determine the output characteristics (VDS vs. ID) of an N-channel enhancement MOSFET for VGS = 3.1 V.

The equipment used is the same as Problem Statement-1.
The manual circuit diagram is also the same.

## PSPICE Schematic diagram:

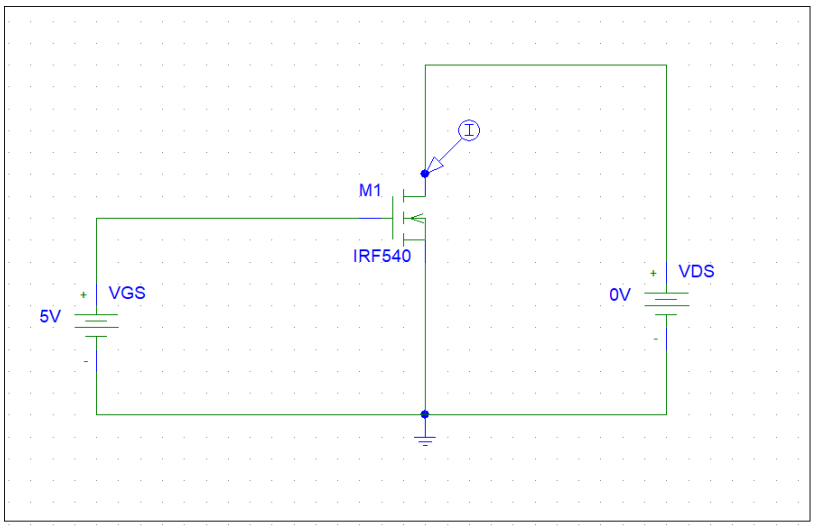


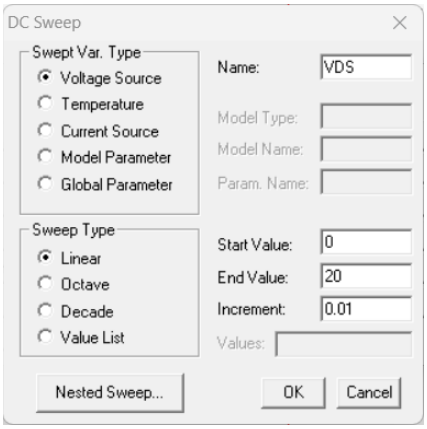

*Diagram for output characteristics in simulation*

## PSPICE Simulation settings:

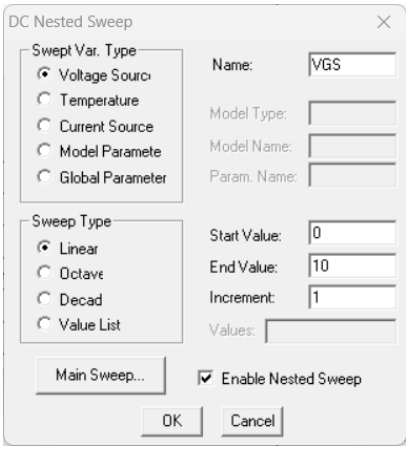
### Analysis setup menu:

Same as statement 1

### DC Sweep with nested functionality on:

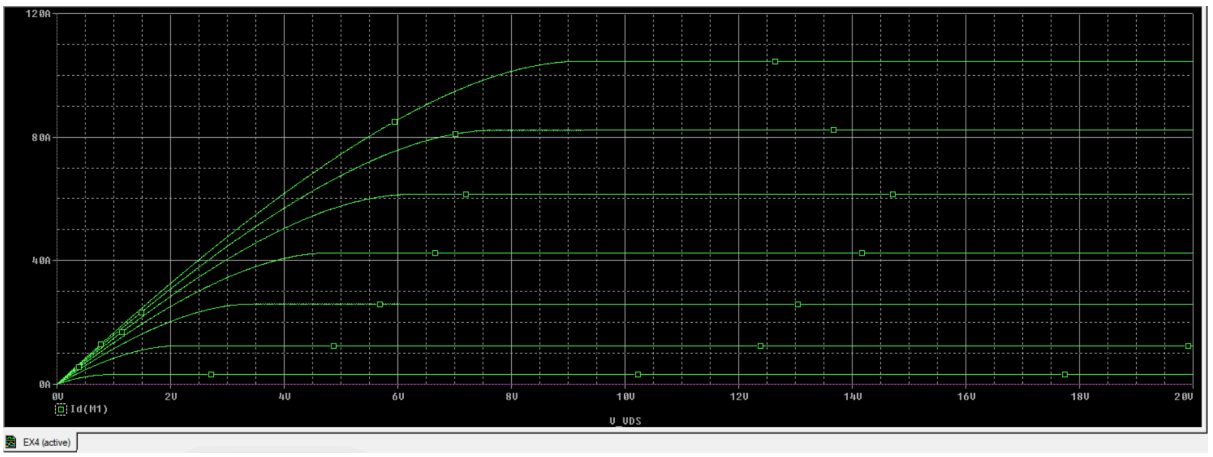



*Name: VDS, Start value: 0, End value: 20, Increment: 0.01*



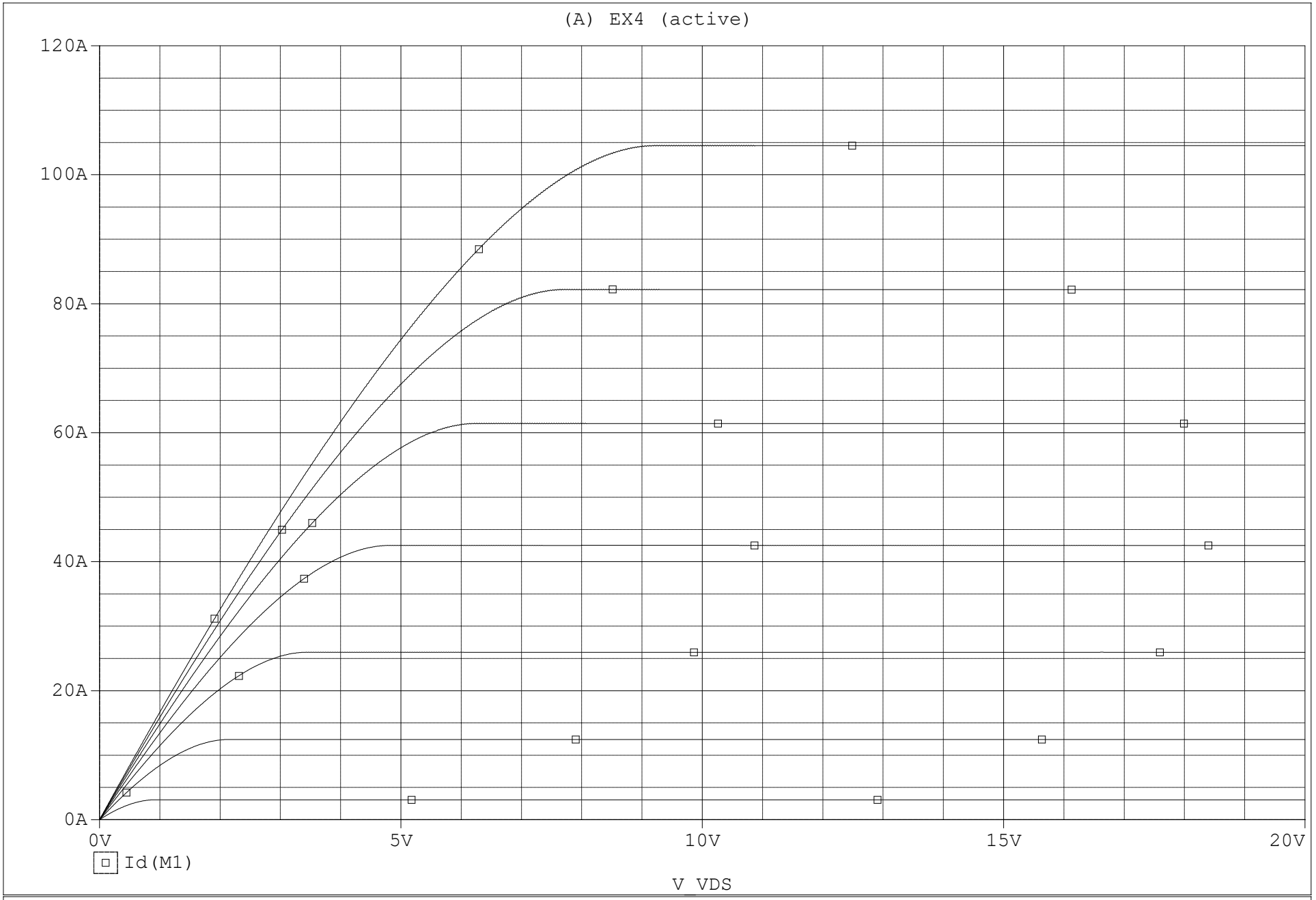

*Name: VGS, Start value: 0, End value: 10 Increment: 1*

## Output waveforms:




*Output characteristics simulated plot*

Explanation: The graph shown is the output characteristic curve of an N-channel




A1:(0.000,0.000) A2:(0.000,0.000) DIFF(A):(0.000,0.000)

MOSFET, where the drain current is plotted against the drain-to-source voltage for different values of gate-to-source voltage At low, the MOSFET operates in the ohmic or linear region, where the current increases almost linearly with voltage, behaving like a variable resistor. As increases, the curves gradually flatten, indicating the transition into the saturation or active region, where IDI_DID remains nearly constant and is primarily controlled by. For small, the MOSFET remains in cutoff, showing little or no current flow, while higher values allow significantly larger drain currents, with the uppermost curve exceeding 100 A. This demonstrates the ability of the MOSFET to handle large currents and illustrates how the device shifts between cutoff, linear, and saturation regions depending on the applied voltages.

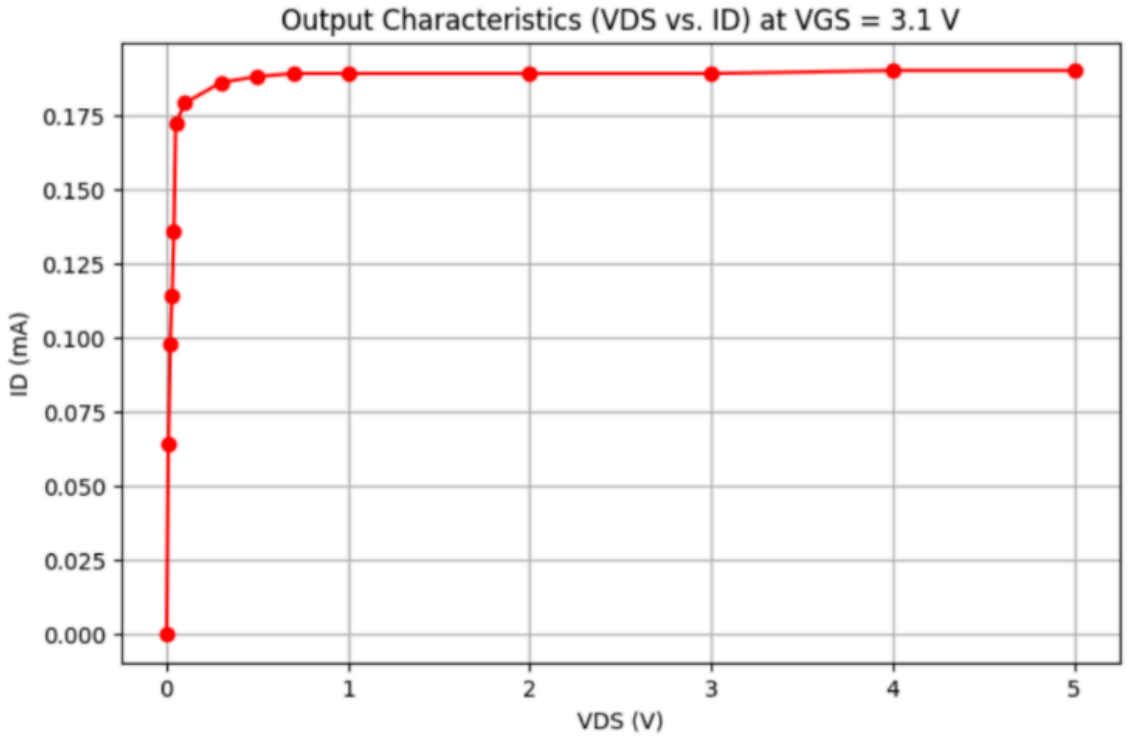
## Data table (Simulated):

| $V_{DS}$ (V) | $I_D$ |
|---|---|
| 0 | 0 |
| 0.01 | 108.123mA |
| 0.02 | 203.377mA |
| 0.03 | 305.934mA |
| 0.04 | 390.949mA |
| 0.05 | 497.571mA |
| 0.06 | 604.193mA |
| 0.07 | 710.816mA |
| 0.08 | 804.396mA |
| 0.09 | 904.615mA |
| 0.10 | 1.0023A |
| 1 | 1.0023A |
| 2 | 1.0023A |
| 3 | 1.0023A |

## Data table and Graph (From hardware experiment):

| $V_{DS}$ (V) | $V_{RD}$ (V) | $I_D = \frac{V_{RD}}{R_d}$ (mA) |
|---|---|---|
| 0 | 0 | 0 |
| .01 | 0.063 | 0.064 |
| .02 | 0.096 | 0.098 |
| .03 | 0.113 | 0.1141 |
| .04 | 0.135 | 0.136 |
| .05 | 0.169 | 0.172 |
| .10 | 0.177 | 0.179 |
| .30 | 0.184 | 0.186 |
| .50 | 0.186 | 0.188 |
| .70 | 0.187 | 0.189 |
| 1.0 | 0.187 | 0.189 |
| 2.0 | 0.187 | 0.189 |
| 3.0 | 0.188 | 0.189 |
| 4.0 | 0.189 | 0.190 |
| 5.0 | 0.189 | 0.190 |

3)MOSFET output characteristics curve using the data from Table 2




## Comparison:

If we connect a load (resistor) like the diagram from the lab manual.
Simulated saturation voltage 0.10V = 1.0023A

Hardware saturation voltage 0.50V = 0.188mA
Difference = (1.0023A-0.188mA) = 1.002112A

## Discussion:

From the simulated graph we can see that starting from 0 to 0.09V the current increases almost proportionally but after crossing 0.10V it stays constant with 1.0023A output current. This is the starting point of the saturation region. In the lab experiment the values are different and the saturation region starts from 0.50V with an output current value hovering around 0.188 to 0.190mA. There is about 1A difference here because in the lab inaccurate resistor values, human error, power supply issues, heat and other factors contribute to loss. The simulation values align with theoretical values and the graph shows constant current so the experiment was successful.

To conclude, input and transfer characteristics simulation was completed and it helped us to learn how MOSFET's work in different electronic devices.

## Drive links (.sch files): Output and transfer characteristics

# EEE205L

**Electronic Circuits I Laboratory**

# Lab Report

Section: 05

Group No:**04**

## Experiment no: 05 (Software)

Name of the experiment: *Investigation of I-V characteristics of BJT (PSPICE Simulation)*


*Prepared by:*

**Name: Tanzeel Ahmed** **ID: 24321367** **Signature** *Tanzeel*

*All Group members:*

| Sl. | Name | ID | Signature |
|---|---|---|---|
| 1. | **Esrar Ul Hossain Rafin** | **24121187** | *Esrar* |
| 2. | **Tasmiya Tahsin Roza** | **24121339** | *Tasmiya* |


Date of Submission: 26/08/2025

## Objective:

To measure and analyze the I-V characteristics of a BJT and determine its DC current gain (β).

## Theoretical Background:

In other words a Bipolar Junction Transistor (BJT) is a three terminal semiconductor component with Emitter, Base and Collector forms in such a way that each leg makes a p-n junction. Within NPN BJT, current flows in the emitter to the lightly doped base, where they are swept to the collector hence amplifying the current. Very small base current regulates collector-emitter current much larger, and the current gain is commonly 50-500 (called 50 500).

The transistor has 3 regions namely saturation (both junctions forward-biased), active (base-emitter forward-biased, collector-base reverse-biased), and cut off (both junctions are reverse-biased). These are input characteristics drawn by plotting base current against base-emitter voltage and output characteristics plotted by fixing base currents and observing collector current against collector-emitter voltage. There should be suitable biasing so that the active area of amplification is conducted.

In modern circuit analysis, simulation is widely used to predict and study the behavior of electronic circuits before actual implementation. Simulation provides a time efficient way to test different circuit configurations and verify theoretical calculations.

PSPICE is one of the most commonly used circuit simulation tools. It allows users to design electronic circuits on a computer, apply test signals, and visualize the circuit response through graphs and plots. By simulating BJT systems in PSPICE, we can understand its characteristics without any kind of practical loss.

## Problem Statement:

Determine the input and output characteristic curves of an NPN BJT and calculate its DC current gain.

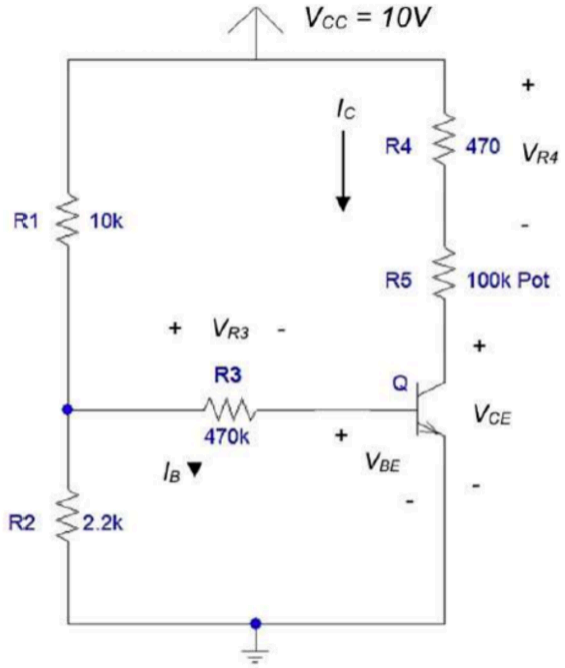
## List of equipments:

1. Suitable computer or laptop that meets the minimum requirements
2. ORCAD Pspice Schematics software

## List of equipments required in simulation:

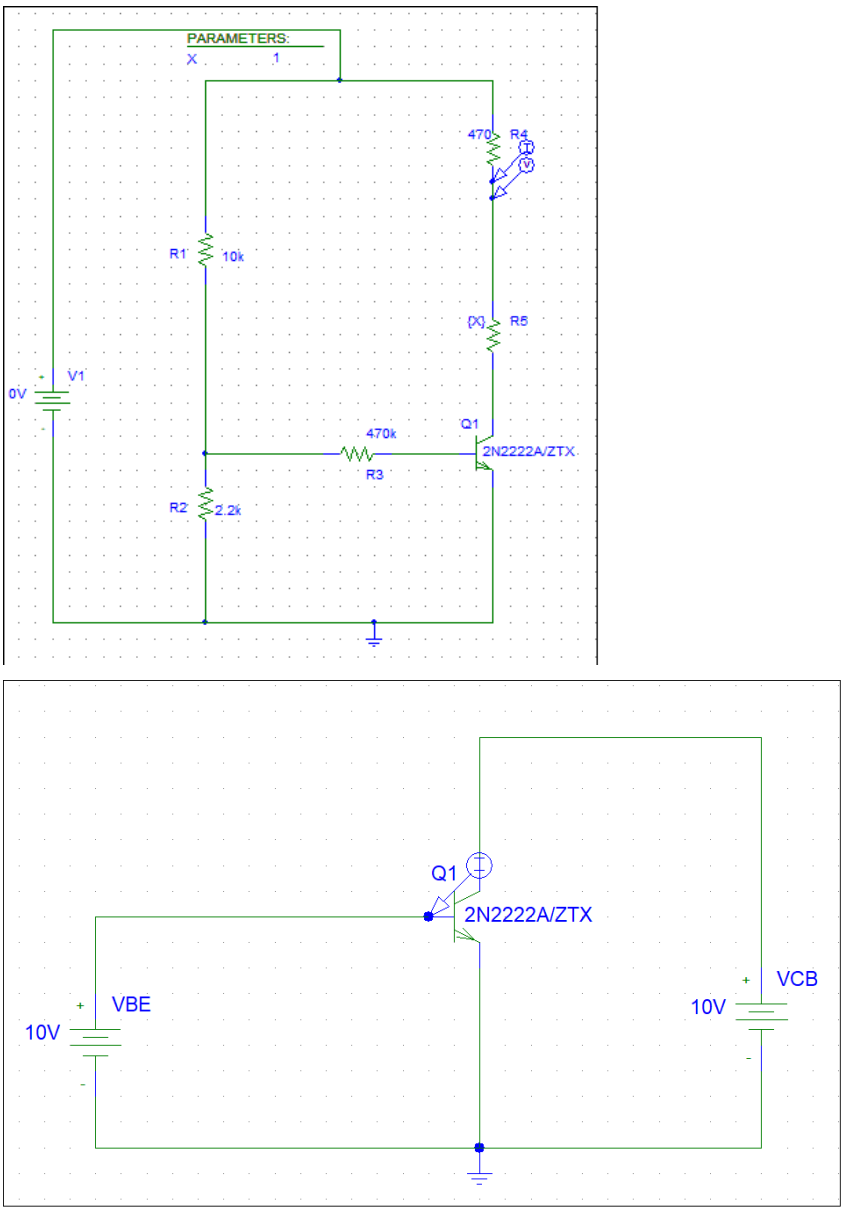
1. VDC - 2x
2. Resistors of various values
3. BJT (2N222A/ZTX)
4. Voltage level and current markers

## Circuit diagram (from manual):




*I-V investigation diagram from manual*

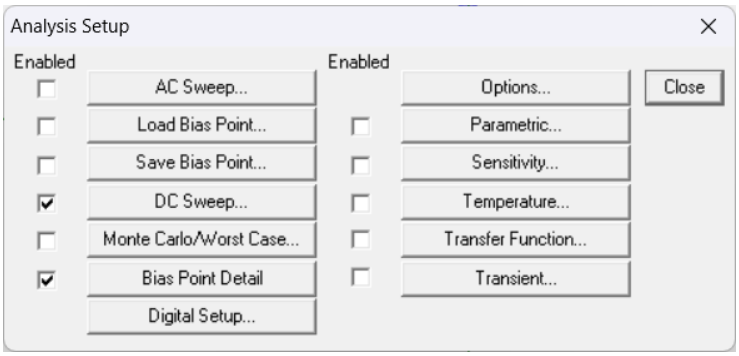
## PSPICE Schematic diagram:



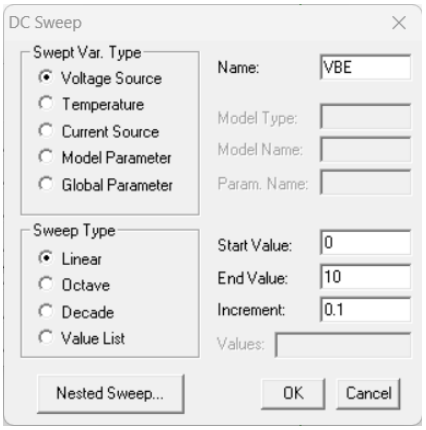

*I-V Investigation diagram simulated in schematics*

# PSPICE Simulation settings:

## Analysis setup menu:

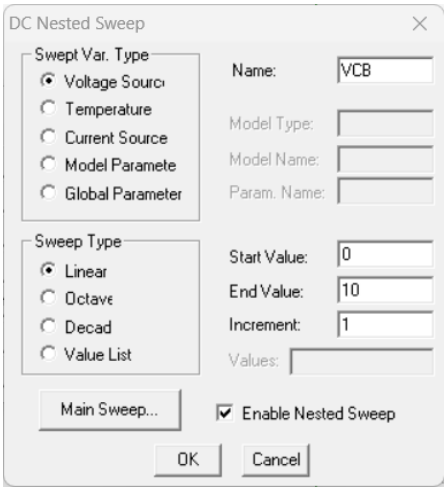


## DC Sweep (For input):



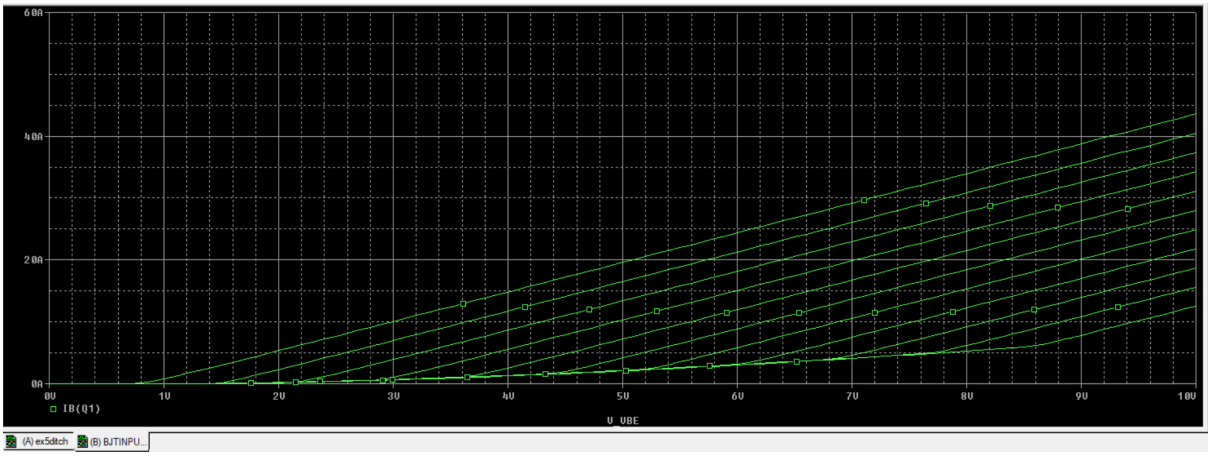

VBE, Start 0, End 10, Increment 0.1

## DC Nested Sweep (For input):




VCE, Start 0, End 10, Increment 1

# Output waveforms:

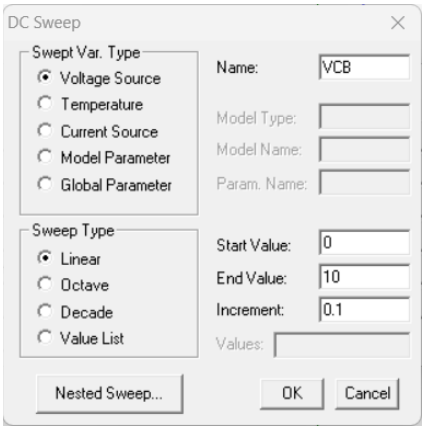



*Input characteristics plot*

Explanation: The input characteristic of the BJT was obtained by sweeping VBE from 0-10 V while keeping VcE fixed at different values. The resulting graph (Fig. ...)

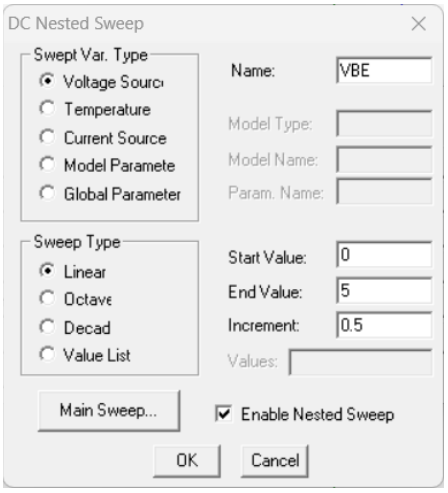
shows IB increasing exponentially with VBE, similar to a diode's forward conduction. At low VBE (<0.6 V), the base current is negligible, indicating cutoff. As VBE crosses 0.7 V, IB rises sharply. For higher VOE, the base current at a given VBE is slightly larger, due to reduced base-width and the Early effect. This behavior matches the theoretical input characteristic curves of a transistor.

## DC Sweep (For output:

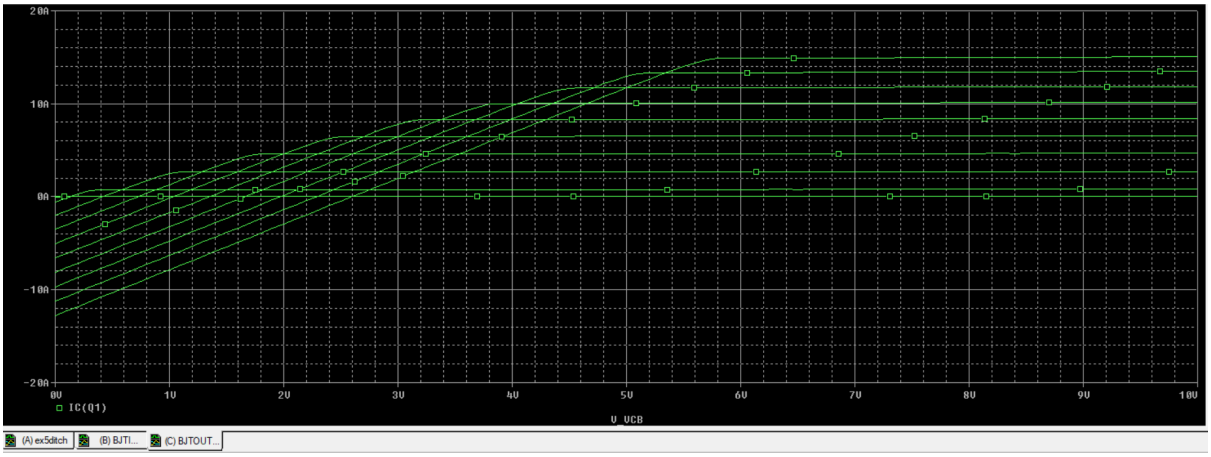



VCB, Start 0, End 10, Increment 0.1

## DC Nested Sweep (For output):



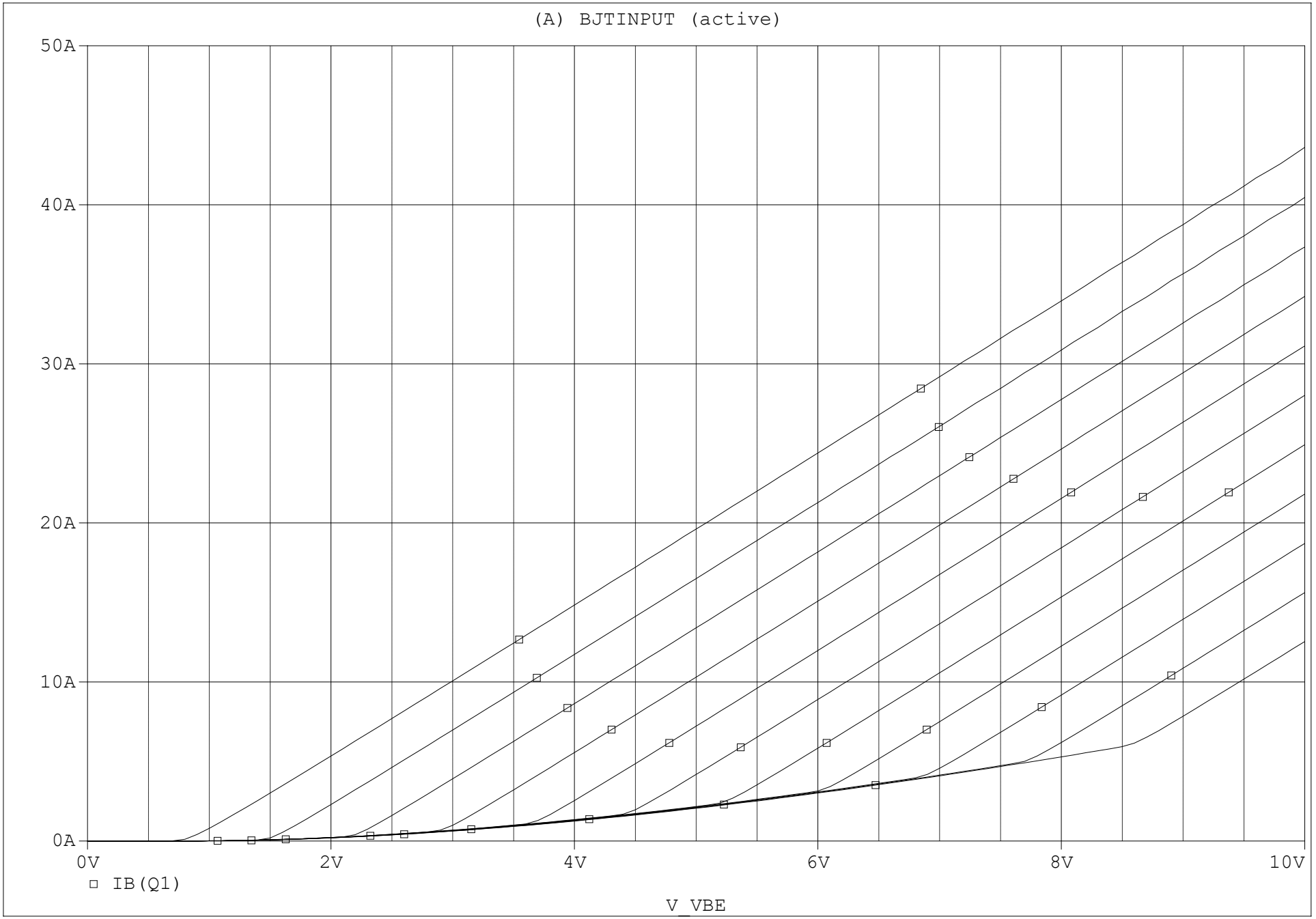

VBE, Start 0, End 10, Increment 1

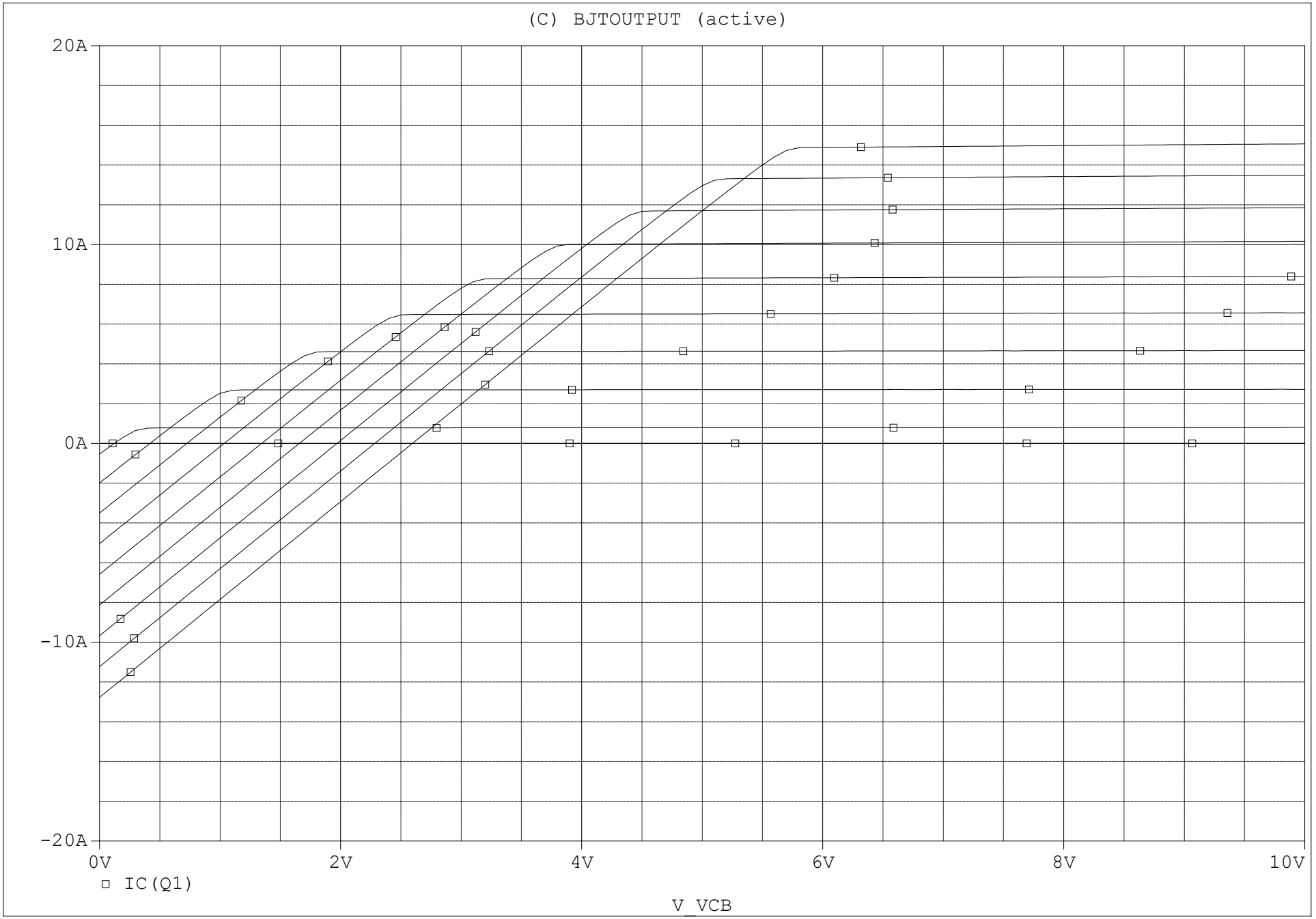



*Output characteristics plot*

* C:\Users\aryan\Downloads\fwdmosfetandbjtinputandoutputcharacteristics\BJTINPUT.sch

Date/Time run: 08/29/25 21:41:42 Temperature: 27.0




(C) BJTOUTPUT (active)
20A
10A
0A
-10A
-20A
0V
2V
4V
6V
8V
10V
IC(Q1)
V_VCB

Explanation: The output characteristics of the BJT were obtained by sweeping the collector-base voltage (VoB) while holding the base current (IB) constant. The resulting graph shows a family of curves representing different base currents. In the saturation region, Ic is nearly constant and increases very slowly with VCB. As VCB increases, the transistor enters the active region, where Io increases linearly with Vcg, and the slope of the curves becomes steeper with increasing IB. At very high VoB, the transistor enters the cutoff region, where Ic is effectively zero. These characteristics are consistent with the expected behavior of a BJT as an amplifier.

## Data table (Simulated):

| $V_{CE}$ (V) | $V_{R4}$ (mV) | $I_C = V_{R4} / R_4$ (mA) |
|---|---|---|
| 0 | 0 | 0 |
| 0.1 | 123 | 0.26 |
| 0.2 | 330 | 0.706 |
| 0.3 | 340 | 0.72 |
| 0.4 | 350 | 0.74 |
| 0.5 | 347 | 0.745 |
| 0.6 | 348 | 0.745 |
| 0.7 | 348 | 0.745 |
| 0.8 | 350 | 0.7490 |
| 0.9 | 349 | 0.747 |
| 1 | 350 | 0.749 |
| 2 | 354 | 0.758 |
| 3 | 357 | 0.728 |
| *4* | *359* | *0.749* |
| *5* | *360* | *0.743* |
| *6* | *361* | *0.779* |
| *7* | *364* | *0.783* |
| *8* | *366* | *0.78* |

| | | |
|---|---|---|
| *9* | *368* | *0.79* |
| *10* | *370* | *0.79* |

## Data table (From hardware experiment):

Table-1:

| $R_3$ (kΩ) | $V_{R3}$ (V) | $I_B = V_{R3} / R_3$ (μA) |
|---|---|---|
| 471 | 1.22 | $2.59 \times 10^{-6}$ |

Table-2:

| $R_4$ (kΩ) | $V_{CE}$ (V) | $V_{R4}$ (mV) | $I_C = V_{R4} / R_4$ (mA) |
|---|---|---|---|
| 0.467 | 0 | 0.03 | $6.42 \times 10^{-5}$ |
| | (0.101) 0.1 | 138 | 0.296 |
| | (0.202) 0.2 | 356 | 0.762 |
| | (0.312) 0.3 | 369 | 0.790 |
| | (0.407) 0.4 | 372 | 0.797 |
| | 6501 0.5 | 373 | 0.799 |
| | (0.608) 0.6 | 374 | 0.801 |
| | (0.697) 0.7 | 374 | 0.801 |
| | (0.812) 0.8 | 375 | 0.803 |
| | (0894) 0.9 | 376 | 0.805 |
| | (1.07) 1 | 376 | 0.805 |
| | (2.03) 2 | 382 | 0.818 |
| | (3.17) 3 | 383 | 0.82 |
| | (3.98) 4 | 385 | 0.824 |
| | (5.14) 5 | 387 | 0.829 |
| | (6.03) 6 | 391 | 0.837 |
| | (6.97) 7 | 393 | 0.841 |
| | (8.14) 8 | 395 | 0.846 |
| | (9.01) 9 | 398 | 0.852 |
| | (9.6) 10 | 399 | 0.854 |

## Comparison:

Random points have been taken for comparison
Simulated starting Ic = 0
Hardware starting Ic = $6.42*10^{-5}$

---

Simulated Ic at 0.5V = 0.745
Hardware Ic = 0.799
Difference = (0.799-0.745) = 0.054mA

---

Simulated Ic at 5V = 0.743
Hardware Ic = 0.829
Difference = (0.829-0.743) = 0.086mA

---

Simulated Ic at 10V = 0.79
Hardware Ic = 0.829
Difference = (0.829-0.79) = 0.039mA

## Discussion:

From the comparison of simulated and hardware results, it is observed that the measured collector current (Ic) values are consistently slightly higher than the simulated values across all test points. At Vo = 0.5, V, the hardware current was 0.799, mA compared to the simulated 0.745, mA, while at Vcg = 5 V the hardware result was 0.829, mA against 0.743, mA. Similarly, at Vcg = 10, V, the hardware current was 0.829, mA compared to the simulated 0.790, mA. The deviations remain small, ranging between 0.039 mA and 0.086 mA, indicating that while the practical transistor exhibits slightly higher current, the overall trends and behaviors between hardware and simulation closely agree. These differences can be attributed to factors such as parasitic resistances, component tolerances, and temperature effects in real devices, which are not fully captured in the idealized simulation model.

## Drive links (.sch files): EX5

# EEE205L

**Electronic Circuits I Laboratory**

# Lab Report

Section: 05

Group No:**04**

## Experiment no: 06 (Software)

Name of the experiment: *Implementation of Common Emitter BJT Amplifier Circuits (PSPICE Simulation)*


*Prepared by:*

**Name: Tanzeel Ahmed** **ID: 24321367** **Signature** *Tanzeel*

*All Group members:*

| Sl. | Name | ID | Signature |
|---|---|---|---|
| 1. | **Esrar Ul Hossain Rafin** | **24121187** | *Esrar* |
| 2. | **Tasmiya Tahsin Roza** | **24121339** | *Tasniya* |


Date of Submission: 26/08/2025

## Objective:

Objective: The aim of the experiment is to explore the common emitter amplifier and find its gain, input and output impedance.gain (β).

## Theoretical Background:

Bipolar transistors have two junctions namely the emitter-base and collector-base. When operating at high frequencies the corresponding capacitances start to have a significant effect on the operation of the devices; at low-band and mid-band frequencies can be ignored at the expense of minimal transistor performance.

In modern circuit analysis, simulation is widely used to predict and study the behavior of electronic circuits before actual implementation. Simulation provides a time efficient way to test different circuit configurations and verify theoretical calculations.

PSPICE is one of the most commonly used circuit simulation tools. It allows users to design electronic circuits on a computer, apply test signals, and visualize the circuit response through graphs and plots. By simulating BJT systems in PSPICE, we can understand its characteristics without any kind of practical loss.

## Problem Statement:

This experiment investigates the common emitter amplifier's performance by measuring its current gain (β), input impedance, and output impedance at low-band and mid-band frequencies using an n-p-n transistor

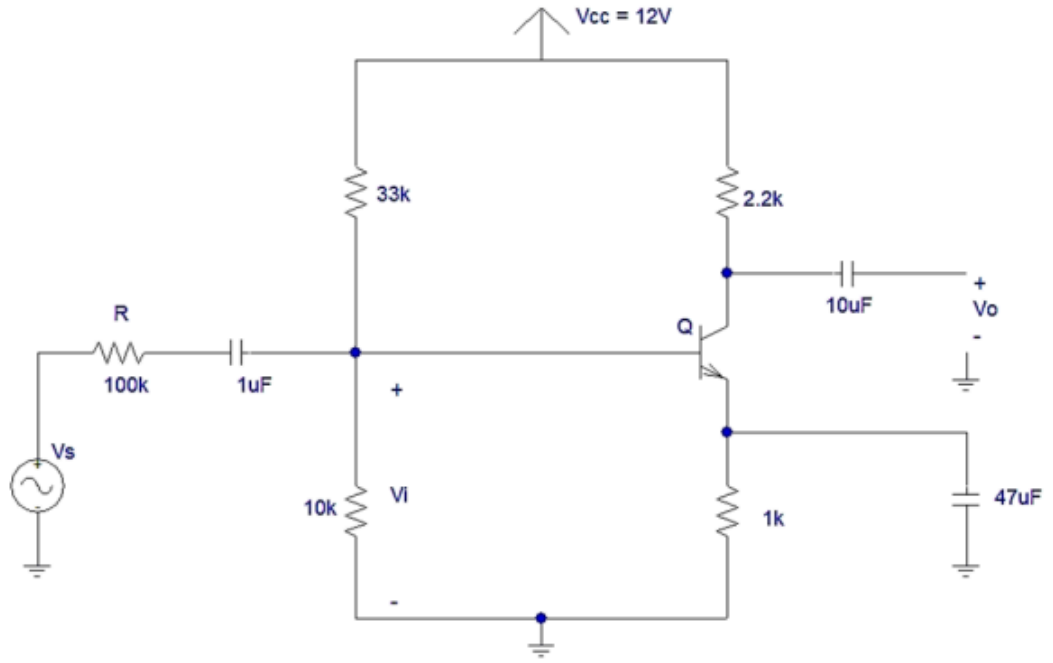
## List of equipments:

1. Suitable computer or laptop that meets the minimum requirements
2. ORCAD Pspice Schematics software

## List of equipments required in simulation:

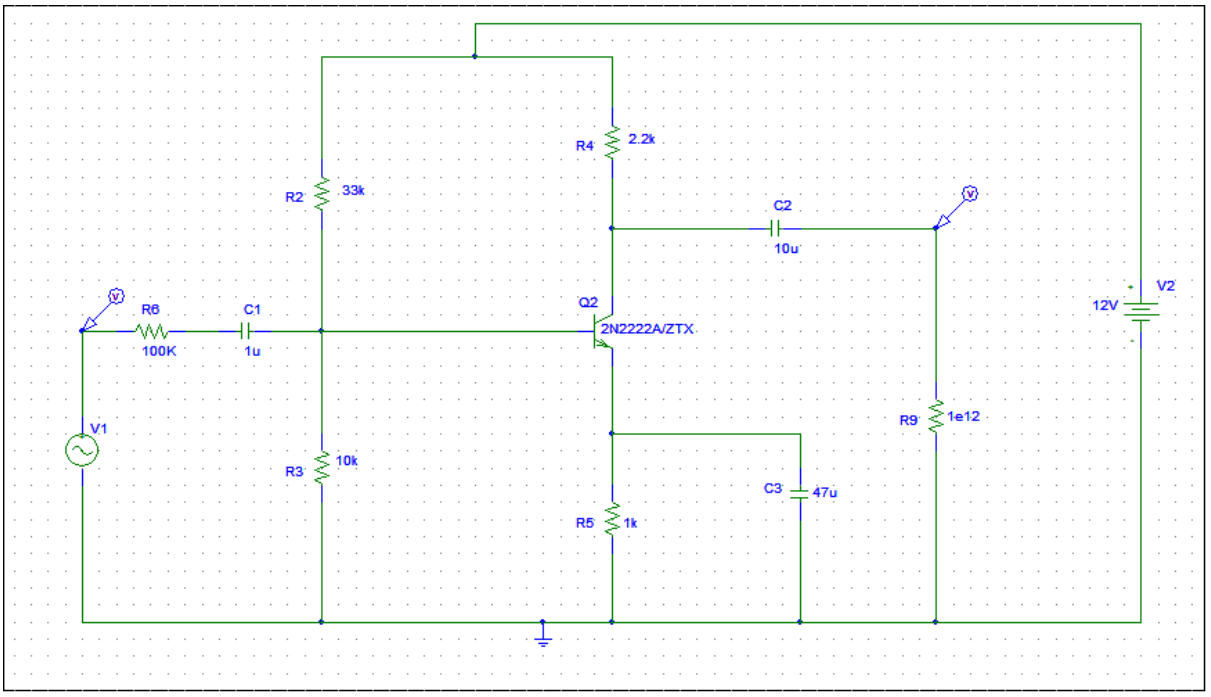
1. VSIN - 1x
2. VDC - 1x
3. Capacitors of various values
4. Resistors of various values
5. BJT (2N222A/ZTX)
6. Voltage level markers

## Circuit diagram (from manual):




*Common emitter BJT amplifier circuit*

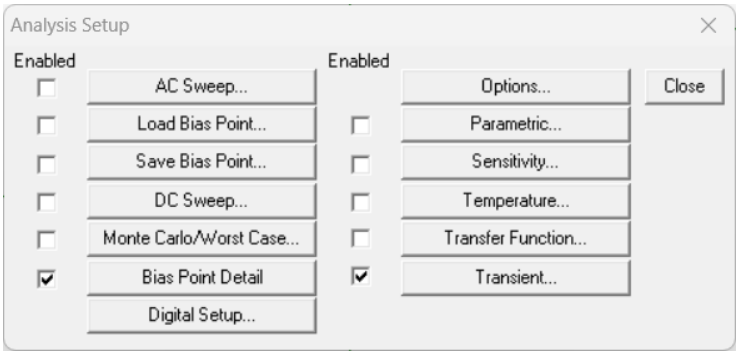
## PSPICE Schematic diagram:



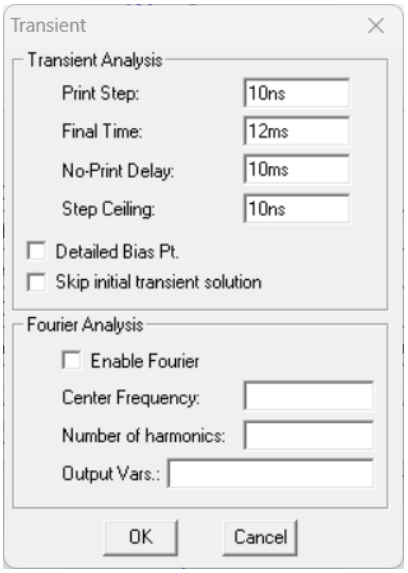

*Common emitter BJT amplifier circuit in simulation*

## PSPICE Simulation settings:

### Analysis setup menu:

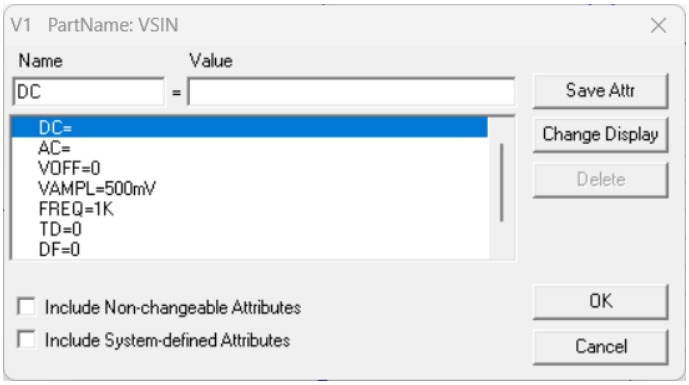



## Transient:




*Print step 10ns, Final time 12ms, No-print delay 10ms, Step Ceiling 10ns*

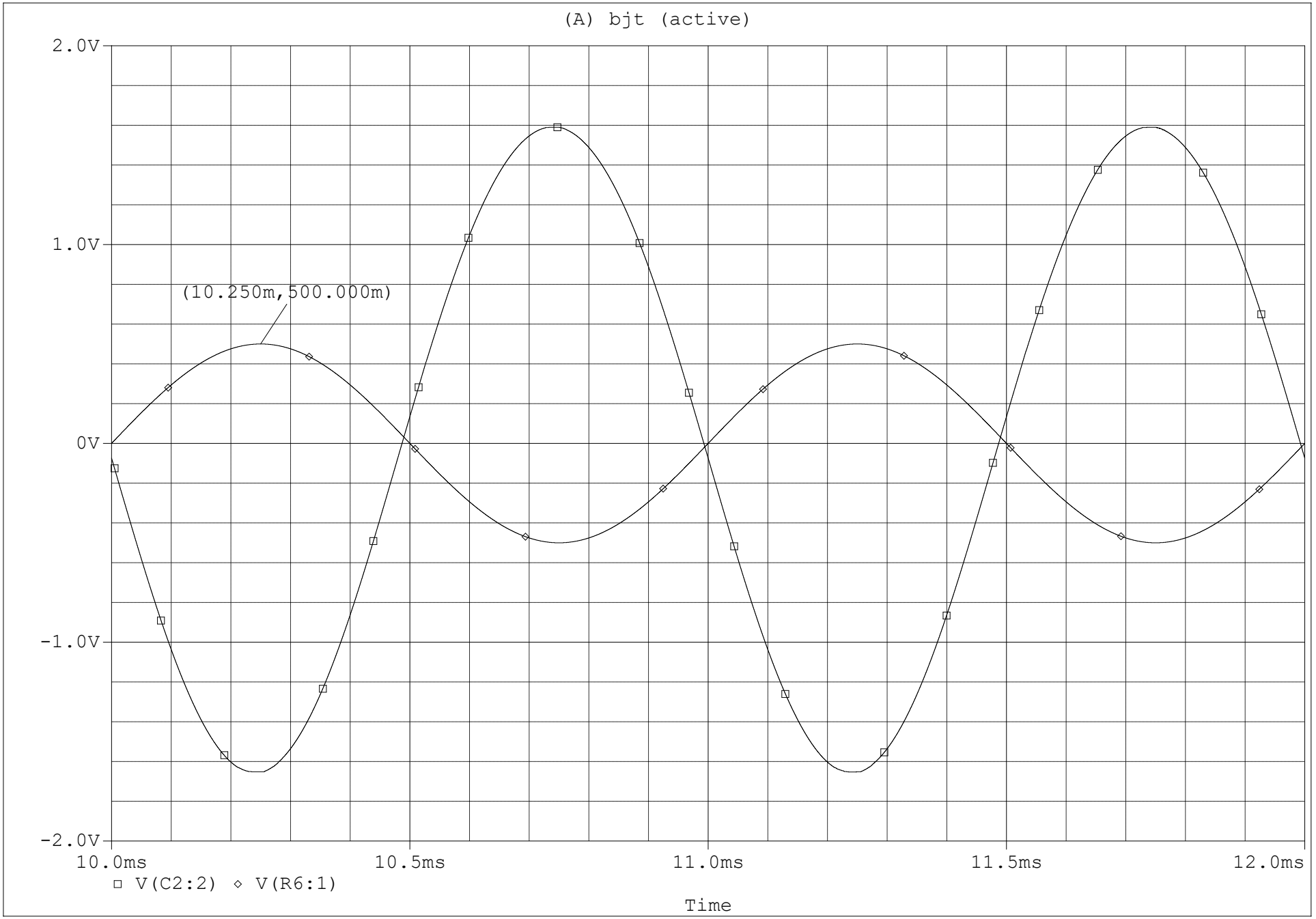
## VSIN:



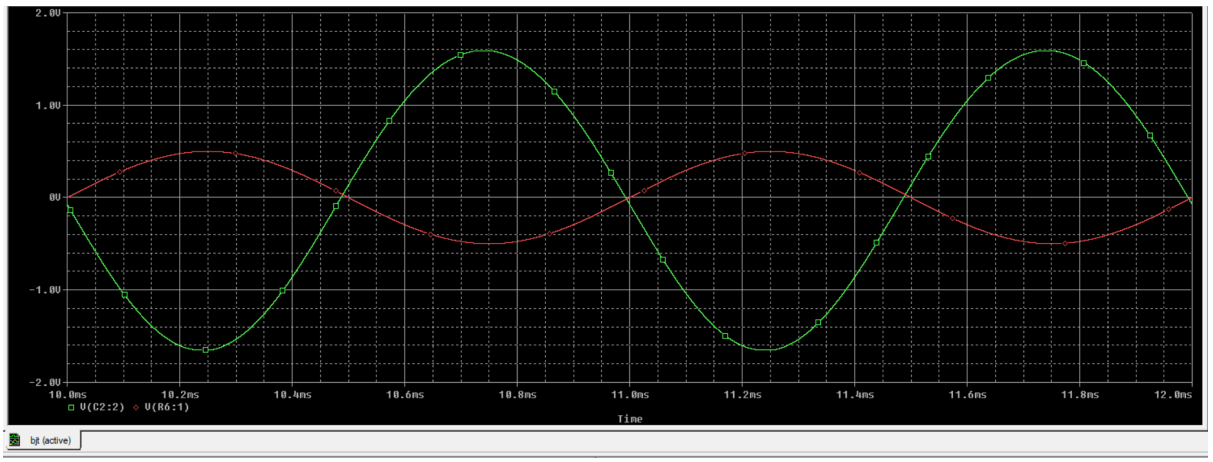

*VOFF=0, VAMPL=500mV. FREQ=1K*

* D:\BracU\5. Fifth Semester (SU-25)\EEE205L\SW EXP\ex6\bjt.sch

Date/Time run: 08/28/25 21:03:41 Temperature: 27.0



## Output waveforms:




## Data table (Simulated):

**Amplification Vi** = 5.11mV
Vo = 733mV

(Reason: the 100 kΩ input resistor and 1 µF coupling cap drop the 0.5 V source to ~5.1 mV at the base; small-signal gain $\approx -R_C/(r_e + (R_5 \parallel X_{C3})) \approx -2200/(11.96 + 3.39) \approx -143.5$.)

**Input impedance Ri**
Vi = 5.11mV
Vs=500mV
R=100k-ohm (series source resistor)

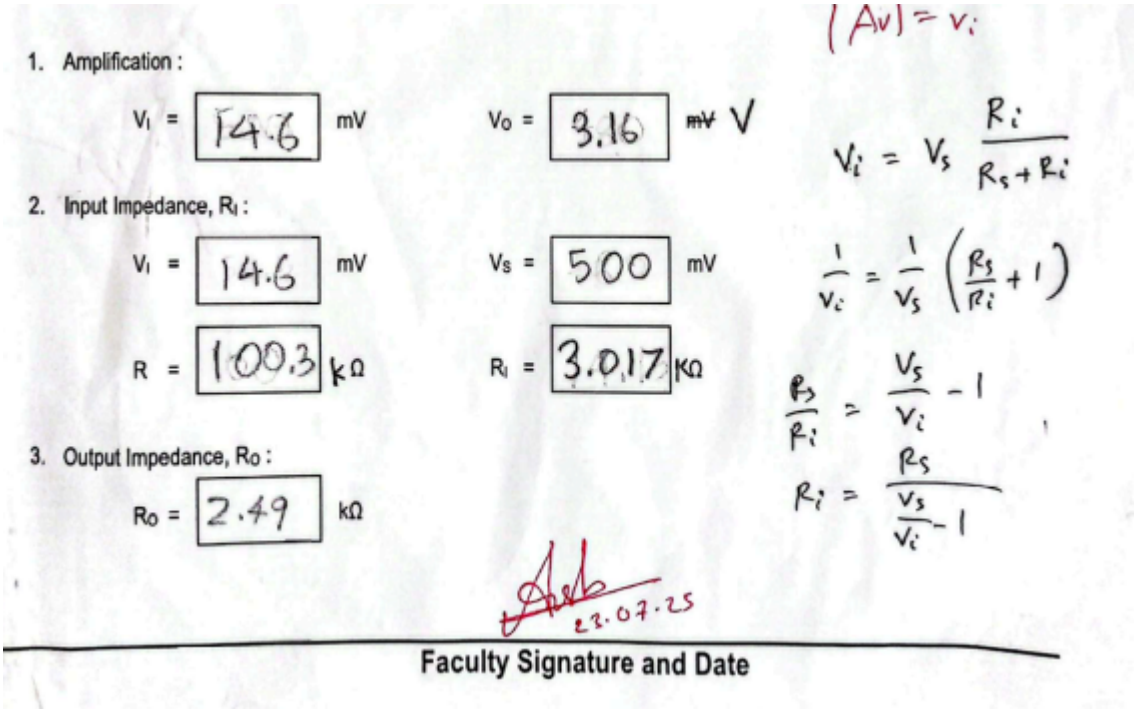
- $R_i = R\dfrac{V_i}{V_s - V_i} \approx 100\,000 \times \dfrac{0.00511}{0.500 - 0.00511} \approx 1.03\ \text{k}\Omega$

(Consistent with $r_\pi \parallel (R_2 \parallel R_3)$: with $I_C \approx 2.09\ \text{mA} \Rightarrow r_e \approx 11.96\,\Omega$, $\beta \approx 100 \Rightarrow r_\pi \approx 1.20\,\text{k}\Omega$; $R_2 \parallel R_3 \approx 7.67\,\text{k}\Omega$; hence $R_i \approx 1.04\,\text{k}\Omega$.)

**Output Impedance Ro**

- $R_o \approx R_C + |X_{C2}|$ at 1 kHz (load $\approx \infty$ via $R_9$)
- $|X_{C2}| = \dfrac{1}{2\pi f C_2} \approx \dfrac{1}{2\pi(1000)(10\,\mu\text{F})} \approx 15.9\,\Omega$
- $R_o \approx 2.2\,\text{k}\Omega + 15.9\,\Omega \approx \mathbf{2.22\ k\Omega}$

## Data table (From hardware experiment):




## Comparison:

Most of the data doesn't match with the software experiment because in simulation, an extra load resistor 1e12 was added so the software shows an output plot. This was done in our simulation class because without this resistor, there was a flatline output.

## Discussion:

The PSPICE simulation of the common emitter amplifier confirmed its amplification property, where a small input signal of 5.11 mV was amplified to about 733 mV. The input impedance was calculated using the source resistance and voltage division, while the output impedance was estimated from the circuit response. However, differences were found when comparing the simulated and hardware results, mainly because an additional large load resistor (1e12 Ω) was used in the simulation to obtain a proper output waveform. This adjustment, along with the idealized conditions of simulation, explains the mismatch with practical data. Overall, the experiment successfully demonstrated the operation of a common emitter amplifier and the value of using PSPICE for circuit analysis before implementation.

## Drive links (.sch files): EXP 6 Common emitter amplifier