DANANG UNIVERSITY

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FACULTY OF SCIENCE AND TECHNOLOGY

ECE 485/585 MICROPROCESSOR SYSTEM DESIGN

FINAL PROJECT

Cache Simulation

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1. Project Objective

The project focuses on designing and simulating the L1 Split cache for a 32-bit processor. This processor is not intended to be used in a multi-core or multi-processing environment and does not require support for cache coherence.

2. System Description

2.1. L1 Instruction Cache

Configuration: 2-way set associative

Size: 16K sets and 64-byte lines

2.2. L1 Data Cache

Configuration: 4-way set associative

Size: 16K sets and 64-byte lines

The L1 data cache uses write allocate and is write-back except for the first write to a line which is write-through

Both caches employ **LRU replacement policy** and are backed by a shared L2 cache. The cache hierarchy is **inclusive**.

Since this is a 32-bit processor, there will be 32 address bits. With 64-byte lines, there are 6 address bits (2^6) for Byte Select bits. 16K sets cache is reflected in the 14 address bits (2^{14}) for index. We then know there are 12 tag bits by looking at the difference of byte offset bits and index bits from address bits (32-6-14 = 12).

Tag	Index	Offset
12	14	6

3. Simulation Details

Project: using C++ to describe and simulate cache. Simulation does not need to be clock accurate and does not need to store/retrieve data.

Key statistics: The simulation will record and display:

- Number of cache reads
- Number of cache writes
- Number of cache hits
- Number of cache misses
- Cache hit ratio

Communicating with the shared L2 cache (maintain inclusivity the L1 caches): The following messages will be displayed in the simulation (where <address> is a hexadecimal address):

- **Write to L2 <address>**: This operation is used to write back a modified line to L2 upon eviction from the L1 cache.
- **Read from L2 <address>**: This operation is used to obtain the data from L2 on an L1 cache miss
- **Read for Ownership from L2 <address>**: This operation is used to obtain the data from L2 on an L1 cache write miss

Simulation mode:

➢ **Mode 0**: displays only the required summary of usage statistics and responses to 9s in the trace file and nothing else.
➢ **Mode 1**: display everything from mode 0 but also display the communication messages to the L2 described above (and nothing else).

Trace file format: The testbench must read cache accesses/events from a text file of the following format. Each line has a structure:

- **n <address>**, in which:
  + **n**: The type of operation.
  + **address**: hex address.

where **n** is:

0	read data request to L1 data cache
1	write data request to L1 data
2	cache instruction fetch (a read request to L1 instruction cache)
3	evict command from L2 (for L2 evictions and inclusivity)
8	clear the cache and reset all state (and statistics) but continue reading trace file
9	print contents and state of the cache (continue reading traces, don't clear cache)

**Code and test plan available here: taothao120/L1_Cache_Design*

4. Test plan

Data Cache contents table Instruction Cache contents table	Data Cache	Instruction cache

Way	0	1	2	3
Tag	-	-	-	-
LRU Bits	-	-	-	-
States	I	I	I	I

Reads	0	Reads	0
Writes	0		
Hits	0	Hits	0
Misses	0	Misses	0
Hit Ratio	0 : 0	Hit Ratio	0

a) Scenario 1: Loading all data cache lines of a particular set

- Trace_file_01:

  0 286CD482
  0 800CD490
  0 236CD488
  0 999CD4BA

  - Step 1: 0 286CD482
    Binary: 0010 1000 0110 1100 1101 0100 1000 0010

Byte offset	Index	Tag
00 0010	1100 1101 0100 10	0010 1000 0110

Data Cache contents table				
Way	0	1	2	3
Tag	286	-	-	-
LRU Bits	11	-	-	-
States	V	I	I	I

Data Cache		Instruction cache	
Reads	1	Reads	0
Writes	0		
Hits	0	Hits	0
Misses	1	Misses	0

  - Step 2: 0 800CD490
    Binary: 1000 0000 0000 1100 1101 0100 1001 0000

Byte offset	Index	Tag

01 0000	1100 1101 0100 10	1000 0000 0000

Data Cache contents table				
Way	0	1	2	3
Tag	286	800	-	-
LRU Bits	10	11	-	-
States	V	V	I	I

Data Cache		Instruction cache	
Reads	1	**Reads**	0
Writes	0		
Hits	0	**Hits**	0
Misses	1	**Misses**	0

- Step 3: 0 236CD488

  Binary: 0010 0011 0110 1100 1101 0100 1000 1000

Byte offset	Index	Tag
00 1000	1100 1101 0100 10	0010 0011 0110

Data Cache contents table				
Way	0	1	2	3
Tag	286	800	236	-
LRU Bits	01	10	11	-
States	V	V	V	I

Data Cache		Instruction cache	
Reads	1	**Reads**	0
Writes	0		
Hits	0	**Hits**	0
Misses	1	**Misses**	0

- Step 4: 0 999CD4BA

  Binary: 1001 1001 1001 1100 1101 0100 1011 1010

Byte offset	Index	Tag
11 1010	1100 1101 0100 10	1001 1001 1001

Data Cache contents table	Data Cache	Instruction cache

Way	0	1	2	3
Tag	286	800	236	999
LRU Bits	00	01	10	11
States	V	V	V	V

Reads	1	Reads	0
Writes	0		
Hits	0	Hits	0
Misses	1	Misses	0

=> Final results of Trace_file_01:

Scenario 1: Data Cache contents table				
Way	1	2	3	4
Tag	286	800	236	999
LRU Bits	00	01	10	11
States	V	V	V	V

Data Cache		Instruction cache	
Reads	4	Reads	0
Writes	0		
Hits	0	Hits	0
Misses	4	Misses	0
Hit Ratio	0 : 4	Hit Ratio	0

b) Scenario 2: Read/ Write on cache after Scenario 1:

- Trace_file_02: (add to trace_file_01)
  0 286CD495
  1 236CD483
  1 123CD4B1
  2 871CD4A3

  - Step 1: 0 286CD495
    Binary: 0010 1000 0110 1100 1101 0100 1001 0101

Byte offset	Index	Tag
01 0101	1100 1101 0100 10	0010 1000 0110

+ The same Tag bit as Way-0 in Scenario-1 should be Read-hit. Therefore do not change the state

Data Cache contents table

Data Cache	Instruction

Way	0	1	2	3
Tag	286	800	236	999
LRU Bits	11	00	01	10
States	V	V	V	V

		cache	
Reads	1	**Reads**	0
Writes	0		
Hits	1	**Hits**	0
Misses	0	**Misses**	0

- Step 2: 1 236CD483

  Binary: 0010 0011 0110 1100 1101 0100 1000 0011

Byte offset	Index	Tag
00 0011	1100 1101 0100 10	0010 0011 0110

  + The same Tag bit as Way-2 in Scenario-1 should be Write-hit. Therefore do change the state

Data Cache contents table				
Way	0	1	2	3
Tag	286	800	236	999
LRU Bits	10	00	11	01
States	V	V	M	V

Data Cache		**Instruction cache**	
Reads	0	**Reads**	0
Writes	1		
Hits	1	**Hits**	0
Misses	0	**Misses**	0

- Step 3: 1 123CD4B1

Binary: 0001 0010 0011 1100 1101 0100 1011 0001

Byte offset	Index	Tag
11 0001	1100 1101 0100 10	0001 0010 0011

+ The set is filled, so the way-1 with LRU value is 0 will be evicted to make room for another block then decrementing the LRU value of other lines.
+ In this case, the data will install in way-1 and update LRU bits

Data Cache contents table				
Way	0	1	2	3
Tag	286	123	236	999
LRU Bits	01	11	10	00
States	V	M	M	V

Data Cache		Instruction cache	
Reads	0	**Reads**	0
Writes	1		
Hits	0	**Hits**	0
Misses	1	**Misses**	0

- Step 4: 2 871CD4A3

  Binary: 1000 0111 0001 1100 1101 0100 1010 0011

Byte offset	Index	Tag
10 0011	1100 1101 0100 10	1000 0111 0001

Instruction Cache contents table		
Way	0	1
Tag	871	-
LRU Bits	1	-
States	V	I

Data Cache		Instruction cache	
Reads	0	**Reads**	1
Writes	0		
Hits	0	**Hits**	0
Misses	0	**Misses**	1

=> Final results of Trace_file_02: (for data cache statistic)

Scenario 1: Data Cache contents table				
Way	1	2	3	4
Tag	286	123	236	999
LRU Bits	01	11	10	00
States	V	M	M	V

Data Cache		Instruction cache	
Reads	5	**Reads**	1
Writes	2		
Hits	5	**Hits**	0
Misses	5	**Misses**	1

Instruction Cache contents table		
Way	0	1
Tag	871	-
LRU Bits	1	-
States	V	I

Hit Ratio	2 : 7	**Hit Ratio**	0

c) Scenario 3:Evict/print/Clear on cache after Scenario 2:

- Trace_file_03:
  3 236CD483
  1 223CD484
  8
  0 245CD491
  9
  - Step 1: 3 236CD483

    Binary: 0010 0011 0110 1100 1101 0100 1000 0011

Byte offset	Index	Tag
01 0101	1100 1101 0100 10	0010 0011 0110

+ The same Tag bit as Way-3 in Scenario-2 should be evicted.

Data Cache contents table				
Way	0	1	2	3
Tag	286	123	-	999
LRU Bits	01	11	10	00
States	V	V	I	V

Data Cache		Instruction cache	
Reads	0	**Reads**	0
Writes	0		
Hits	0	**Hits**	0
Misses	0	**Misses**	0

- Step 2: 1 223CD484

Binary: 0010 0010 0011 1100 1101 0100 1000 0100

Byte offset	Index	Tag
00 0100	1100 1101 0100 10	0010 0010 0011

+ The other Tag bit as Way-3 should be written.

Data Cache contents table				
Way	0	1	2	3
Tag	286	123	223	999
LRU Bits	01	10	11	00
States	V	M	V	V

Data Cache		**Instruction cache**	
Reads	0	**Reads**	0
Writes	1		
Hits	0	**Hits**	0
Misses	1	**Misses**	0

- Step 3: 8

+ Clear the cache.

- Step 4: 0 245CD491

  Binary: 0010 0100 0101 1100 1101 0100 1001 0001

Byte offset	Index	Tag
01 0001	1100 1101 0100 10	0010 0100 0101

+ The other Tag bit as Way-3 should be written.

Data Cache contents table				
Way	0	1	2	3

Data Cache		**Instruction cache**	
Reads	0	**Reads**	0

Tag	245	-	-	-
LRU Bits	11	-	-	-
States	V	I	I	I

Writes	1		
Hits	0	Hits	0
Misses	1	Misses	0

5. Simulation results

a) Scenario 1: Loading all data cache lines of a particular set

```
  Please enter the mode number you'd like to select (0,1): 0

Operation: 0, Address: 286cd482
Operation: 0, Address: 800cd490
Operation: 0, Address: 236cd488
Operation: 0, Address: 999cd4ba
Operation: 9, Address: 999cd4ba

        ** KEY CACHE USAGE STATISTICS **

        -- DATA CACHE STATISTICS --
 number of Cache Reads:         4
 number of Cache Writes:        0
 number of Cache Hits:          0
 number of Cache Misses:        4
 Cache Hit Ratio:               0
 Cache Hit Ratio percentage:    0 %

 More information in valid line:
Line valid : 286cd482   |       Way : 0        |       Set :3352      |       State : V      |       LRU bit : 1    |       Tag :286
Line valid : 800cd490   |       Way : 1        |       Set :3352      |       State : V      |       LRU bit : 2    |       Tag :800
Line valid : 236cd488   |       Way : 2        |       Set :3352      |       State : V      |       LRU bit : 3    |       Tag :236
Line valid : 999cd4ba   |       Way : 3        |       Set :3352      |       State : V      |       LRU bit : 4    |       Tag :999

       There are 4 valid lines

 The cache instruction was not used/not operated on

        --- L1 Split Cache Anaylsis and Simulation Completed! ---
```

b) Scenario 2: Read/ Write on cache after Scenario 1:

```
Operation: 0, Address: 286cd482
Operation: 0, Address: 800cd490
Operation: 0, Address: 236cd488
Operation: 0, Address: 999cd4ba
Operation: 0, Address: 286cd495
Operation: 1, Address: 236cd483
Operation: 1, Address: 123cd4b1
Operation: 2, Address: 871cd4a3
Operation: 9, Address: 871cd4a3

        ** KEY CACHE USAGE STATISTICS **

        -- DATA CACHE STATISTICS --
 number of Cache Reads:         5
 number of Cache Writes:        2
 number of Cache Hits:          2
 number of Cache Misses:        5
 Cache Hit Ratio:               0.285714
 Cache Hit Ratio percentage:    28.5714 %

 More information in valid line:
Line valid : 286cd495   |       Way : 0        |       Set :3352      |       State : V      |       LRU bit : 2    |       Tag :286
Line valid : 123cd4b1   |       Way : 1        |       Set :3352      |       State : M      |       LRU bit : 4    |       Tag :123
Line valid : 236cd483   |       Way : 2        |       Set :3352      |       State : M      |       LRU bit : 3    |       Tag :236
Line valid : 999cd4ba   |       Way : 3        |       Set :3352      |       State : V      |       LRU bit : 1    |       Tag :999

       There are 4 valid lines

        -- INSTRUCTION CACHE STATISTICS --
 number of Cache Reads:         1
 number of Cache Hits:          0
 number of Cache Misses:        1
 Cache Hit Ratio:               0
 Cache Hit Ratio percentage:    0 %

 More information in valid line:
 Line valid : 871cd4a3  |       Way : 0        |       Set :3352      |       State : V      |       LRU bit : 1    |       Tag :871

       There are 1 valid lines

        --- L1 Split Cache Anaylsis and Simulation Completed! ---
```

c) Scenario 3:Evict/Inst_fetch/print/Clear on cache after Scenario 2:

```
Operation: 0, Address: 286cd482
Operation: 0, Address: 800cd490
Operation: 0, Address: 236cd488
Operation: 0, Address: 999cd4ba
Operation: 0, Address: 286cd495
Operation: 1, Address: 236cd483
Operation: 1, Address: 123cd4b1
Operation: 2, Address: 871cd4a3
Operation: 3, Address: 236cd483
Operation: 1, Address: 223cd484
Operation: 9, Address: 223cd484

        ** KEY CACHE USAGE STATISTICS **

        -- DATA CACHE STATISTICS --
 number of Cache Reads:         5
 number of Cache Writes:        3
 number of Cache Hits:          2
 number of Cache Misses:        6
 Cache Hit Ratio:               0.25
 Cache Hit Ratio percentage:    25 %

 More information in valid line:
Line valid : 286cd495   |        Way : 0        |        Set :3352      |        State : V      |        LRU bit : 2    |        Tag :286
Line valid : 123cd4b1   |        Way : 1        |        Set :3352      |        State : M      |        LRU bit : 3    |        Tag :123
Line valid : 223cd484   |        Way : 2        |        Set :3352      |        State : V      |        LRU bit : 4    |        Tag :223
Line valid : 999cd4ba   |        Way : 3        |        Set :3352      |        State : V      |        LRU bit : 1    |        Tag :999

       There are 4 valid lines

        -- INSTRUCTION CACHE STATISTICS --
 number of Cache Reads:         1
 number of Cache Hits:          0
 number of Cache Misses:        1
 Cache Hit Ratio:               0
 Cache Hit Ratio percentage:    0 %

 More information in valid line:
 Line valid : 871cd4a3  |        Way : 0        |        Set :3352      |        State : V      |        LRU bit : 1    |        Tag :871

       There are 1 valid lines

        --- L1 Split Cache Anaylsis and Simulation Completed! ---
```

```
Operation: 0, Address: 286cd482
Operation: 0, Address: 800cd490
Operation: 0, Address: 236cd488
Operation: 0, Address: 999cd4ba
Operation: 0, Address: 286cd495
Operation: 1, Address: 236cd483
Operation: 1, Address: 123cd4b1
Operation: 2, Address: 871cd4a3
Operation: 3, Address: 236cd483
Operation: 1, Address: 223cd484
Operation: 8, Address: 223cd484

        Clear the cache to the initial state and reset the statistics
Operation: 0, Address: 245cd491
Operation: 9, Address: 245cd491

        ** KEY CACHE USAGE STATISTICS **

        -- DATA CACHE STATISTICS --
 number of Cache Reads:         1
 number of Cache Writes:        0
 number of Cache Hits:          0
 number of Cache Misses:        1
 Cache Hit Ratio:               0
 Cache Hit Ratio percentage:    0 %

 More information in valid line:
Line valid : 245cd491   |        Way : 0        |        Set :3352      |        State : V      |        LRU bit : 4    |        Tag :245

       There are 1 valid lines

 The cache instruction was not used/not operated on

        --- L1 Split Cache Anaylsis and Simulation Completed! ---
```