BLM32F40AXX

32-bit ARM Cortex-M4/M0+ MCU; 104 kB SRAM; 512 kB flash, 3 x I2C, 2 x SPI, 4 x USART, 32-bit counter/ timers, SCTimer/PWM, 12-bit 5.0 Msamples/sec ADC

Rev. 2.3 — 03 July 2018 Product data sheet

1. General description

The BLM32F40AXX are ARM Cortex-M4 based microcontrollers for embedded applications. These devices include an optional ARM Cortex-M0+ coprocessor, 104 kB of on-chip SRAM, up to 512 kB on-chip flash, five general-purpose timers, one State-Configurable Timer with PWM capabilities (SCTimer/PWM), one RTC/alarm timer, one 24-bit Multi-Rate Timer (MRT), a Repetitive Interrupt Timer (RIT), a Windowed Watchdog Timer (WWDT), four USARTs, two SPIs, three Fast-mode plus I^2C-bus interfaces with high-speed slave mode, and one 12-bit 5.0 Msamples/sec ADC.

The ARM Cortex-M4 is a 32-bit core that offers system enhancements such as low power consumption, enhanced debug features, and a high level of support block integration. The ARM Cortex-M4 CPU incorporates a 3-stage pipeline, uses a Harvard architecture with separate local instruction and data buses as well as a third bus for peripherals, and includes an internal prefetch unit that supports speculative branching. The ARM Cortex-M4 supports single-cycle digital signal processing and SIMD instructions. A hardware floating-point unit is integrated in the core.

The ARM Cortex-M0+ coprocessor is an energy-efficient and easy-to-use 32-bit core which is code and tool-compatible with the Cortex-M4 core. The Cortex-M0+ coprocessor offers up to 100 MHz performance with a simple instruction set and reduced code size. In BLM32F40AXX, the Cortex-M0 coprocessor hardware multiply is implemented as a 32-cycle iterative multiplier.

2. Features and benefits

- Dual processor cores: ARM Cortex-M4 and ARM Cortex-M0+. The M0+ core runs at the same frequency as the M4 core. Both cores operate up to a maximum frequency of 100 MHz.
- ARM Cortex-M4 core (version r0p1):
  - ARM Cortex-M4 processor, running at a frequency of up to 100 MHz, using the same clock as the Cortex-M4.
  - Floating Point Unit (FPU) and Memory Protection Unit (MPU).
  - ARM Cortex-M4 built-in Nested Vectored Interrupt Controller (NVIC).
  - Non-maskable Interrupt (NMI) input with a selection of sources.
  - Serial Wire Debug with eight breakpoints and four watch points. Includes Serial Wire Output for enhanced debug capabilities.
  - System tick timer.

- ARM Cortex-M0+ core (version r0p1):
  - ARM Cortex-M0+ processor, running at a frequency of up to 100 MHz.
  - ARM Cortex-M0+ built-in Nested Vectored Interrupt Controller (NVIC).
  - Non-maskable Interrupt (NMI) input with a selection of sources.
  - Serial Wire Debug with four breakpoints and two watch points.
  - System tick timer.
- On-chip memory:
  - Up to 512 kB on-chip flash program memory with flash accelerator and 256 byte page erase and write.
  - 104 kB total SRAM composed of:
  - Up to 96 kB contiguous main SRAM.
  - An additional 8 kB SRAM.
- ROM API support:
  - Flash In-Application Programming (IAP) and In-System Programming (ISP).
  - Power control API.
- Serial interfaces:
  - Four USART interfaces with synchronous mode and 32 kHz mode for wake-up from deep sleep and power down modes. The USARTs have FIFO support from the System FIFO and share a fractional baud-rate generator.
  - Two SPI interfaces, each with four slave selects and flexible data configuration. The SPIs have FIFO support from the System FIFO. The slave function is able to wake up the device from deep sleep and power down modes.
  - Three I^2C-bus interfaces supporting fast mode and Fast-mode Plus with data rates of up to 1Mbit/s and with multiple address recognition and monitor mode. Each I^2C-bus interface also supports High Speed Mode (3.4 Mbit/s) as a slave. The slave function is able to wake up the device from deep sleep and power down modes.
- Digital peripherals:
  - DMA controller with 22 channels and 20 programmable triggers, able to access all memories and DMA-capable peripherals.
  - Up to 50 General-Purpose Input/Output (GPIO) pins. Most GPIOs have configurable pull-up/pull-down resistors, programmable open-drain mode, and input inverter.
  - GPIO registers are located on the AHB for fast access. The DMA supports GPIO ports.
  - Up to eight GPIOs (pin interrupts) can be selected as edge-sensitive (rising or falling edges or both) interrupt requests or level-sensitive (active low or active high) interrupt requests. In addition, up to eight GPIOs can be selected to contribute a boolean expression and interrupt generation using the pattern match engine block.
  - Two GPIO grouped interrupts (GINT) enable an interrupt based on a logical (AND/OR) combination of input states.
  - CRC engine.
- Timers:
  - Five 32-bit standard general purpose timers/counters, four of which support up to 4 capture inputs and 4 compare outputs, PWM mode, and external count input. Specific timer events can be selected to generate DMA requests. The fifth timer does not have external pin connections and may be used for internal timing operations.

- One State Configurable Timer/PWM (SCT/PWM) with 8 inputs (6 external inputs and 2 internal inputs) and 8 output functions (including capture and match). Inputs and outputs can be routed to/from external pins and internally to/from selected peripherals. Internally, the SCT supports 13 captures/matches, 13 events and 13 states.
- 32-bit Real-time clock (RTC) with 1 s resolution running in the always-on power domain. A timer in the RTC can be used for wake-up from all low power modes including deep power-down, with 1 ms resolution.
- Multiple-channel multi-rate 24-bit timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
- Windowed Watchdog Timer (WWDT).
- Ultra-low power Micro-tick Timer, running from the Watchdog oscillator, that can be used to wake up the device from low power modes.
- Repetitive Interrupt Timer (RIT) for debug time-stamping and general-purpose use.

- Analog peripheral: 12-bit, 12-channel, Analog-to-Digital Converter (ADC) supporting 5.0 Msamples/s. The ADC supports two independent conversion sequences.
- Clock generation:
  - 12 MHz internal RC oscillator.
  - External clock input for clock frequencies of up to 25 MHz.
  - Internal low-power, watchdog oscillator (WDOSC) with a nominal frequency of 500 kHz.
  - 32 kHz low-power RTC oscillator.
  - System PLL allows CPU operation up to the maximum CPU rate. May be run from the internal RC oscillator, the external clock input CLKIN, or the RTC oscillator.
  - Clock output function for monitoring internal clocks.
  - Frequency measurement unit for measuring the frequency of any on-chip or off-chip clock signal.
- Power-saving modes and wake-up:
  - Integrated PMU (Power Management Unit) to minimize power consumption.
  - Reduced power modes: sleep, deep sleep, power down, and deep power-down.
  - Wake-up from deep sleep and power down modes via activity on the USART, SPI, and I^2C peripherals.
  - Wake-up from sleep, deep sleep, power down, and deep power-down modes using the RTC alarm.
- Single power supply 1.62 V to 3.6 V.
- Power-On Reset (POR).
- Brown-Out Detect (BOD) with separate thresholds for interrupt and forced reset.
- JTAG boundary scan supported.
- Unique device serial number (128 bit) for identification.
- Operating temperature range −40 °C to 105 °C.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
BLM32F40ACE	QFN48	body 6.0 x 6.0 x 0.85 mm	-
BLM32F40ARE	QFN64	body 9.0× 9.0 × 0.85 mm	-

3.1 Ordering options

Table 2. Ordering options

Type number	Device order part number	Flash/kB	Total SRAM/kB	Core M4 w/ FPU	Core M0+	GPIO
BLM32F40ACE	BLM32F40AJ512UK48Z	512	104	1	0	34
BLM32F40ARE	BLM32F40AJ512UK64Z	512	104	1	0	50

[1] All of the parts include five 32-bit general-purpose timers, one State-Configurable Timer with PWM capabilities (SCTimer/PWM), one RTC/alarm timer, one 24-bit Multi-Rate Timer (MRT), a Windowed Watchdog Timer (WWDT), four USARTs, two SPIs, three Fast-mode plus I2C-bus interfaces with high-speed slave mode, and one 12-bit 5.0 Msamples/sec ADC.

4. Marking

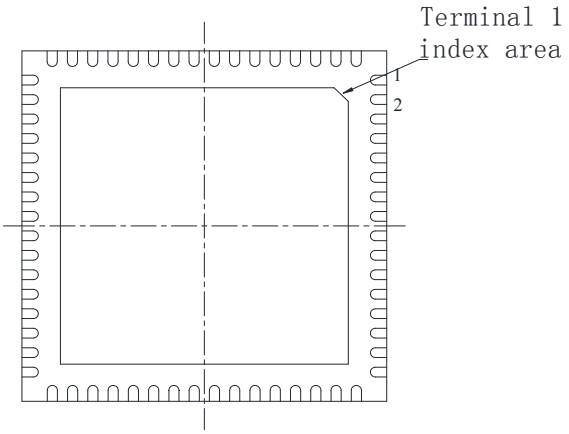


Fig 1. QFN64 package marking(bottom view)

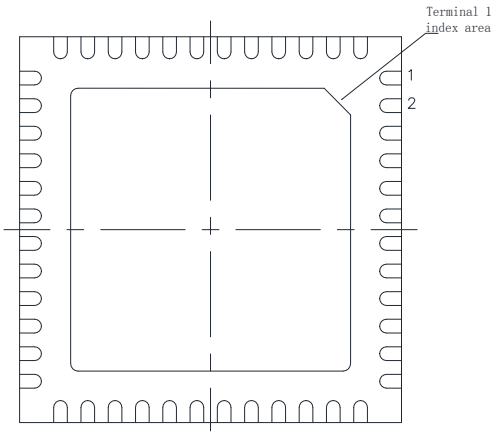


Fig 2. QFN48 package marking(bottom view)

The BLM32F40AXX QFN64 package has the following top-side marking:

- First line: BLM32F40AxxJyyy
  - yyy: flash size
- Second line: BD64
- Third line: xxxxxxxxxxxx
- Fourth line: xxxyywwx[R]z
  - yyww: Date code with yy = year and ww = week.
  - xR = boot code version and device revision.

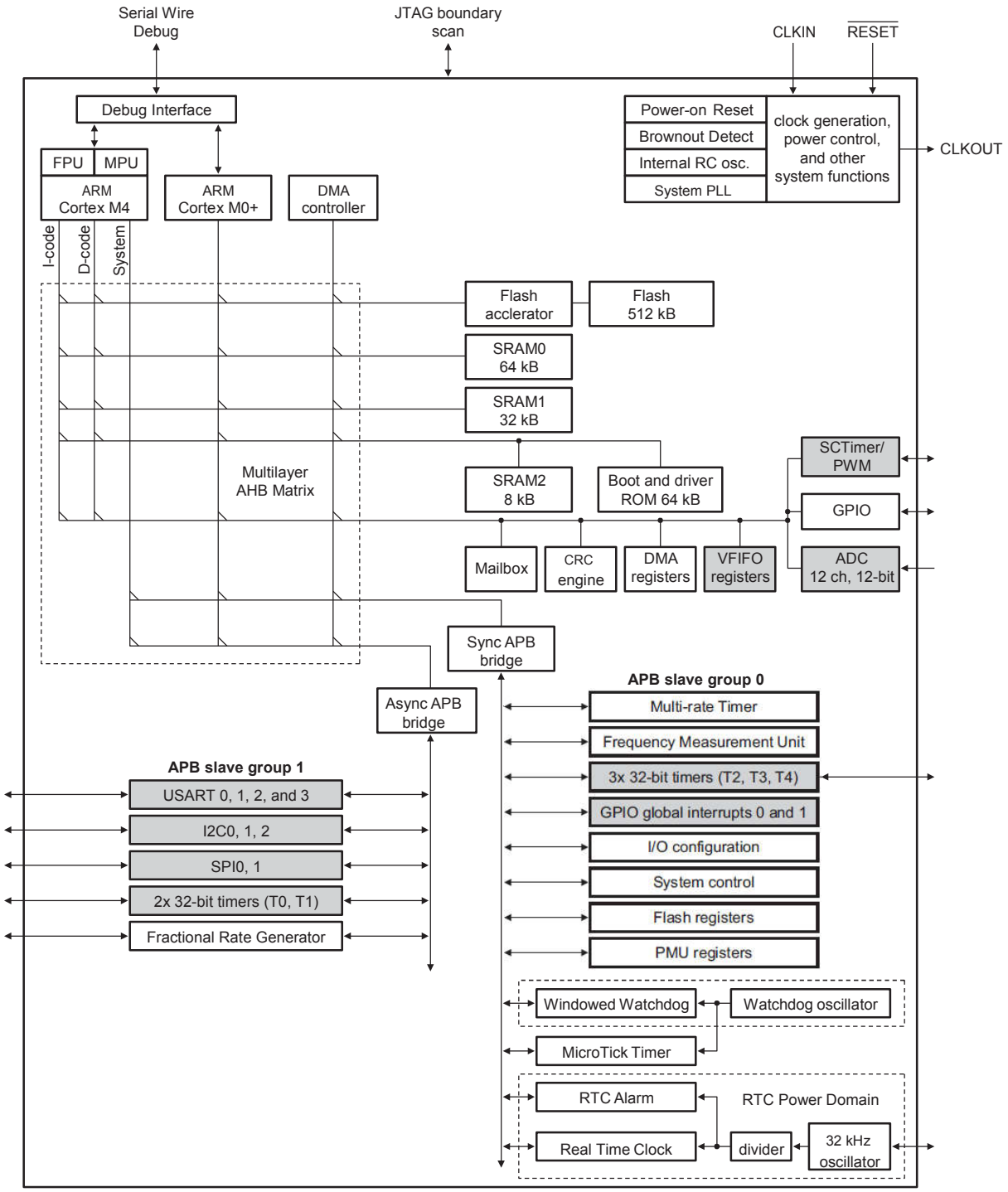
The BLM32F40AXX QFN48 package has the following top-side marking:

- First line: BLM32F40AXX
- Second line: JxxxUK48
  - xxx: flash size
- Third line: xxxxxxxx
- Fourth line: xxxyyww
  - yyww: Date code with yy = year and ww = week.
- Fifth line: xxxxx
- Sixth line: BTL x[R]z
  - xR = boot code version and device revision.

Table 3. Device revision table

Revision identifier (R)	Revision description
'1B'	Initial device revision with boot code version 17.1.
'1C'	Second device revision with boot code version 17.1.

5. Block diagram



Gray-shaded peripheral blocks provide dedicated request lines or triggers for DMA transfers.

Fig 3. BLM32F40AXX Block diagram

6. Pinning information

6.1 Pinning

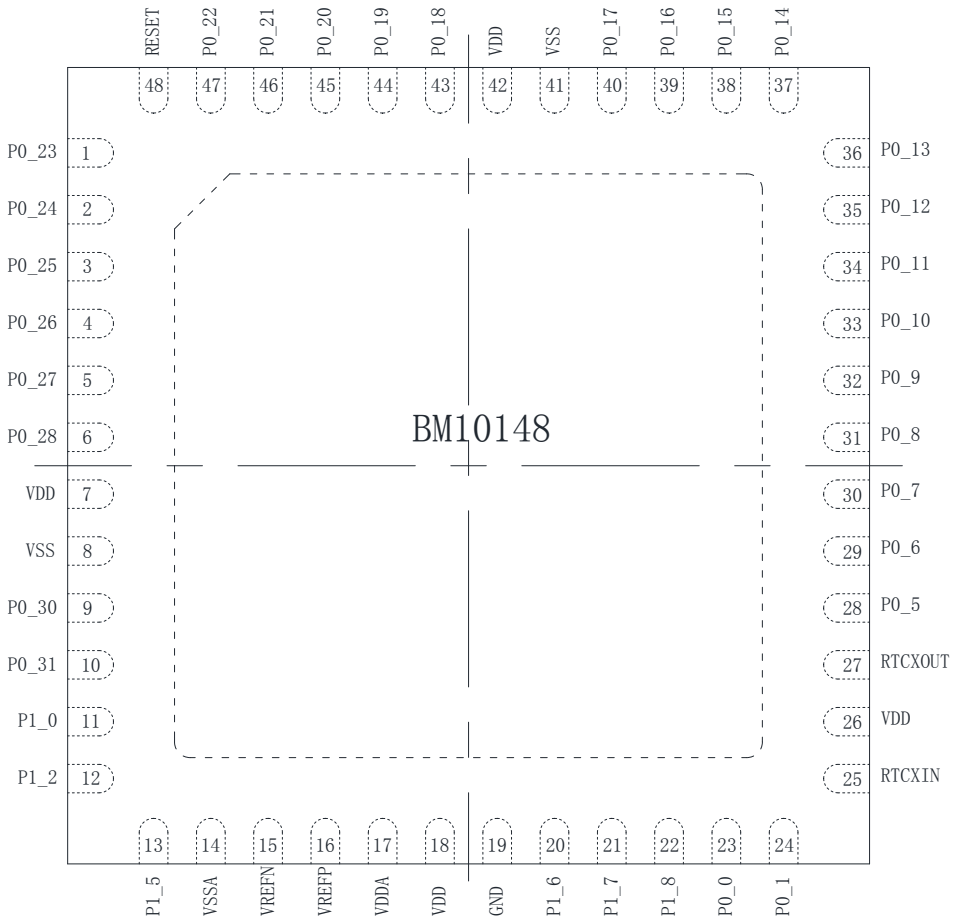


Fig 4. QFN48 Pin configuration (top view)

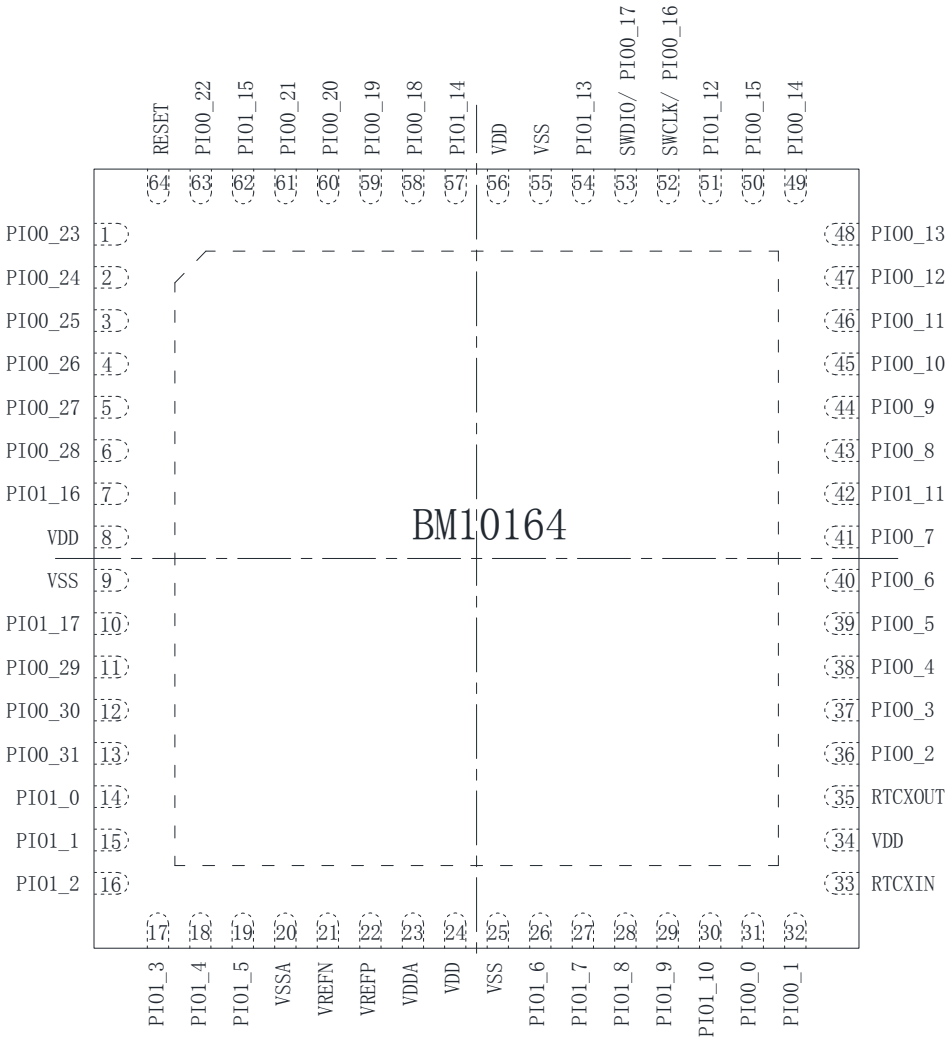


Fig 5. QFN64 Pin configuration (top view)

6.2 Pin description

On the BLM32F40AXX, digital pins are grouped into two ports. Each digital pin may support up to four different digital functions and one analog function, including General Purpose I/O (GPIO).

Table 4. Pin description

Symbol	QFN48	QFN64		Reset state [1]	Type [6]	Description
PIO0_0	23	31	[2]	PU	I/O	**PIO0_0 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is the UART0 RXD function.
					I	**U0_RXD —** Receiver input for USART0.
					I/O	**SPI0_SSEL0 —** Slave Select 0 for SPI0.
					I	**CT32B0_CAP0 —** 32-bit CT32B0 capture input 0.
					I	**R —** Reserved.
					O	**SCT0_OUT3 —** SCT0 output 3. PWM output 3.
PIO0_1	24	32	[2]	PU	I/O	**PIO0_1 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is the UART0 TXD function.
					O	**U0_TXD —** Transmitter output for USART0.
					I/O	**SPI0_SSEL1 —** Slave Select 1 for SPI0.
					I	**CT32B0_CAP1 —** 32-bit CT32B0 capture input 1.
					I	**R —** Reserved.
					O	**SCT0_OUT1 —** SCT0 output 1. PWM output 1.
PIO0_2	-	36	[2]	PU	I/O	**PIO0_2 —** General-purpose digital input/output pin.
					I	**U0_CTS —** Clear To Send input for USART0.
					I	**R —** Reserved.
					I	**CT32B2_CAP1 —** 32-bit CT32B2 capture input 1.
					I	**R —** Reserved.
PIO0_3	-	37	[2]	PU	I/O	**PIO0_3 —** General-purpose digital input/output pin.
					O	**U0_RTS —** Request To Send output for USART0.
					I	**R —** Reserved.
					O	**CT32B1_MAT3 —** 32-bit CT32B1 match output 3.
					I	**R —** Reserved.
PIO0_4	-	38	[2]	PU	I/O	**PIO0_4 —** General-purpose digital input/output pin.
					I/O	**U0_SCLK —** USART0 clock in synchronous USART mode.
					I/O	**SPI0_SSEL2 —** Slave Select 2 for SPI0.
					I	**CT32B0_CAP2 —** 32-bit CT32B0 capture input 2.
					I	**R —** Reserved.

Table 4. Pin description *...continued*

Symbol	QFN48	QFN64		Reset state [1]	Type [6]	Description
PIO0_5	28	39	[2]	PU	I/O	**PIO0_5 —** General-purpose digital input/output pin.
					I	**U1_RXD —** Receiver input for USART1.
					O	**SCT0_OUT6 —** SCT0 output 6. PWM output 6.
					O	**CT32B0_MAT0 —** 32-bit CT32B0 match output 0.
					I	**R —** Reserved.
PIO0_6	29	40	[2]	PU	I/O	**PIO0_6 —** General-purpose digital input/output pin.
					O	**U1_TXD —** Transmitter output for USART1.
					I	**R —** Reserved.
					O	**CT32B0_MAT1 —** 32-bit CT32B0 match output 1.
					I	**R —** Reserved.
PIO0_7	30	41	[2]	PU	I/O	**PIO0_7 —** General-purpose digital input/output pin.
					I/O	**U1_SCLK —** USART1 clock in synchronous USART mode.
					O	**SCT0_OUT0 —** SCT0 output 0. PWM output 0.
					O	**CT32B0_MAT2 —** 32-bit CT32B0 match output 2.
					I	**R —** Reserved.
					I	**CT32B0_CAP2 —** 32-bit CT32B0 capture input 2.
PIO0_8	31	43	[2]	PU	I/O	**PIO0_8 —** General-purpose digital input/output pin.
					I	**U2_RXD —** Receiver input for USART2.
					O	**SCT0_OUT1 —** SCT0 output 1. PWM output 1.
					O	**CT32B0_MAT3 —** 32-bit CT32B0 match output 3.
					I	**R —** Reserved.
PIO0_9	32	44	[2]	PU	I/O	**PIO0_9 —** General-purpose digital input/output pin.
					O	**U2_TXD —** Transmitter output for USART2.
					O	**SCT0_OUT2 —** SCT0 output 2. PWM output 2.
					I	**CT32B3_CAP0 —** 32-bit CT32B3 capture input 0.
					I	**R —** Reserved.
					I/O	**SPI0_SSEL0 —** Slave Select 0 for SPI0.
PIO0_10	33	45	[2]	PU	I/O	**PIO0_10 —** General-purpose digital input/output pin.
					I/O	**U2_SCLK —** USART2 clock in synchronous USART mode.
					O	**SCT0_OUT3 —** SCT0 output 3. PWM output 3.
					O	**CT32B3_MAT0 —** 32-bit CT32B3 match output 0.
					I	**R —** Reserved.
PIO0_11	34	46	[2]	PU	I/O	**PIO0_11 —** General-purpose digital input/output pin.
					I/O	**SPI0_SCK —** Serial clock for SPI0.
					I	**U1_RXD —** Receiver input for USART1.
					O	**CT32B2_MAT1 —** 32-bit CT32B2 match output 1.
					I	**R —** Reserved.

Table 4. Pin description *...continued*

Symbol	QFN48	QFN 64		Reset state [1]	Type [6]	Description
PIO0_12	35	47	[2]	PU	I/O	**PIO0_12 —** General-purpose digital input/output pin.
					I/O	**SPI0_MOSI —** Master Out Slave in for SPI0.
					O	**U1_TXD —** Transmitter output for USART1.
					O	**CT32B2_MAT3 —** 32-bit CT32B2 match output 3.
					I	**R —** Reserved.
PIO0_13	36	48	[2]	PU	I/O	**PIO0_13 —** General-purpose digital input/output pin.
					I/O	**SPI0_MISO —** Master In Slave Out for SPI0.
					O	**SCT0_OUT4 —** SCT0 output 4. PWM output 4.
					O	**CT32B2_MAT0 —** 32-bit CT32B2 match output 0.
					I	**R —** Reserved.
PIO0_14/TCK	37	49	[2]	PU	I/O	**PIO0_14 —** General-purpose digital input/output pin. In boundary scan mode: TCK (Test Clock).
					I/O	**SPI0_SSEL0 —** Slave Select 0 for SPI0.
					O	**SCT0_OUT5 —** SCT0 output 5. PWM output 5.
					O	**CT32B2_MAT1 —** 32-bit CT32B2 match output 1.
					I	**R —** Reserved.
PIO0_15/TDO	38	50	[2]	PU	I/O	**PIO0_15 —** General-purpose digital input/output pin. In boundary scan mode: TDO (Test Data Out).
					I/O	**SPI0_SSEL1 —** Slave Select 1 for SPI0.
					I/O	**SWO —** Serial wire trace output.
					O	**CT32B2_MAT2 —** 32-bit CT32B2 match output 2.
					I	**R —** Reserved.
SWCLK/ PIO0_16	39	52	[2]	PU	I/O	**PIO0_16 —** General-purpose digital input/output pin. After booting, this pin is connected to the SWCLK.
					I/O	**SPI0_SSEL2 —** Slave Select 2 for SPI0.
					I	**U1_CTS —** Clear To Send input for USART1.
					O	**CT32B3_MAT1 —** 32-bit CT32B3 match output 1.
					I	**R —** Reserved.
					I/O	**SWCLK —** Serial Wire Clock. This is the default function after booting.
SWDIO/ PIO0_17	40	53	[2]	PU	I/O	**PIO0_17 —** General-purpose digital input/output pin. After booting, this pin is connected to SWDIO.
					I/O	**SPI0_SSEL3 —** Slave Select 3 for SPI0.
					O	**U1_RTS —** Request To Send output for USART1.
					O	**CT32B3_MAT2 —** 32-bit CT32B3 match output 2.
					I	**R —** Reserved.
					I/O	**SWDIO —** Serial Wire Debug I/O. This is the default function after booting.

Table 4. Pin description *…continued*

Symbol	QFN48	QFN 64		Reset state [1]	Type [6]	Description
PIO0_18/TRST	43	58	[2]	PU	I/O	**PIO0_18 —** General-purpose digital input/output pin. In boundary scan mode: TRST (Test Reset).
					O	**U3_TXD —** Transmitter output for USART3.
					O	**SCT0_OUT0 —** SCT0 output 0. PWM output 0.
					O	**CT32B0_MAT0 —** 32-bit CT32B0 match output 0.
					I	**R —** Reserved.
PIO0_19/TDI	44	59	[2]	PU	I/O	**PIO0_19 —** General-purpose digital input/output pin. In boundary scan mode: TDI (Test Data In).
					I/O	**U3_SCLK —** USART3 clock in synchronous USART mode.
					O	**SCT0_OUT1 —** SCT0 output 1. PWM output 1.
					O	**CT32B0_MAT1 —** 32-bit CT32B0 match output 1.
					I	**R —** Reserved.
PIO0_20/TMS	45	60	[2]	PU	I/O	**PIO0_20 —** General-purpose digital input/output pin. In boundary scan mode: TMS (Test Mode Select).
					I	**U3_RXD —** Receiver input for USART3.
					I/O	**U0_SCLK —** USART0 clock in synchronous USART mode.
					I	**CT32B3_CAP0 —** 32-bit CT32B3 capture input 0.
					I	**R —** Reserved.
PIO0_21	46	61	[2]	PU	I/O	**PIO0_21 —** General-purpose digital input/output pin.
					O	**CLKOUT —** Clock output pin.
					O	**U0_TXD —** Transmitter output for USART0.
					O	**CT32B3_MAT0 —** 32-bit CT32B3 match output 0.
					I	**R —** Reserved.
PIO0_22	47	63	[2]	PU	I/O	**PIO0_22 —** General-purpose digital input/output pin.
					I	**CLKIN —** Clock input.
					I	**U0_RXD —** Receiver input for USART0.
					O	**CT32B3_MAT3 —** 32-bit CT32B3 match output 3.
					I	**R —** Reserved.
PIO0_23	1	1	[3]	Z	I/O	**PIO0_23 —** General-purpose digital input/output pin.
					I/O	**I2C0_SCL —** I^2C0 clock input/output.
					I	**R —** Reserved.
					I	**CT32B0_CAP0 —** 32-bit CT32B0 capture input 0.
					I	**R —** Reserved.

Table 4. Pin description *…continued*

Symbol	QFN48	QFN 64		Reset state [1]	Type [6]	Description
PIO0_24	2	2	[3]	Z	I/O	**PIO0_24 —** General-purpose digital input/output pin.
					I/O	**I2C0_SDA —** I^2C0 data input/output.
					I	**R —** Reserved.
					I	**CT32B0_CAP1 —** 32-bit CT32B0 capture input 1.
					I	**R —** Reserved.
					O	**CT32B0_MAT0 —** 32-bit CT32B0 match output 0.
PIO0_25	3	3	[3]	Z	I/O	**PIO0_25 —** General-purpose digital input/output pin.
					I/O	**I2C1_SCL —** I^2C1 clock input/output.
					I	**U1_CTS —** Clear To Send input for USART1.
					I	**CT32B0_CAP2 —** 32-bit CT32B0 capture input 2.
					I	**R —** Reserved.
					I	**CT32B1_CAP1 —** 32-bit CT32B1 capture input 1.
PIO0_26	4	4	[3]	Z	I/O	**PIO0_26 —** General-purpose digital input/output pin.
					I/O	**I2C1_SDA —** I^2C1 data input/output.
					I	**R —** Reserved.
					I	**CT32B0_CAP3 —** 32-bit CT32B0 capture input 3.
					I	**R —** Reserved.
PIO0_27	5	5	[3]	Z	I/O	**PIO0_27 —** General-purpose digital input/output pin.
					I/O	**I2C2_SCL —** I^2C2 clock input/output.
					I	**R —** Reserved.
					I	**CT32B2_CAP0 —** 32-bit CT32B2 capture input 0.
					I	**R —** Reserved.
PIO0_28	6	6	[3]	Z	I/O	**PIO0_28 —** General-purpose digital input/output pin.
					I/O	**I2C2_SDA —** I^2C2 data input/output.
					I	**R —** Reserved.
					O	**CT32B2_MAT0 —** 32-bit CT32B2 match output 0.
					I	**R —** Reserved.
PIO0_29/ ADC0_0	-	11	[4]	PU	I/O; AI	**PIO0_29/ADC0_0 —** General-purpose digital input/output pin (default). ADC input channel 0 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					O	**SCT0_OUT2 —** SCT0 output 2.
					O	**CT32B0_MAT3 —** 32-bit CT32B0 match output 3.
					I	**R —** Reserved.
					I	**CT32B0_CAP1 —** 32-bit CT32B0 capture input 1.
					O	**CT32B0_MAT1 —** 32-bit CT32B0 match output 1.

Table 4. Pin description *…continued*

Symbol	QFN48	QFN 64		Reset state [1]	Type [6]	Description
PIO0_30/ ADC0_1	9	12	[4]	PU	I/O; AI	**PIO0_30/ADC0_1 —** General-purpose digital input/output pin (default). ADC input channel 1 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					O	**SCT0_OUT3 —** SCT0 output 3.
					O	**CT32B0_MAT2 —** 32-bit CT32B0 match output 2.
					I	**R —** Reserved.
					I	**CT32B0_CAP2 —** 32-bit CT32B0 capture input 2.
PIO0_31/ ADC0_2	10	13	[4]	PU	I/O; AI	**PIO0_31/ADC0_2 —** General-purpose digital input/output pin (default). ADC input channel 2 if the DIGIMODE bit is set to 0 in the IOCON register for this pin. **Remark:** This pin is also used to force In-System Programming mode (ISP) after device reset. See the BLM32F40AXX User Manual (Boot Process chapter) for
					-	**R —** Reserved.
					I	**U2_CTS —** Clear To Send input for USART2.
					I	**CT32B2_CAP2 —** 32-bit CT32B2 capture input 2.
					I	**R —** Reserved.
					I	**CT32B0_CAP3 —** 32-bit CT32B0 capture input 3.
					O	**CT32B0_MAT3 —** 32-bit CT32B0 match output 3.
PIO1_0/ ADC0_3	11	14	[4]	PU	I/O; AI	**PIO1_0/ADC0_3 —** General-purpose digital input/output pin (default). ADC input channel 3 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					O	**U2_RTS —** Request To Send output for USART2.
					O	**CT32B3_MAT1 —** 32-bit CT32B3 match output 1.
					I	**R —** Reserved.
					I	**CT32B0_CAP0 —** 32-bit CT32B0 capture input 0.
PIO1_1/ ADC0_4	-	15	[4]	PU	I/O; AI	**PIO1_1/ADC0_4 —** General-purpose digital input/output pin (default). ADC input channel 4 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SWO —** Serial wire trace output.
					O	**SCT0_OUT4 —** SCT0 output 4.
PIO1_2/ ADC0_5	12	16	[4]	PU	I/O; AI	**PIO1_2/ADC0_5 —** General-purpose digital input/output pin (default). ADC input channel 5 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_SSEL3 —** Slave Select 3 for SPI1.
					O	**SCT0_OUT5 —** SCT0 output 5.

Table 4. Pin description *…continued*

Symbol	QFN48	QFN 64		Reset state [1]	Type [6]	Description
PIO1_3/ ADC0_6	-	17	[4]	PU	I/O; AI	**PIO1_3/ADC0_6 —** General-purpose digital input/output pin (default). ADC input channel 6 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_SSEL2 —** Slave Select 2 for SPI1.
					O	**SCT0_OUT6 —** SCT0 output 6.
					I	**R —** Reserved.
					I/O	**SPI0_SCK —** Serial clock for SPI0.
					I	**CT32B0_CAP1 —** 32-bit CT32B0 capture input 1.
PIO1_4/ ADC0_7	-	18	[4]	PU	I/O; AI	**PIO1_4/ADC0_7 —** General-purpose digital input/output pin (default). ADC input channel 7 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_SSEL1 —** Slave Select 1 for SPI1.
					O	**SCT0_OUT7 —** SCT0 output 7.
					I	**R —** Reserved.
					I/O	**SPI0_MISO —** Master In Slave Out for SPI0.
					O	**CT32B0_MAT1 —** 32-bit CT32B0 match output 1.
PIO1_5/ ADC0_8	13	19	[4]	PU	I/O; AI	**PIO1_5/ADC0_8 —** General-purpose digital input/output pin (default). ADC input channel 8 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_SSEL0 —** Slave Select 0 for SPI1.
					I	**CT32B1_CAP0 —** 32-bit CT32B1 capture input 0.
					I	**R —** Reserved.
					O	**CT32B1_MAT3 —** 32-bit CT32B1 match output 3.
					I	**R —** Reserved.
PIO1_6/ ADC0_9	20	26	[4]	PU	I/O; AI	**PIO1_6/ADC0_9 —** General-purpose digital input/output pin (default). ADC input channel 9 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_SCK —** Serial clock for SPI1.
					I	**CT32B1_CAP2 —** 32-bit CT32B1 capture input 2.
					-	**R —** Reserved.
					O	**CT32B1_MAT2 —** 32-bit CT32B1 match output 2.
					I	**R —** Reserved.

Table 4. Pin description *...continued*

Symbol	QFN48	QFN 64		Reset state [1]	Type [6]	Description
PIO1_7/ ADC0_10	21	27	[4]	PU	I/O; AI	**PIO1_7/ADC0_10 —** General-purpose digital input/output pin (default). ADC input channel 10 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_MOSI —** Master Out Slave in for SPI1.
					O	**CT32B1_MAT2 —** 32-bit CT32B1 match output 2.
					-	**R —** Reserved.
					I	**CT32B1_CAP2 —** 32-bit CT32B1 capture input 2.
					I	**R —** Reserved.
PIO1_8/ ADC0_11	22	28	[4]	PU	I/O; AI	**PIO1_8/ADC0_11 —** General-purpose digital input/output pin (default). ADC input channel 11 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_MISO —** Master In Slave Out for SPI1.
					O	**CT32B1_MAT3 —** 32-bit CT32B1 match output 3.
					I	**R —** Reserved.
					I	**CT32B1_CAP3 —** 32-bit CT32B1 capture input 3.
					I	**R —** Reserved.
PIO1_9	-	29	[2]	PU	I/O	**PIO1_9 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					I/O	**SPI0_MOSI —** Master Out Slave In for SPI0.
					I	**CT32B0_CAP2 —** 32-bit CT32B0 capture input 2.
PIO1_10	-	30	[2]	PU	I/O	**PIO1_10 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					O	**U1_TXD —** Transmitter output for USART1.
					O	**SCT0_OUT4 —** SCT0 output 4.
PIO1_11	-	42	[2]	PU	I/O	**PIO1_11 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					O	**U1_RTS —** Request To Send output for USART1.
					I	**CT32B1_CAP0 —** 32-bit CT32B1 capture input 0.
PIO1_12	-	51	[2]	PU	I/O	**PIO1_12 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					I	**U3_RXD —** Receiver input for USART3.
					O	**CT32B1_MAT0 —** 32-bit CT32B1 match output 0.
					I/O	**SPI1_SCK —** Serial clock for SPI1.
PIO1_13	-	54	[2]	PU	I/O	**PIO1_13 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					O	**U3_TXD —** Transmitter output for USART3.
					O	**CT32B1_MAT1 —** 32-bit CT32B1 match output 1.
					I/O	**SPI1_MOSI —** Master Out Slave In for SPI1.

Table 4. Pin description *...continued*

Symbol	QFN48	QFN 64		Reset state [1]	Type [6]	Description
PIO1_14	-	57	[2]	PU	I/O	**PIO1_14 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					I	**U2_RXD —** Receiver input for USART2.
					O	**SCT0_OUT7 —** SCT0 output 7.
					I/O	**SPI1_MISO —** Master In Slave Out for SPI1.
PIO1_15	-	62	[2]	PU	I/O	**PIO1_15 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					O	**SCT0_OUT5 —** SCT0 output 5.
					I	**CT32B1_CAP3 —** 32-bit CT32B1 capture input 3.
					I/O	**SPI1_SSEL0 —** Slave Select 0 for SPI1.
PIO1_16	-	7	[2]	PU	I/O	**PIO1_16 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					O	**CT32B0_MAT0 —** 32-bit CT32B0 match output 0.
					I	**CT32B0_CAP0 —** 32-bit CT32B0 capture input 0.
					I/O	**SPI1_SSEL1 —** Slave Select 1 for SPI1.
PIO1_17	-	10	[2]	PU	I/O	**PIO1_17 —** General-purpose digital input/output pin.
RESET	48	64	[5]	PU	I	External reset input: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. Wakes up the part from deep power-down mode.
RTCXIN	25	33		-	-	RTC oscillator input.
RTCXOUT	27	35		-	-	RTC oscillator output.
VREFP	16	22		-	-	ADC positive reference voltage.
VREFN	15	21		-	-	ADC negative reference voltage.
VDDA	17	23		-	-	Analog supply voltage.
VDD	7 18 26 42	8, 24, 56, 34		-	-	Single 1.62 V to 3.6 V power supply powers internal digital functions and I/Os.
VSS	8 19 41	9, 25, 55		-	-	Ground.
VSSA	14	20		-	-	Analog ground.

[1] PU = input mode, pull-up enabled (pull-up resistor pulls up pin to V_{DD}). Z = high impedance; pull-up or pull-down disabled. Reset state reflects the pin state at reset without boot code operation. For pin states in the different power modes, see Section 6.2.2 “Pin states in different power modes”. For termination on unused pins, see Section 6.2.1 “Termination of unused pins”.

[2] 5 V tolerant pad with programmable glitch filter (5 V tolerant if V_{DD} present; if V_{DD} not present, do not exceed 3.6 V); provides digital I/O functions with TTL levels and hysteresis; normal drive strength. See Figure 27. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 16 ns (simulated value).

[3] True open-drain pin. I2C-bus pins compliant with the I2C-bus specification for I2C standard mode, I2C Fast-mode, and I2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[4] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[5] Reset pad.5 V tolerant pad with glitch filter with hysteresis. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 20 ns (simulated value)

[6] I = Input; AI = Analog input; O = Output

6.2.1 Termination of unused pins

Table 5 shows how to terminate pins that are **not** used in the application. In many cases, unused pins should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as outputs set to LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin's IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 5. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
RESET	I; PU	The RESET pin can be left unconnected if the application does not use it.
all PIOn_m (not open-drain)	I; PU	Can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software.
PIOn_m (I2C open-drain)	IA	Can be left unconnected if driven LOW and configured as GPIO output by software.
RTCXIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
RTCXOUT	-	Can be left unconnected.
VREFP	-	Tie to VDD.
VREFN	-	Tie to VSS.
VDDA	-	Tie to VDD.
VSSA	-	Tie to VSS.

[1] I = Input, IA = Inactive (no pull-up/pull-down enabled), PU = Pull-Up.

6.2.2 Pin states in different power modes

Table 6. Pin states in different power modes

Pin	Active	Sleep	Deep sleep/Power down	Deep power-down
PIOn_m pins (not I2C)	As configured in the IOCON[1]. Default: internal pull-up enabled.			Floating.
PIO0_23 to PIO0_28 (open-drain I2C-bus pins)	As configured in the IOCON[1].			Floating.
RESET	Reset function enabled. Default: input, internal pull-up enabled. Reset function disabled.			

[1] Default and programmed pin states are retained in sleep, deep sleep, and power down modes.

7. Functional description

7.1 Architectural overview

The ARM Cortex-M4 includes three AHB-Lite buses, one system bus and the I-code and D-code buses. One bus is dedicated for instruction fetch (I-code), and one bus is dedicated for data access (D-code). The use of two core buses allows for simultaneous operations if concurrent operations target different devices.

A multi-layer AHB matrix connects the CPU buses and other bus masters to peripherals in a flexible manner that optimizes performance by allowing peripherals on different slaves ports of the matrix to be accessed simultaneously by different bus masters. Connections in the multilayer matrix are shown in Figure 3.

APB peripherals are connected to the AHB matrix via two APB buses using separate slave ports from the multilayer AHB matrix. This allows for better performance by reducing collisions between the CPU and the DMA controller, and also for peripherals on the asynchronous bridge to have a fixed clock that does not track the system clock.

7.2 ARM Cortex-M4 processor

The ARM Cortex-M4 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption. The ARM Cortex-M4 offers many new features, including a Thumb-2 instruction set, low interrupt latency, hardware multiply and divide, interruptable/continuable multiple load and store instructions, automatic state save and restore for interrupts, tightly integrated interrupt controller with wake-up interrupt controller, and multiple core buses capable of simultaneous accesses.

A 3-stage pipeline is employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

7.3 ARM Cortex-M4 integrated Floating Point Unit (FPU)

The FPU fully supports single-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations. It also provides conversions between fixed-point and floating-point data formats, and floating-point constant instructions.

The FPU provides floating-point computation functionality that is compliant with the ANSI/IEEE Std 754-2008, IEEE Standard for Binary Floating-Point Arithmetic, referred to as the IEEE 754 standard.

7.4 Memory Protection Unit (MPU)

The Cortex-M4 includes a Memory Protection Unit (MPU) which can be used to improve the reliability of an embedded system by protecting critical data within the user application.

The MPU allows separating processing tasks by disallowing access to each other's data, disabling access to memory regions, allowing memory regions to be defined as read-only and detecting unexpected memory accesses that could potentially break the system.

The MPU separates the memory into distinct regions and implements protection by preventing disallowed accesses. The MPU supports up to eight regions each of which can be divided into eight subregions. Accesses to memory locations that are not defined in the MPU regions, or not permitted by the region setting, will cause the Memory Management Fault exception to take place.

7.5 Nested Vectored Interrupt Controller (NVIC) for Cortex-M4

The NVIC is an integral part of the Cortex-M4. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.5.1 Features

- Controls system exceptions and peripheral interrupts.
- 37 vectored interrupts.
- Eight programmable interrupt priority levels, with hardware priority level masking.
- Relocatable vector table.
- Non-Maskable Interrupt (NMI).
- Software interrupt generation.

7.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags.

7.6 ARM Cortex-M0+ co-processor

The ARM Cortex-M0+ co-processor offers high performance and very low power consumption. This processor uses a 2-stage pipeline von Neumann architecture and a small but powerful instruction set providing high-end processing hardware. The processor includes an NVIC with 32 interrupts and a separate system tick timer. In BLM32F40AXX, the Cortex-M0 coprocessor hardware multiply is implemented as a 32-cycle iterative multiplier.

7.7 Nested Vectored Interrupt Controller (NVIC) for Cortex-M0+

The NVIC is an integral part of the Cortex-M0+. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.7.1 Features

- Controls system exceptions and peripheral interrupts.
- 32 vectored interrupts.
- Four programmable interrupt priority levels, with hardware priority level masking.
- Relocatable vector table.
- Non-Maskable Interrupt (NMI).
- Software interrupt generation.

7.7.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags.

7.8 System Tick timer (SysTick)

The ARM Cortex-M4 and ARM Cortex-M0+ cores include a system tick timer (SysTick) that is intended to generate a dedicated SYSTICK exception. The clock source for the SysTick can be the system clock or the SYSTICK clock.

7.9 On-chip static RAM

The BLM32F40AXX support 104 kB SRAM with separate bus master access for higher throughput and individual power control for low-power operation.

7.10 On-chip flash

The BLM32F40AXX supports 512 kB of on-chip flash memory.

7.11 On-chip ROM

The 64 kB on-chip ROM contains the boot loader and the following Application Programming Interfaces (API):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash programming.
- Power control API for configuring power consumption and PLL settings.

7.12 Memory mapping

The BLM32F40AXX incorporates several distinct memory regions. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals.Each peripheral is allocated 16 kB of space simplifying the address decoding. The registers incorporated into the CPU, such as NVIC, SysTick, and sleep mode control, are located on the private peripheral bus.

Figure 6 shows the overall map of the entire address space from the user program viewpoint following reset.

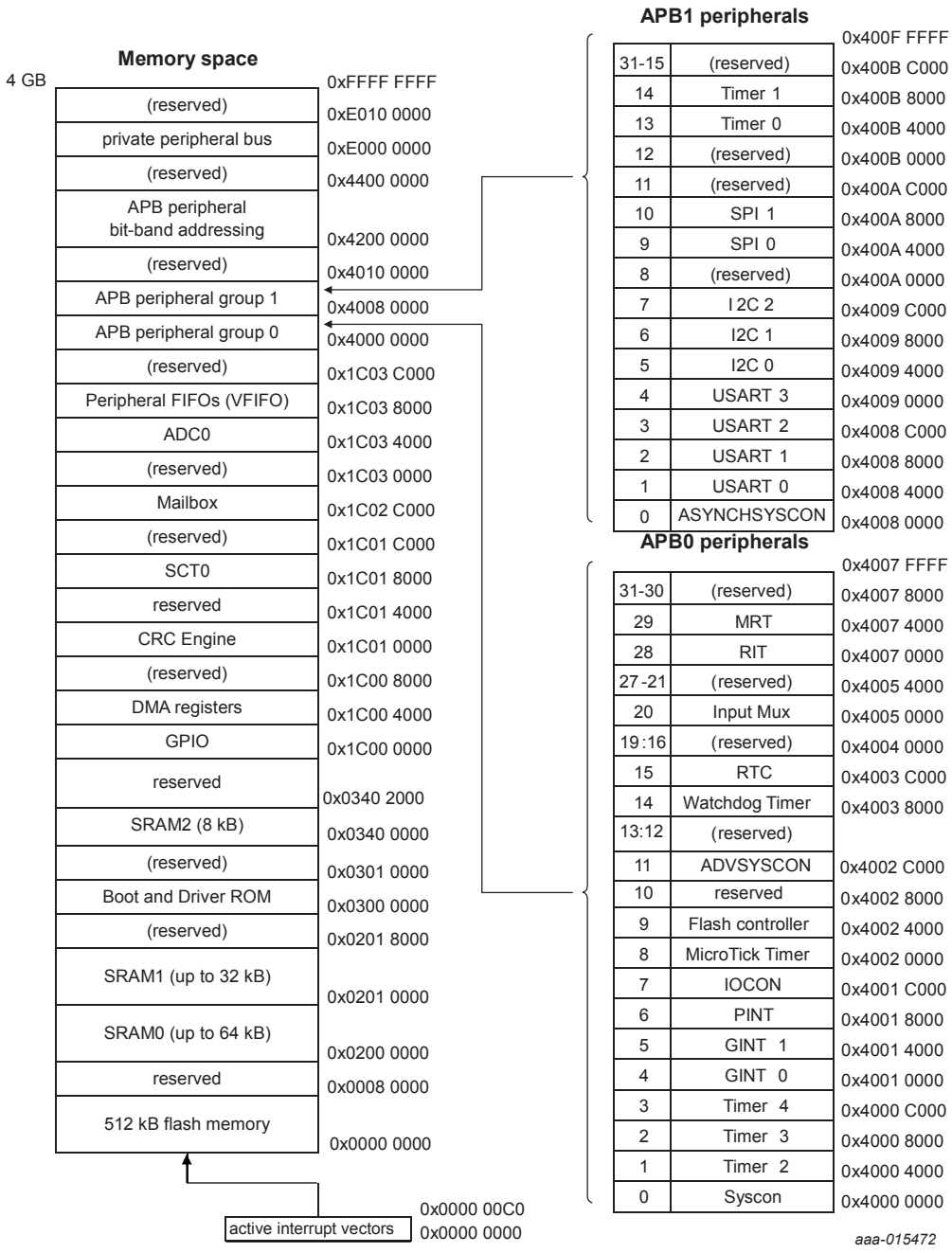


Fig 6. BLM32F40AXX Memory

7.13 General Purpose I/O (GPIO)

The BLM32F40AXX provides two GPIO ports with a total of 50 GPIO pins.

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The current level of a port pin can be read back no matter what peripheral is selected for that pin.

See Table 4 for the default state on reset.

7.13.1 Features

- Accelerated GPIO functions:
  - GPIO registers are located on the AHB so that the fastest possible I/O timing can be achieved.
  - Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
  - All GPIO registers are byte and half-word addressable.
  - Entire port value can be written in one instruction.
- Bit-level set, clear and toggle registers allow a single instruction set, clear or toggle of any number of bits in one port.
- Direction control of individual bits.
- All I/O default to inputs after reset.
- All GPIO pins can be selected to create an edge or level-sensitive GPIO interrupt request.
- One GPIO group interrupt can be triggered by a combination of any pin or pins.

7.14 Pin interrupt/pattern engine

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC. The pattern match engine can be used in conjunction with software to create complex state machines based on pin inputs. Any digital pin, independent of the function selected through the switch matrix can be configured through the SYSCON block as an input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are located on the I/O+ bus for fast single-cycle access.

7.14.1 Features

- Pin interrupts:
  - Up to eight pins can be selected from all GPIO pins on ports 0 and 1 as edge-sensitive or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
  - Level-sensitive interrupt pins can be HIGH-active or LOW-active.
  - Level-sensitive interrupt pins can be HIGH-active or LOW-active.
  - Pin interrupts can wake up the device from sleep mode, deep sleep mode, and power down mode.

- Pattern match engine:
  - Up to eight pins can be selected from all digital pins on ports 0 and 1 to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each bit slice minterm (product term) comprising of the specified boolean expression can generate its own, dedicated interrupt request.
  - Any occurrence of a pattern match can also be programmed to generate an RXEV notification to the CPU. The RXEV signal can be connected to a pin.
  - Pattern match can be used in conjunction with software to create complex state machines based on pin inputs.
  - Pattern match engine facilities wake-up only from active and sleep modes.

7.15 AHB peripherals

7.15.1 DMA controller

The DMA controller allows peripheral-to memory, memory-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional DMA transfers for a single source and destination.

7.15.1.1 Features

- 22 channels, 21 of which are connected to peripheral DMA requests. These come from the USART, SPI, and I^2C peripherals. One spare channels has no DMA request connected, and can be used for functions such as memory-to-memory moves.
- DMA operations can be triggered by on- or off-chip events. Each DMA channel can select one trigger input from 20 sources. Trigger sources include ADC interrupts, Timer interrupts, pin interrupts, and the SCT DMA request lines.
- Priority is user selectable for each channel.
- Continuous priority arbitration.
- Address cache.
- Efficient use of data bus.
- Supports single transfers up to 1,024 words.
- Address increment options allow packing and/or unpacking data.

7.16 Digital serial peripherals

7.16.1 USART

7.16.1.1 Features

- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Maximum bit rates of 6.25 Mbit/s in asynchronous mode.
- Maximum supported bit rate of 24 Mbit/s for USART master and slave synchronous modes.
- 7, 8, or 9 data bits and 1 or 2 stop bits.

- Multiprocessor/multidrop (9-bit) mode with software address compare.
- RS-485 transceiver output enable.
- Autobaud mode for automatic baud rate detection
- Parity generation and checking: odd, even, or none.
- Software selectable oversampling from 5 to 16 clocks in asynchronous mode.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.
- FIFO support from the System FIFO.
- Received data and status can optionally be read from a single register
- Break generation and detection.
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator with auto-baud function.
- A fractional rate divider is shared among all USARTs.
- Interrupts available for Receiver Ready, Transmitter Ready, Receiver Idle, change in receiver break detect, Framing error, Parity error, Overrun, Underrun, Delta CTS detect, and receiver sample noise detected.
- Loopback mode for testing of data and flow control.
- In synchronous slave mode, wakes up the part from deep sleep and power down modes.
- Special operating mode allows operation at up to 9600 baud using the 32 kHz RTC oscillator as the UART clock. This mode can be used while the device is in deep sleep or power down mode and can wake-up the device when a character is received.
- USART transmit and receive functions work with the system DMA controller.
- Activity on the USART synchronous slave mode allows wake-up from deep sleep and power down modes on any enabled interrupt.

7.16.2 SPI serial I/O controller

7.16.2.1 Features

- Master and slave operation.
- Maximum supported bit rate for SPI master mode is 71 Mbit/s, and the maximum supported bit rate for SPI slave mode is 21 Mbit/s.
- Data frames of 1 to 16 bits supported directly. Larger frames supported by software or DMA set-up.
- Data can be transmitted to a slave without the need to read incoming data. This can be useful while setting up an SPI memory.
- Control information can optionally be written along with data. This allows very versatile operation, including “any length” frames.
- Up to four Slave Select input/outputs with selectable polarity and flexible usage.
- Supports DMA transfers: SPIn transmit and receive functions can operated with the system DMA controller.

- FIFO support from the System FIFO.
- Activity on the SPI in slave mode allows wake-up from deep sleep and power down modes on any enabled interrupt.

7.17 I²C-bus interface

The I²C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (for example, an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I²C is a multi-master bus and can be controlled by more than one bus master connected to it.

7.17.1 Features

- All I²Cs support standard (up to 100 Kbits/s), fast mode (up to 400 Kbits/s), and Fast-mode Plus (up to 1 Mbit/s).
- All I²Cs support high-speed slave mode with data rates of up to 3.4 Mbit/s.
- Independent Master, Slave, and Monitor functions.
- Supports both Multi-master and Multi-master with Slave functions.
- Multiple I²C slave addresses supported in hardware.
- One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I²C-bus addresses.
- 10-bit addressing supported with software assist.
- Supports System Management Bus (SMBus).
- No chip clocks are required in order to receive and compare an address as a Slave, so this event can wake up the device from power down mode.
- Supports the I²C-bus specification up to Fast-mode Plus (FM+, up to 1 MHz) in both master and slave modes. High-speed (HS, up to 3.4 MHz) I²C is support in slave mode only.
- Activity on the I²C in slave mode allows wake-up from deep sleep and power down modes on any enabled interrupt.

7.18 Counter/timers

7.18.1 General-purpose 32-bit timers/external event counter

The BLM32F40AXX includes five general-purpose 32-bit timer/counters.

The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.18.1.1 Features

- Each is a 32-bit counter/timer with a programmable 32-bit prescaler. Four of the timers include external capture and match pin connections.

- Counter or timer operation.
- For each timer with pin connections, up to 4 32-bit capture channels that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse-width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- For each timer with pin connections, up to 4 external outputs corresponding to match registers with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- PWM: for each timer with pin connections, up to 3 match outputs can be used as single edge controlled PWM outputs.

7.18.2 State Configurable Timer/PWM (SCTimer/PWM)

The SCTimer/PWM (SCT0) allows a wide variety of timing, counting, output modulation, and input capture operations. The inputs and outputs of the SCTimer/PWM are shared with the capture and match inputs/outputs of the 32-bit general-purpose counter/timers.

The SCTimer/PWM can be configured as two 16-bit counters or a unified 32-bit counter. In the two-counter case, in addition to the counter value the following operational elements are independent for each half:

- State variable
- Limit, halt, stop, and start conditions
- Values of Match/Capture registers, plus reload or capture control values

In the two-counter case, the following operational elements are global to the SCT, but the last three can use match conditions from either counter:

- Clock selection
- Inputs
- Events
- Outputs
- Interrupts

7.18.2.1 Features

- Two 16-bit counters or one 32-bit counter.
- Counter(s) clocked by bus clock or selected input.
- Up counter(s) or up-down counter(s).
- State variable allows sequencing across multiple counter cycles.
- Event combines input or output condition and/or counter match in a specified state.
- Events control outputs, interrupts, and the SCT states.
  - Match register 0 can be used as an automatic limit.
  - In bi-directional mode, events can be enabled based on the count direction.
  - Match events can be held until another qualifying event occurs.
- Selected event(s) can limit, halt, start, or stop a counter.
- Supports:
  - 8 inputs (6 GPIO pins, ADC0_THCMP_IRQ, DEBUG_HALTED)
  - up to 8 outputs
  - 13 match/capture registers
  - 13 events
  - 13 states
- PWM capabilities including dead time and emergency abort functions

7.18.3 Windowed WatchDog Timer (WWDT)

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

7.18.3.1 Features

- Internally resets chip if not reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time-out period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Programmable 24-bit timer with internal fixed pre-scaler.
- Selectable time period from 1,024 watchdog clocks ($T_{WDCLK} \times 256 \times 4$) to over 67 million watchdog clocks ($T_{WDCLK} \times 2^{24} \times 4$) in increments of 4 watchdog clocks.
- “Safe” watchdog operation. Once enabled, requires a hardware reset or a Watchdog reset to be disabled.
- Incorrect feed sequence causes immediate watchdog event if enabled.
- The watchdog reload value can optionally be protected such that it can only be changed after the “warning interrupt” time is reached.
- Flag to indicate Watchdog reset.
- The Watchdog clock (WDCLK) source is the fixed 500 kHz clock (+/- 40%) provided by the low-power watchdog oscillator.
- The Watchdog timer can be configured to run in deep sleep or power down mode.

- Debug mode.

7.18.4 RTC timer

The RTC block has two timers: main RTC timer, and high-resolution/wake-up timer. The main RTC timer is a 32-bit timer that uses a 1 Hz clock and is intended to run continuously as a real-time clock. When the timer value reaches a match value, an interrupt is raised. The alarm interrupt can also wake up the part from any low power mode, if enabled.

The high-resolution or wake-up timer is a 16-bit timer that uses a 1 kHz clock and operates as a one-shot down timer. When the timer is loaded, it starts counting down to 0 at which point an interrupt is raised. The interrupt can wake up the part from any low power mode, if enabled. This timer is intended to be used for timed wake-up from deep sleep, power down, or deep power-down modes. The high-resolution wake-up timer can be disabled to conserve power if not used.

The RTC timer uses the 32 kHz clock input to create a 1 Hz or 1 kHz clock

7.18.4.1 Features

- The RTC oscillator has the following clock outputs:
  - 32 kHz clock, selectable for system clock and CLKOUT pin.
  - 1 Hz clock for RTC timing.
  - 1 kHz clock for high-resolution RTC timing.
- 32-bit, 1 Hz RTC counter and associated match register for alarm generation.
- Separate 16-bit high-resolution/wake-up timer clocked at 1 kHz for 1 ms resolution with a more that one minute maximum time-out period.
- RTC alarm and high-resolution/wake-up timer time-out each generate independent interrupt requests. Either time-out can wake up the part from any of the low power modes, including deep power-down.

7.18.5 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

7.18.5.1 Features

- 24-bit interrupt timer.
- Four channels independently counting down from individually set values.
- Repeat interrupt, one-shot interrupt, and one-shot bus stall modes.

7.18.6 Repetitive Interrupt Timer (RIT)

The Repetitive Interrupt Timer provides a versatile means of generating interrupts at specified time intervals, without using a standard timer. It is intended for repeating interrupts that are not related to Operating System interrupts. However, it could be used as an alternative to the System Tick Timer if there are different system requirements.

7.18.6.1 Features

- 48-bit counter running from the main clock. Counter can be free-running or be reset by a generated interrupt.
- 48-bit compare value.
- 48-bit compare mask. An interrupt is generated when the counter value equals the compare value, after masking. This allows for combinations not possible with a simple compare.

7.18.7 Micro-tick timer (UTICK)

The ultra-low power Micro-tick Timer, running from the Watchdog oscillator, can be used to wake up the device from low power modes.

7.18.7.1 Features

- Ultra simple timer.
- Write once to start.
- Interrupt or software polling.

7.19 12-bit Analog-to-Digital Converter (ADC)

The ADC supports a resolution of 12-bit and fast conversion rates of up to 5.0 Msamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources. Possible trigger sources are the SCT, external pins, and the ARM TXEV interrupt.

The ADC supports a variable clocking scheme with clocking synchronous to the system clock or independent, asynchronous clocking for high-speed conversions

The ADC includes a hardware threshold compare function with zero-crossing detection. The threshold crossing interrupt is connected internally to the SCT inputs for tight timing control between the ADC and the SCT.

7.19.1 Features

- 12-bit successive approximation analog to digital converter.
- Input multiplexing among up to 12 pins.
- Two configurable conversion sequences with independent triggers.
- Optional automatic high/low threshold comparison and “zero crossing” detection.
- Measurement range VREFN to VREFP (typically 3 V; not to exceed VDDA voltage level).
- 12-bit conversion rate of 5.0 MHz. Options for reduced resolution at higher conversion rates.

- Burst conversion mode for single or multiple inputs.
- Synchronous or asynchronous operation. Asynchronous operation maximizes flexibility in choosing the ADC clock frequency, Synchronous mode minimizes trigger latency and can eliminate uncertainty and jitter in response to a trigger.

7.20 System control

7.20.1 Clock sources

The BLM32F40AXX supports two external and three internal clock sources:

- The Internal RC (IRC).
- Watchdog oscillator (WDOSC).
- External clock source from the digital I/O pin CLKIN.
- External RTC 32 KHz clock.
- Output of the system PLL.

7.20.1.1 Internal RC oscillator (IRC)

The IRC can be used as the clock that drives the system PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz.

Upon power-up or any chip reset, the BLM32F40AXX uses the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.20.1.2 Watchdog oscillator (WDOSC)

The watchdog oscillator is a low-power internal oscillator. The WDOSC can be used to provide a clock to the WWDT and to the entire chip. The nominal output frequency is 500 kHz.

7.20.1.3 Clock input pin (CLKIN)

An external square-wave clock source (up to 25 MHz) can be supplied on the digital I/O pin CLKIN.

7.20.2 System PLL

The system PLL accepts an input clock frequency in the range of 32 kHz to 12 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO).

The PLL can be enabled or disabled by software.

7.20.3 Clock Generation

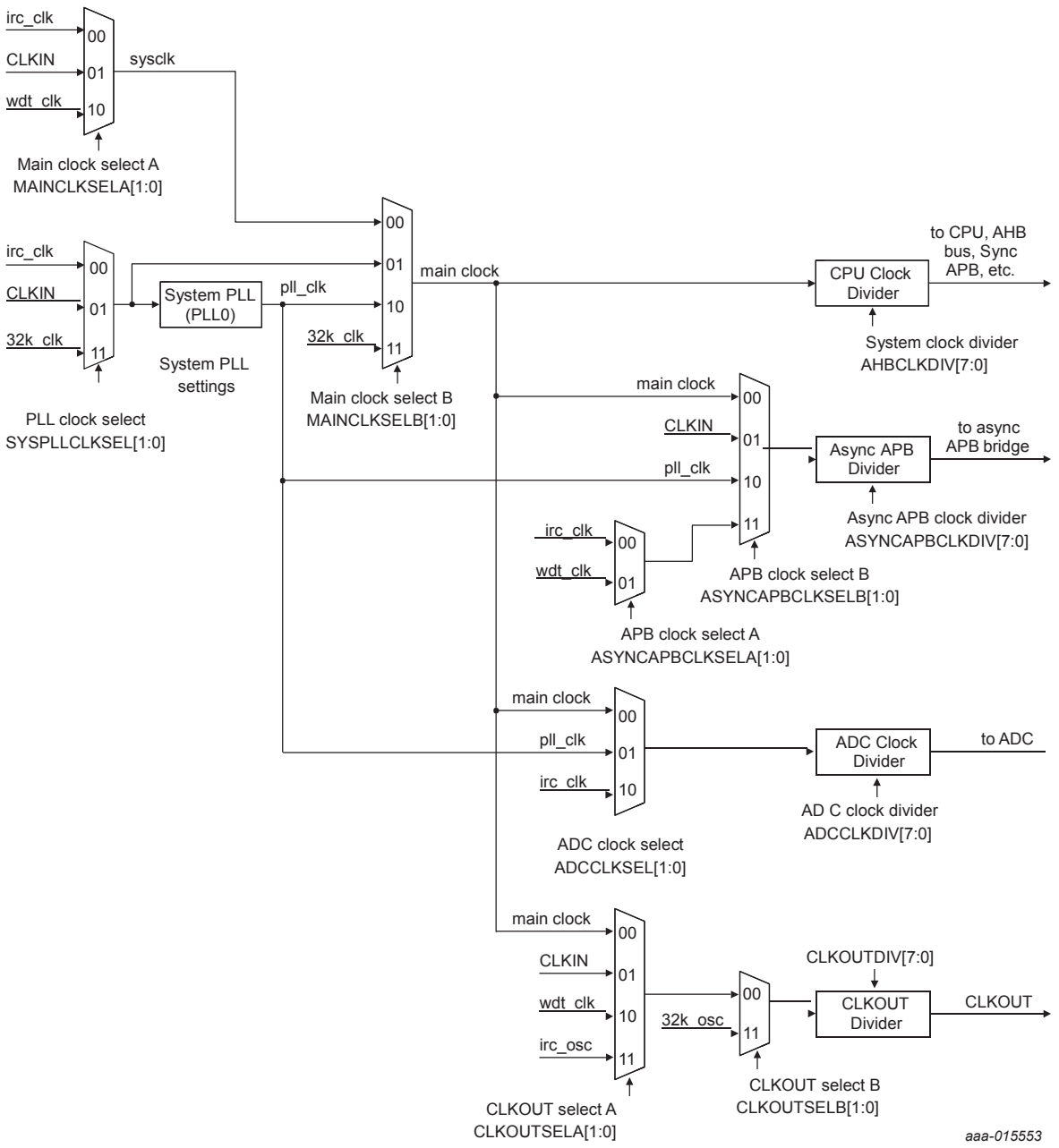


Fig 7. BLM32F40AX clock

7.20.4 Power control

The BLM32F40AXX support a variety of power control features. In Active mode, when the chip is running, power and clocks to selected peripherals can be optimized for power consumption. In addition, there are four special modes of processor power reduction with different peripherals running: Sleep mode, deep sleep mode, power down mode, and deep power-down mode, activated by the power mode configure API.

7.20.4.1 Sleep mode

When sleep mode is entered, the clock to the core is stopped along with any unused peripherals. Waking up from the sleep mode does not need any special sequence other than re-enabling the clock to the ARM core.

In sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, internal buses, and unused peripherals. The processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static.

7.20.4.2 Deep sleep mode

In deep sleep mode, all peripheral clocks and all clock sources are off with the option of keeping the 32 kHz clock and the WDOSC running. In addition, all analog blocks are shut down and the flash is put in stand-by mode. In deep sleep mode, the application can keep some of the internal clocks and the BOD circuit running for self-timed wake-up and BOD protection.

The BLM32F40AXX can wake up from deep sleep mode via a reset, digital pins selected as inputs to the pin interrupt block, RTC alarm, Micro-tick, a watchdog timer reset interrupt, BOD interrupt/reset, or an interrupt from the USART (in 32 kHz mode or synchronous slave mode), the SPI, or any of the I2C peripherals. For wake-up from deep sleep mode, the SPI, USART, and I2C peripherals must be configured in slave mode.

Any interrupt used for waking up from deep sleep mode must be enabled in one of the SYSCON wake-up enable registers and the NVIC.

In deep sleep mode, the processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static. deep sleep mode allows for very low quiescent power and fast wake-up options.

7.20.4.3 Power down mode

In power down mode, all peripheral clocks and all clock sources are off with the option of keeping the 32 kHz clock, and the WDOSC running. In addition, all analog blocks and the flash are shut down. In power down mode, the application can keep the BOD circuit running for BOD protection.

The BLM32F40AXX can wake up from power down mode via a reset, digital pins selected as inputs to the pin interrupt block, RTC alarm, Micro-tick, a watchdog timer reset interrupt, BOD interrupt/reset, or an interrupt from the USART (in 32 kHz mode or synchronous slave mode), the SPI, or any of the I2C peripherals. For wake-up from power down mode, the SPI, USART, and I2C peripherals must be configured in slave mode.

In power down mode, the processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static. Power down mode reduces power consumption compared to deep sleep mode at the expense of longer wake-up times.

7.20.4.4 Deep power-down mode

In deep power-down mode, power is shut off to the entire chip except for the RTC power domain and the RESET pin. The BLM32F40AXX can wake up from deep power down mode via the RESET pin and the RTC alarm.

7.20.5 Brownout detection

The BLM32F40AXX includes a monitor for the voltage level on the V_{DD} pin. If this voltage falls below a fixed level, the BOD sets a flag that can be polled or cause an interrupt. In addition, a separate threshold levels can be selected to cause chip reset and interrupt.

7.20.6 Safety

The BLM32F40AXX includes a Windowed WatchDog Timer (WWDT), which can be enabled by software after reset. Once enabled, the WWDT remains locked and cannot be modified in any way until a reset occurs.

7.21 Code security (Code Read Protection - CRP)

This feature of the BLM32F40AXX allows user to enable different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

In addition, ISP entry can be invoked by pulling a pin on the BLM32F40AXX LOW on reset. This pin is called the ISP entry pin.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. CRP3 fully disables any access to the chip via SWD and ISP. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or a call to reinvoke ISP command to enable a flash update via USART.
4. In addition to the three CRP levels, sampling of the ISP entry pin for valid user code can be disabled (No_ISP mode). For details, see the BLM32F40AXX user manual.

CAUTION	
	If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

7.22 Emulation and debugging

Debug and trace functions are integrated into the ARM Cortex-M4 and ARM Cortex-M0+. Serial wire debug and trace functions are supported. The ARM Cortex-M4 is configured to support up to eight breakpoints and four watch points. The ARM Cortex-M0+ is configured to support up to four breakpoints and two watch points. In addition, JTAG boundary scan mode is provided.

The ARM SYSREQ reset is supported and causes the processor to reset the peripherals, execute the boot code, restart from address 0x0000 0000, and break at the user entry point.

The SWD pins are multiplexed with other digital I/O pins. On reset, the pins assume the SWD functions by default.

8. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)	on pin VDD	[2]	−0.5	+4.6	V
V_{DDA}	analog supply voltage	on pin VDDA		-0.5	+4.6	V
V_{ref}	reference voltage	on pin VREFP	-	−0.5	+4.6	V
V_I	input voltage	only valid when the V_{DD} > 1.8 V; 5 V tolerant I/O pins	[6][7]	−0.5	5.0	V
V_I	input voltage	on I2C open-drain pins	[5]	−0.5	+5.0	V
V_{IA}	analog input voltage	on digital pins configured for an analog function	[8][9]	−0.5	V_{DD}	V
I_{DD}	total supply current		[3]	-	60	mA
I_{SS}	total ground current		[3]	-	60	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; T_j < 125 °C		-	100	mA
$V_{i(rtcx)}$	32 kHz oscillator input voltage		[2]	-0.5	4.6	V
T_{stg}	storage temperature		[10]	−65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[4]		4000	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

c) The limiting values are stress ratings only and operating the part at these values is not recommended and proper operation is not guaranteed. The conditions for functional operation are specified in Table 16.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 16) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] The peak current is limited to 25 times the corresponding maximum current.

[4] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[5] V_{DD} present or not present. Compliant with the I^2C-bus standard. 5.5 V can be applied to this pin when V_{DD} is powered down.

[6] Applies to all 5 V tolerant I/O pins except true open-drain pins.

[7] Including the voltage on outputs in 3-state mode.

[8] An ADC input voltage above 3.6 V can be applied for a short time without leading to immediate, unrecoverable failure. Accumulated exposure to elevated voltages at 4.6 V must be less than 10^6 s total over the lifetime of the device. Applying an elevated voltage to the ADC inputs for a long time affects the reliability of the device and reduces its lifetime.

[9] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[10] Dependent on package type.

9. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 8. Thermal resistance

Symbol	Parameter	Conditions	Max/Min	Unit
QFN64 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	58 ± 15 %	°C/W
		Single-layer (4.5 in × 3 in); still air	81 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		18 ± 15 %	°C/W
QFN48 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	41 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		0.3 ± 15 %	°C/W

10. Static characteristics

10.1 General operating conditions

Table 9. General operating conditions

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{clk}	clock frequency	internal CPU/system clock		-	-	100	MHz
V_{DD}	supply voltage (core and external rail)			1.62	-	3.6	V
V_{DDA}	analog supply voltage		[1]	1.62	-	3.6	V
V_{refp}	ADC positive reference voltage	$V_{DDA} \geq 2$ V	[2]	2.0	-	V_{DDA}	V
		$V_{DDA} < 2$ V		V_{DDA}	-	V_{DDA}	V
RTC oscillator pins							
$V_{i(rtcx)}$	32 kHz oscillator input voltage	on pin RTCXIN		−0.5	-	+3.6	V
$V_{o(rtcx)}$	32 kHz oscillator output voltage	on pin RTCXOUT		−0.5	-	+3.6	V

[1] The V_{DD} voltage must be equal or lower than the voltage level on V_{DDA}.

[2] The V_{refp} voltage must not exceed the voltage level on V_{DDA}.

10.2 CoreMark data

Table 10. CoreMark score

T_{amb} = 25 °C, V_{DD} = 3.3V

Parameter	Conditions		Typ	Unit
ARM Cortex-M4 in active mode; ARM Cortex-M0+ in sleep mode				
CoreMark score	CoreMark code executed from SRAM; CCLK = 12 MHz	[1][3][4][5]	2.6	(Iterations/s) / MHz
	CCLK = 48 MHz	[2][3][4][5]	2.6	(Iterations/s) / MHz
	CCLK = 84 MHz	[2][3][4][5]	2.6	(Iterations/s) / MHz
	CCLK = 100 MHz	[2][3][4][5]	2.6	(Iterations/s) / MHz
CoreMark score	CoreMark code executed from flash; CCLK = 12 MHz; 1 system clock flash access time.	[1][3][4][6]	2.6	(Iterations/s) / MHz
	CCLK = 48 MHz; 3 system clock flash access time.	[2][3][4][6]	2.4	(Iterations/s) / MHz
	CCLK = 84 MHz; 5 system clock flash access time.	[2][3][4][6]	2.3	(Iterations/s) / MHz
	CCLK = 100 MHz; 6 system clock flash access time.	[2][3][4][6]	2.2	(Iterations/s) / MHz

[1] Clock source 12 MHz IRC. PLL disabled.

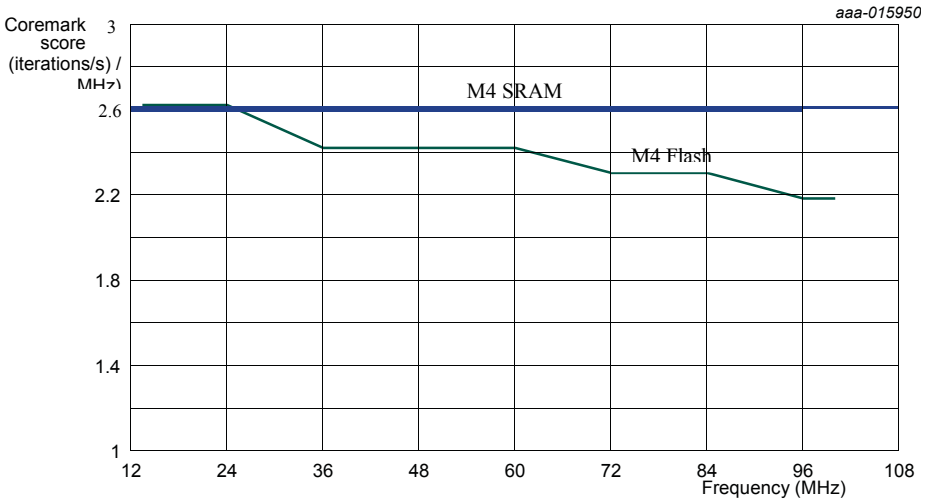
[2] Clock source 12 MHz IRC. PLL enabled.

[3] Characterized through bench measurements using typical samples.

[4] Compiler settings: Keil µVision v.5.12, optimization level 3, optimized for time on.

[5] SRAM0 and SRAM1 powered, SRAM2 powered down.

[6] See the FLASHCFG register in the BLM32F40AXX User Manual for system clock flash access time settings.



Conditions: V_{DD} = 3.3 V; T_{amb} = 25 °C; active mode; all peripherals except one UART; BOD disabled; SRAM0 and SRAM1 powered, SRAM2 powered down. See the FLASHCFG register in the BLM32F40AX User Manual for system clock flash access time settings. Measured with Keil uVision 5.12. Optimization level 3, optimized for time on.

12 MHz: IRC enabled; PLL disabled. 24 MHz - 100 MHz: IRC enabled; PLL enabled.

Fig 8. Typical CoreMark score

10.3 Power consumption

Power measurements in Active, sleep, deep sleep, and power down modes were performed under the following conditions:

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIO DIR register.
- Write 1 to the GPIO CLR register to drive the outputs LOW.
- All peripherals disabled.

Table 11. Static characteristics: Power consumption in active and sleep modes

T_{amb} = −40 °C to +105 °C, unless otherwise specified.1.62 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
ARM Cortex-M0+ in active mode; ARM Cortex-M4 in sleep mode							
I_{DD}	supply current	CoreMark code executed from SRAM; flash powered down CCLK = 12 MHz	[2][4][6]	-	1.2	-	mA
		CCLK = 48 MHz	[3][4][6]	-	3.0	-	mA
		CCLK = 84 MHz	[3][4][6]	-	4.5	-	mA
		CCLK = 100 MHz	[3][4][6]	-	5.5	-	mA
I_{DD}	supply current	CoreMark code executed from flash; CCLK = 12 MHz; 1 system clock flash access time.	[2][4][6]	-	1.5	-	mA
		CCLK = 48 MHz; 3 system clock flash access time.	[3][4][6]	-	3.6	-	mA
		CCLK = 84 MHz; 6 system clock flash access time.	[3][4][6]	-	5.4	-	mA
		CCLK = 100 MHz; 7 system clock flash access time.	[3][4][6]	-	6.6	-	mA
I_{DD}	supply current	Calculating Fibonacci numbers executed from flash; CCLK = 12 MHz	[2][4][5]	-	1.5	-	mA
		CCLK = 84 MHz	[3][4][5]	-	6.2	-	mA
		CCLK = 96 MHz	[3][4][5]	-	7.2	-	mA

Table 11. Static characteristics: Power consumption in active and sleep modes

T_{amb} = −40 °C to +105 °C, unless otherwise specified.1.62 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
ARM Cortex-M4 in active mode; ARM Cortex-M0+ in sleep mode							
I_{DD}	supply current	CoreMark code executed from SRAM; flash powered down					
		CCLK = 12 MHz	[2][4][6]	-	1.5	-	mA
		CCLK = 48 MHz	[3][4][6]	-	4.8	-	mA
		CCLK = 84 MHz	[3][4][6]	-	7.9	-	mA
		CCLK = 100 MHz	[3][4][6]	-	9.9	-	mA
I_{DD}	supply current	CoreMark code executed from flash;					
		CCLK = 12 MHz; 1 system clock flash access time.	[2][4][6]	-	1.9	-	mA
		CCLK = 48 MHz; 3 system clock flash access time.	[3][4][6]	-	5.7	-	mA
		CCLK = 84 MHz; 6 system clock flash access time.	[3][4][6]	-	8.8	-	mA
		CCLK = 100 MHz; 7 system clock flash access time.	[3][4][6]	-	10.7	-	mA
I_{DD}	supply current	Calculating Fibonacci numbers executed from SRAM;					
		CCLK = 12 MHz	[2][4][5]	-	1.7	-	mA
		CCLK = 84 MHz	[3][4][5]	-	8.0	-	mA
		CCLK = 96 MHz	[3][4][5]	-	9.4	-	mA
I_{DD}	supply current	Calculating Fibonacci numbers executed from flash;					
		CCLK = 12 MHz	[2][4][5]	-	1.7	-	mA
		CCLK = 84 MHz	[3][4][5]	-	8.0	-	mA
		CCLK = 96 MHz	[3][4][5]	-	9.4	-	mA

Table 11. Static characteristics: Power consumption in active and sleep modes

T_{amb} = −40 °C to +105 °C, unless otherwise specified.1.62 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
ARM Cortex-M4 in sleep mode; ARM Cortex-M0+ in sleep mode							
I_{DD}	supply current	CCLK = 12 MHz	[2][4][7]	-	990	-	µA
		CCLK = 100 MHz	[3][4][7]	-	4.0	-	mA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C), 3.3V.

[2] Clock source 12 MHz IRC. PLL disabled.

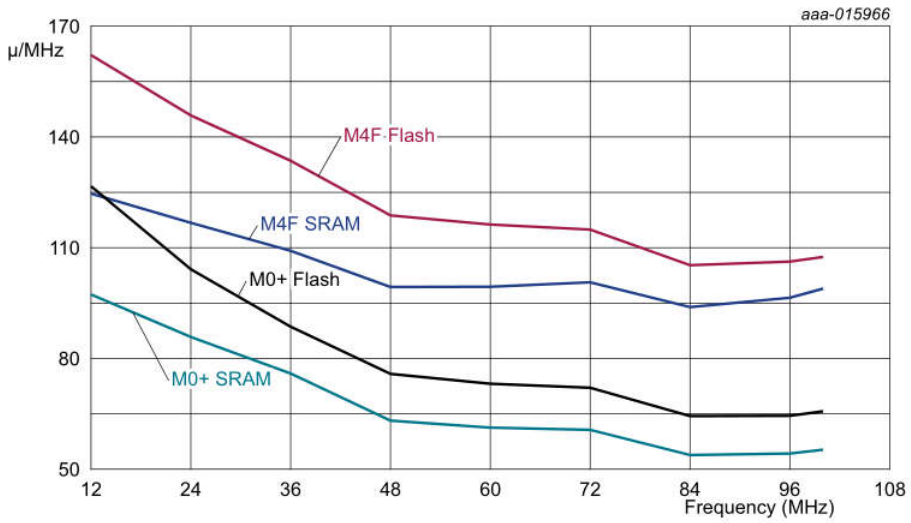
[3] Clock source 12 MHz IRC. PLL enabled.

[4] Characterized through bench measurements using typical samples.

[5] Compiler settings: Keil µVision v.5.10, optimization level 0, optimized for time off.

[6] Prefetch disabled in FLASHCFG register. System clock flash access time set by power API. SRAM0 powered, SRAM1 and SRAM2 powered down.Compiler settings: Keil µVision v.5.12, optimization level 0, optimized for time off.

[7] First 8 kB in SRAM0 powered; Flash, SRAM1, and SRAM2 are powered down; all peripheral clocks disabled. Compiler settings: Keil µVision v.5.12, optimization level 0, optimized for time off.



Conditions: V_{DD} = 3.3 V; T_{amb} = 25 °C; active mode; all peripherals disabled; BOD disabled; Prefetch disabled in FLASHCFG register. System clock flash access time set by power API. SRAM0 powered, SRAM1 and SRAM2 powered down. Measured with Keil uVision 5.12. Optimization level 0, optimized for time off.

12 MHz: IRC enabled; PLL disabled. 24 MHz - 100 MHz: IRC enabled; PLL enabled.

Fig 9. CoreMark power consumption: typical µA/MHz for M4 and M0+ cores

Table 12. Static characteristics: Power consumption in deep sleep, power down, and deep power-down modes

T_{amb} = −40 °C to +105 °C, 1.62 V ≤ V_{DD} ≤ 2.0 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1][2]	Max[3]	Unit
I_{DD}	supply current	Deep sleep mode; all SRAM on:	[2]				
		T_{amb} = 25 °C		-	235	380	µA
		T_{amb} = 105 °C		-	-	1.9	mA
		Power down mode;	[2]				
		first 8 kB in SRAM0 powered:					
		T_{amb} = 25 °C		-	4	8	µA
		T_{amb} = 105 °C			-	110	µA
		SRAM0 (64 kB) powered		-	6.7	-	µA
		SRAM0 (64 kB), SRAM1 (32 kB) powered		-	7.8	-	µA
		SRAM0 (64 kB), SRAM1 (32 kB), SRAM2 (8 kB) powered		-	8.2	-	µA
		Deep power-down mode;	[2]	-			
		RTC oscillator input grounded (RTC oscillator disabled)					
		T_{amb} = 25 °C			160	340	nA
		T_{amb} = 105 °C			-	14	µA
		RTC oscillator running with external crystal		-	240	-	nA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C).

[2] Characterized through bench measurements using typical samples. V_{DD} = 1.62 V

[3] Guaranteed by characterization, not tested in production. V_{DD} = 2.0 V

Table 13. Static characteristics: Power consumption in deep sleep, power down, and deep power-down modes

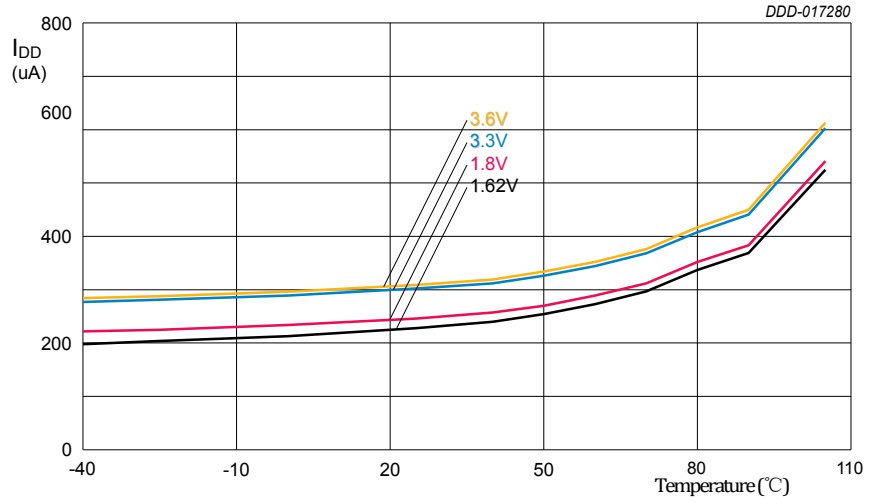
T_{amb} = −40 °C to +105 °C, 2.7 V ≤ V_{DD} ≤ 3.6 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1][2]	Max[3]	Unit
I_{DD}	supply current	Deep sleep mode; all SRAM on:	[2]	-			
		T_{amb} = 25 °C			306	480	µA
		T_{amb} = 105 °C		-	-	2.3	mA
		Power down mode;	[2]				
		first 8 kB in SRAM0 powered:					
		T_{amb} = 25 °C		-	5	10	µA
		T_{amb} = 105 °C		-	-	115	µA
		SRAM0 (64 kB) powered		-	7.3	-	µA
		SRAM0 (64 kB), SRAM1 (32 kB) powered		-	8.6	-	µA
		SRAM0 (64 kB), SRAM1 (32 kB), SRAM2 (8 kB) powered		-	9	-	µA
		Deep power-down mode;	[2]				
		RTC oscillator input grounded (RTC oscillator disabled)					
		T_{amb} = 25 °C		-	200	570	nA
		T_{amb} = 105 °C			-	20	µA
		RTC oscillator running with external crystal		-	280	-	nA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C).

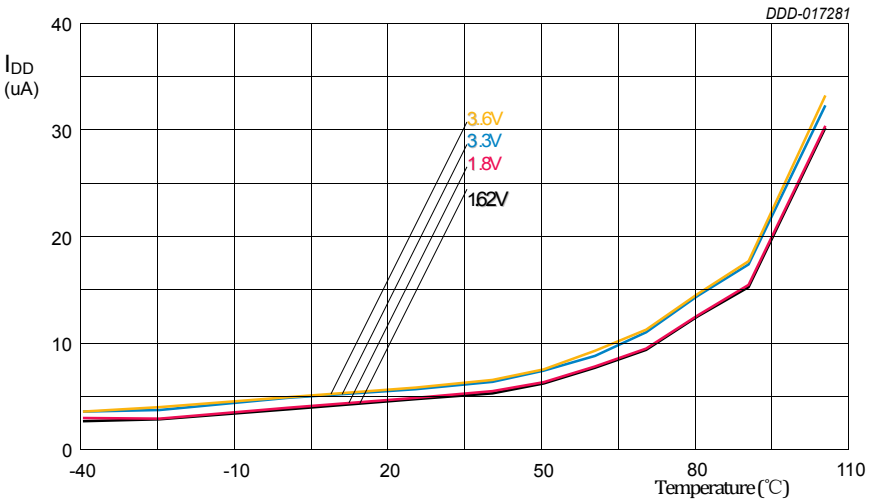
[2] Characterized through bench measurements using typical samples. V_{DD} = 3.3 V

[3] Tested in production, V_{DD} = 3.6 V



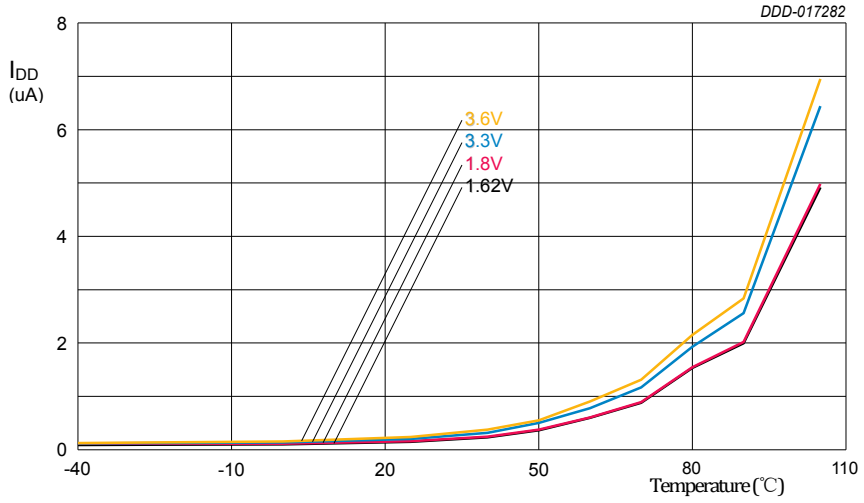
Conditions: BOD disabled; All SRAM blocks enabled.

Fig 10. Deep sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



Conditions: BOD disabled; all SRAM disabled except first 8 kB in SRAM0.

Fig 11. Power down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



RTC disabled (RTC oscillator input grounded)

Fig 12. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

Table 14. Typical peripheral power consumption[1][2][3]

V_{DD} = 3.3 V; T_{amb} = 25 °C

Peripheral	I_{DD} in uA
IRC	262
WDT OSC	2.0
Flash	200.0
BOD	2.0
CLKOUT	37

[1] The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled using PDRUNCFG register. All other blocks are disabled and no code accessing the peripheral is executed.

[2] The supply currents are shown for system clock frequencies of 12MHz.

[3] Typical ratings are not guaranteed. Characterized through bench measurements using typical samples.

Table 15. Typical AHB/APB peripheral power consumption[3][4][5]

V_{DD} = 3.3 V; T = 25 °C

Peripheral		I_{DD} in µA	I_{DD} in µA/MHz	I_{DD} in µA/MHz
AHB peripheral			**CPU: 12 MHz, sync APB bus: 12 MHz**	**CPU: 96MHz, sync APB bus: 96 MHz**
GPIO0	[1]	-	0.50	0.7
GPIO1	[1]	-	0.42	0.52
DMA		-	5.0	6.86
CRC		-	0.42	0.50
MAILBOX		-	0.17	0.20
ADC0		-	2.25	2.92
SCTimer/PWM		-	5.08	7.07

Table 15. Typical AHB/APB peripheral power consumption[3][4][5]

V_{DD} = 3.3 V; T = 25 °C

Peripheral		I_{DD} in µA	I_{DD} in µA/MHz	I_{DD} in µA/MHz
FIFO		-	3.17	4.49
Sync APB periphera			**CPU: 12 MHz, sync APB bus: 12 MHz**	**CPU: 96MHz, sync APB bus: 96 MHz**
INPUTMUX	[1]	-	0.83	0.96
IOCON	[1]	-	1.25	1.55
PINT		-	0.83	1.05
GINT		-	0.50	0.61
WWDT		-	0.17	0.28
MRT		-	0.50	0.65
RTC		-	0.08	0.09
RIT		-	0.50	0.71
UTICK		-	0.17	0.11
Timer2		-	0.58	0.67
Timer3		-	0.42	0.42
Timer4		-	0.50	0.57
Async APB peripheral			**CPU: 12 MHz, Async APB bus: 12 MHz**	**CPU: 96MHz, Async APB bus: 12 MHz[2]**
USART0		-	0.67	0.11
USART1		-	0.75	0.07
USART2		-	0.67	0.11
USART3		-	0.75	0.07
I2C0		-	0.92	0.10
I2C1		-	0.83	0.26
I2C2		-	0.83	0.25
SPIO0		-	0.92	0.21
SPIO1		-	0.83	0.25
CTimer0		-	0.58	0.18
CTimer1		-	0.42	0.14
Fractional Rate Generator		-	4.17	0.73

[1] Turn off the peripheral when the configuration is done.

[2] For optimal system power consumption, use fixed low frequency Async APB bus when the CPU is at a higher frequency.

[3] The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled using ASYNCAPBCLKCTRL, AHBCLKCTRL0/1, and PDRUNCFG register. All other blocks are disabled and no code accessing the peripheral is executed.

[4] The supply currents are shown for system clock frequencies of 12 MHz and 96 MHz.

[5] Typical ratings are not guaranteed. Characterized through bench measurements using typical samples.

10.4 Pin characteristics

Table 16. Static characteristics: pin characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified. 1.62 V ≤ V_{DD} ≤ 3.6 V unless otherwise specified. Values tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
RESET pin							
V_{IH}	HIGH-level input voltage			0.8 × V_{DD}	-	5.0	V
V_{IL}	LOW-level input voltage			−0.5	-	0.3 × V_{DD}	V
V_{hys}	hysteresis voltage		[9]	0.05 × V_{DD}	-	-	V
Standard I/O pins							
Input characteristics							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	3.0	180	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; V_{DD} = 3.6 V; for RESETN pin			3.0	180	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled		-	3.0	180	nA
V_I	input voltage	pin configured to provide a digital function;	[3]				
		V_{DD} > 1.8 V		0	-	5.0	V
		V_{DD} = 0 V		0	-	3.6	V
V_{IH}	HIGH-level input voltage	1.62 V ≤ V_{DD} < 2.7 V		1.5	-	5.0	V
		2.7 V ≤ V_{DD} ≤ 3.6 V		2.0	-	5.0	V
V_{IL}	LOW-level input voltage	1.62 V ≤ V_{DD} < 2.7 V		−0.5	-	+0.4	V
		2.7 V ≤ V_{DD} ≤ 3.6 V		−0.5	-	+0.8	V
V_{hys}	hysteresis voltage		[9]	0.1 × V_{DD}	-	-	V
Output characteristics							
V_O	output voltage	output active		0	-	V_{DD}	V
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/pull-down resistors disabled		-	3	180	nA
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA; 1.62 V ≤ V_{DD} < 2.7 V		V_{DD} − 0.4	-	-	V
		I_{OH} = −6 mA; 2.7 V ≤ V_{DD} ≤ 3.6 V		V_{DD} − 0.4			
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA; 1.62 V ≤ V_{DD} < 2.7 V		-	-	0.4	V
		I_{OL} = 6 mA; 2.7 V ≤ V_{DD} ≤3.6 V		-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V; 1.62 V ≤ V_{DD} < 2.7 V		4.0	-	-	mA
		V_{OH} = V_{DD} − 0.4 V; 2.7 V ≤ V_{DD} ≤ 3.6 V		6.0	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; 1.62 V ≤ V_{DD} < 2.7 V		4.0	-	-	mA
		V_{OL} = 0.4 V; 2.7 V ≤ V_{DD} ≤ 3.6 V		6.0	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	1.62 V ≤ V_{DD} < 2.7 V	[2][4]	-	-	35	mA
	drive HIGH; connected to ground;	2.7 V ≤ V_{DD} ≤ 3.6 V		-	-	87	mA

Table 16. Static characteristics: pin characteristics *...continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified. 1.62 V ≤ V_{DD} ≤ 3.6 V unless otherwise specified. Values tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OLS}	LOW-level short-circuit output current	1.62 V ≤ V_{DD} < 2.7 V	[2][4]	-	-	30	mA
	drive LOW; connected to V_{DD}	2.7 V ≤ V_{DD} ≤ 3.6 V		-	-	77	mA
Weak input pull-up/pull-down characteristics							
I_{pd}	pull-down current	V_I = V_{DD}		25		80	µA
		V_I = 5 V	[2]	80		100	µA
I_{pu}	pull-up current	V_I = 0 V		−25		−80	µA
		V_{DD} < V_I < 5 V	[2][7]	6		30	µA

Table 16. Static characteristics: pin characteristics *...continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified. 1.62 V ≤ V_{DD} ≤ 3.6 V unless otherwise specified. Values tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Open-drain I²C pins							
V_{IH}	HIGH-level input voltage	1.62 V ≤ V_{DD} < 2.7 V		0.7 × V_{DD}	-	-	V
		2.7 V ≤ V_{DD} ≤ 3.6 V		0.7 × V_{DD}	-	-	V
V_{IL}	LOW-level input voltage	1.62 V ≤ V_{DD} < 2.7 V		0	-	0.3 × V_{DD}	V
		2.7 V ≤ V_{DD} ≤ 3.6 V		0	-	0.3 × V_{DD}	V
V_{hys}	hysteresis voltage			0.1 × V_{DD}	-	-	V
I_{LI}	input leakage current	V_I = V_{DD}	[5]	-	2.5	3.5	µA
		V_I = 5 V		-	5.5	10	µA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; pin configured for standard mode or fast mode		4.0	-	-	mA
		V_{OL} = 0.4V; pin configured for Fast-mode Plus		20	-	-	mA
Pin capacitance							
C_{io}	input/output capacitance	I²C-bus pins	[8]	-	-	6.0	pF
		pins with digital functions only	[6]	-	-	2.0	pF
		Pins with digital and analog functions	[6]	-	-	7.0	pF

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltage.

[2] Based on characterization. Not tested in production.

[3] With respect to ground.

[4] Allowed as long as the current limit does not exceed the maximum current allowed by the device. [5] To V_{SS}.

[6] The values specified are simulated and absolute values, including package/bondwire capacitance.

[7] The weak pull-up resistor is connected to the V_{DD} rail and pulls up the I/O pin to the V_{DD} level.

[8] The value specified is a simulated value, excluding package/bondwire capacitance.

[9] Guaranteed by design, not tested in production.

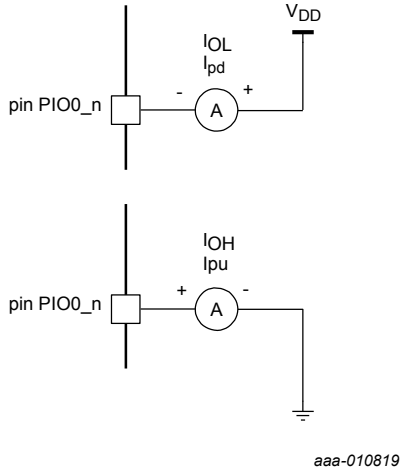
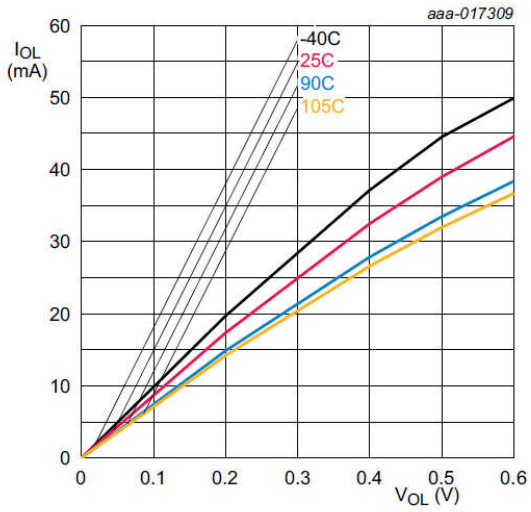
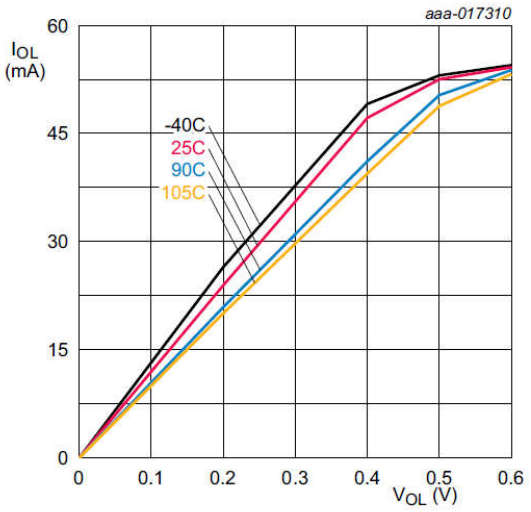


Fig 13. Pin input/output current measurement

10.4.1 Electrical pin characteristics

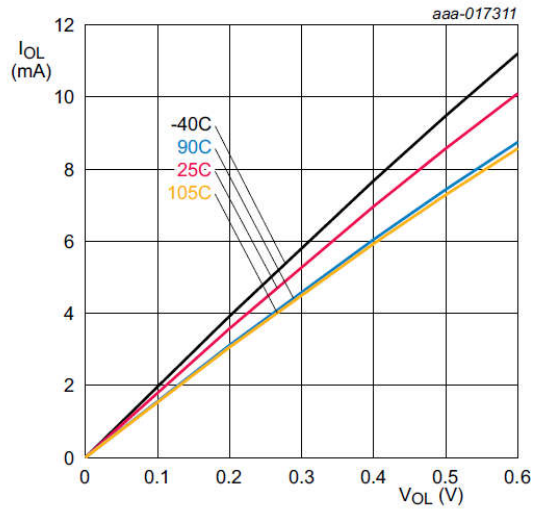


Conditions: V_{DD} = 1.8 V; on pins PIO0_23 to PIO0_28.

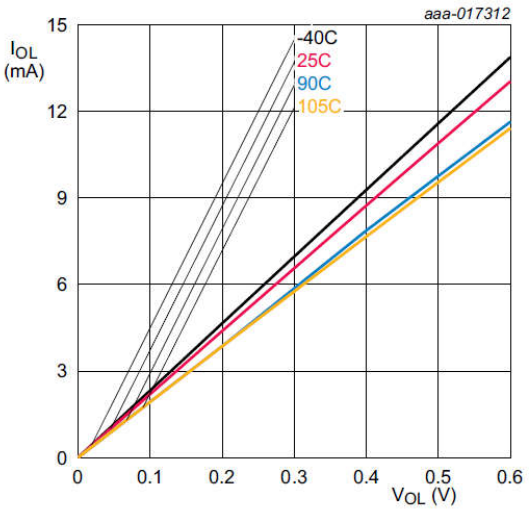


Conditions: V_{DD} = 3.3 V; on pins PIO0_23 to PIO0_28.

Fig 14. I^2C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

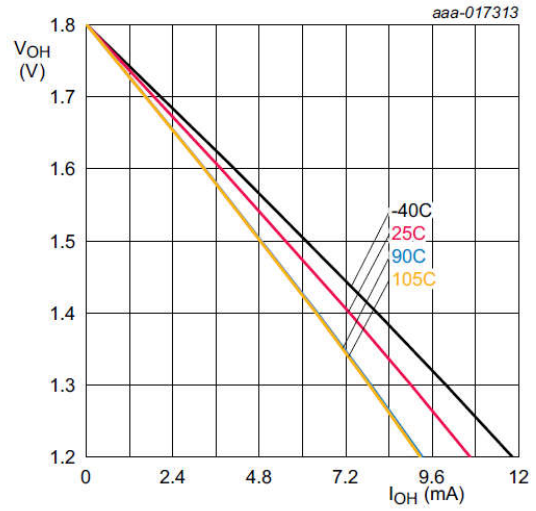


Conditions: V_{DD} = 1.8 V; on standard port pins.

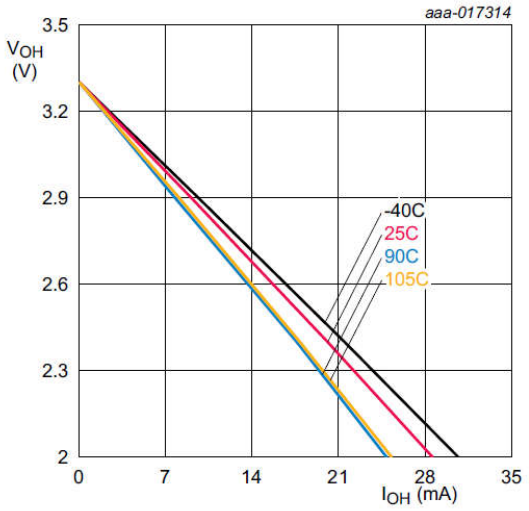


Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 15. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

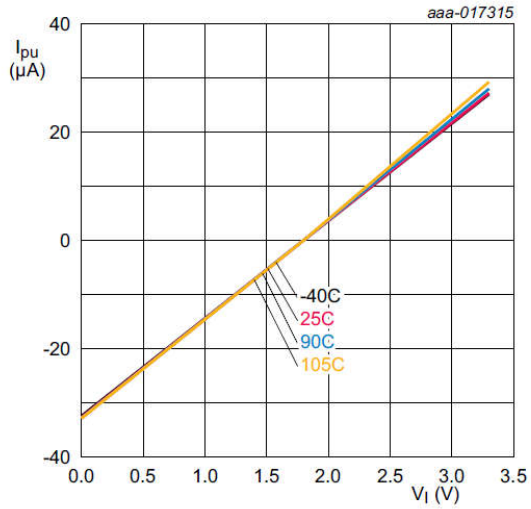


Conditions: V_{DD} = 1.8 V; on standard port pins.

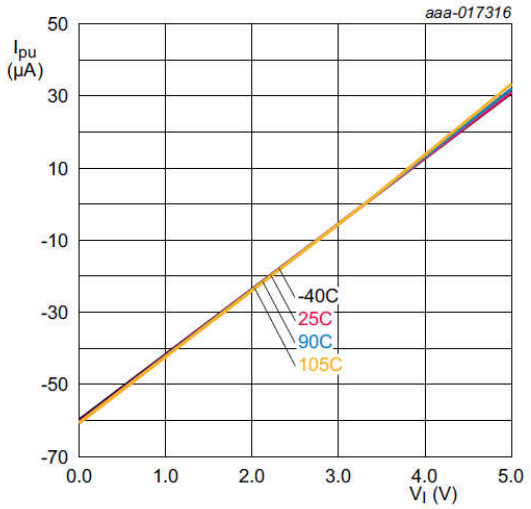


Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 16. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}

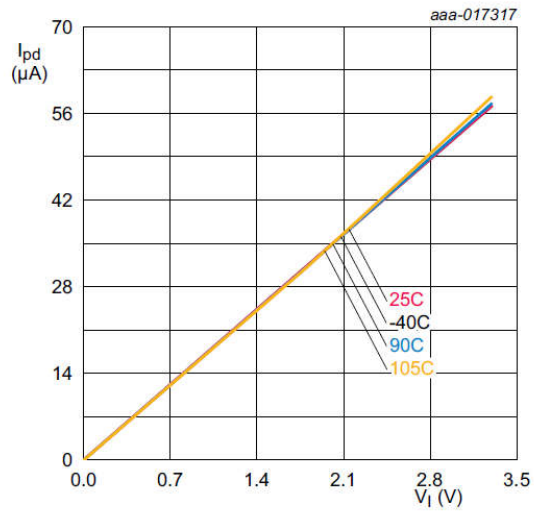


Conditions: V_{DD} = 1.8 V; on standard port pins.

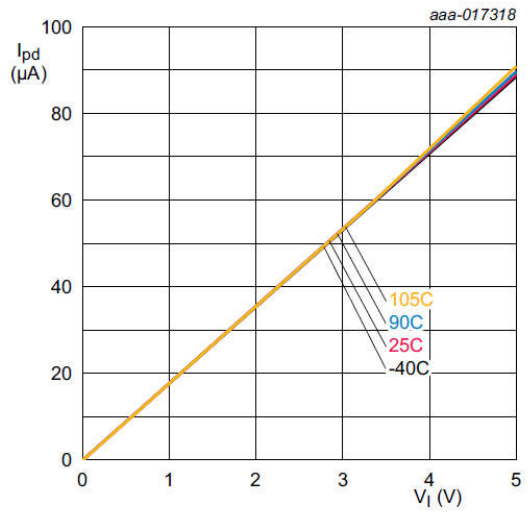


Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 17. Typical pull-up current I_{PU} versus input voltage V_I



Conditions: V_{DD} = 1.8V; on standard port pins.



Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 18. Typical pull-down current I_{PD} versus input voltage V_I

11. Dynamic characteristics

11.1 Power-up ramp conditions

Table 17. Power-up characteristics

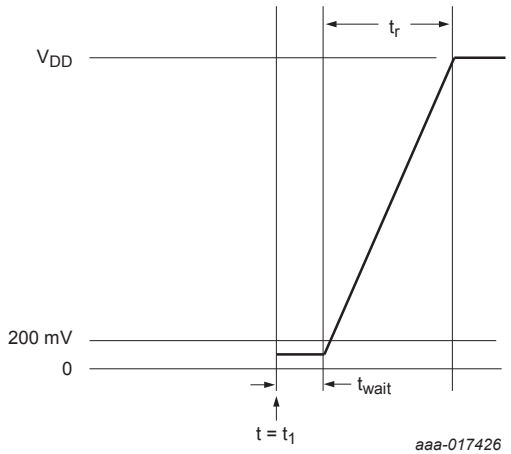
T_{amb} = −40 °C to +105 °C; 1.62 V ≤ V_{DD} ≤ 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	at t = t_1: 0 < V_I ≤ 200 mV	[1][3]	0	-	500	ms
t_{wait}	wait time		[1][2]	12	-	-	µs
V_I	input voltage	at t = t_1 on pin V_{DD}	[3]	0	-	200	mV

[1] See Figure 19.

[2] Based on simulation. The wait time specifies the time the power supply must be at levels below 200 mV before ramping up.

[3] Based on characterization, not tested in production.



Condition: 0 < V_I ≤ 200 mV at start of power-up (t = t_1)

Fig 19. Power-up ramp

11.2 Flash memory

Table 18. Flash characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified. 1.62 V ≤ V_{DD} ≤ 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance	sector erase/program	[1]	10000	-	-	cycles
		page erase/program; page in a sector		1000	-	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		10	-	-	years
t_{er}	erase time	page, sector, or multiple consecutive sectors		-	100	-	ms
t_{prog}	programming time		[2]	-	1	-	ms

[1] Number of erase/program cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash.

11.3 I/O pins

Table 19. Dynamic characteristic: I/O pins[1]

T_{amb} = −40 °C to +85 °C; 1.62 V ≤ V_{DD} ≤ 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Standard I/O pins - normal drive strength							
t_r	rise time	pin configured as output; SLEW = 1 (fast mode); 2.7 V ≤ V_{DD} ≤ 3.6 V	[2][3]	1.0	-	2.5	ns
		1.62 V ≤ V_{DD} ≤ 1.98 V		1.6	-	3.8	ns
t_f	fall time	pin configured as output; SLEW = 1 (fast mode); 2.7 V ≤ V_{DD} ≤ 3.6 V	[2][3]	0.9	-	2.5	ns
		1.62 V ≤V_{DD} ≤ 1.98 V		1.7	-	4.1	ns
t_r	rise time	pin configured as output; SLEW = 0 (standard mode); 2.7 V ≤ V_{DD} ≤ 3.6 V	[2][3]	1.9	-	4.3	ns
		1.62 V ≤ V_{DD} ≤ 1.98 V		2.9	-	7.8	ns
t_f	fall time	pin configured as output; SLEW = 0 (standard mode); 2.7 V ≤ V_{DD} ≤ 3.6 V	[2][3]	1.9	-	4.0	ns
		1.62 V ≤ V_{DD} ≤ 1.98 V		2.7	-	6.7	ns
t_r	rise time	pin configured as input	[4]	0.3	-	1.3	ns
t_f	fall time	pin configured as input	[4]	0.2	-	1.2	ns

[1] Simulated data.

[2] Simulated using 10 cm of 50 Ω PCB trace with 5 pF receiver input. Rise and fall times measured between 80 % and 20 % of the full output signal level.

[3] The slew rate is configured in the IOCON block the SLEW bit. See the BLM32F40AXX user manual. [4] C_L = 20 pF. Rise and fall times measured between 90 % and 10 % of the full input signal level.

11.4 Wake-up process

Table 20. Dynamic characteristic: Typical wake-up times from low power modes

V_{DD} = 3.3 V;T_{amb} = 25 °C; using IRC as the system clock.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{wake}	wake-up time	from sleep mode	[2][3]	-	1.6	-	µs
		from deep sleep mode with full SRAM retention: to code executing in flash or SRAM	[2]	-	18	-	µs

Table 20. Dynamic characteristic: Typical wake-up times from low power modes

V_{DD} = 3.3 V;T_{amb} = 25 °C; using IRC as the system clock.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
		from power down mode to code executing in flash	[2]	-	70	-	µs
		to code executing in SRAM	[2]		18	-	µs
		from deep power-down mode; RTC disabled; using RESET pin.	[4]	-	200	-	µs

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The wake-up time measured is the time between when a GPIO input pin is triggered to wake the device up from the low power modes and from when a GPIO output pin is set in the interrupt service routine (ISR) wake-up handler.

[3] IRC enabled, all peripherals off.

[4] RTC disabled. Wake-up from deep power-down causes the part to go through entire reset process. The wake-up time measured is the time between when the RESET pin is triggered to wake the device up and when a GPIO output pin is set in the reset handler.

11.5 System PLL

Table 21. PLL lock times and current

T_{amb} = −40 °C to +105 °C, unless otherwise specified. V_{DD} = 1.62 V to 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PLL configuration: input frequency 12 MHz; output frequency 75 MHz							
$t_{lock(PLL)}$	PLL lock time	PLL set-up procedure followed	[2]			400	µs
$I_{DD(PLL)}$	PLL current	when locked	[1][3]	-	-	550	µA
PLL configuration: input frequency 12 MHz; output frequency 100 MHz							
$t_{lock(PLL)}$	PLL lock time	PLL set-up procedure followed	[2]	-	-	400	µs
$I_{DD(PLL)}$	PLL current	when locked	[1][3]	-	-	750	µA
PLL configuration: input frequency 32.768 kHz; output frequency 75 MHz							
$t_{lock(PLL)}$	PLL lock time	-	[1]			6250	µs
$I_{DD(PLL)}$	PLL current	when locked	[1][3]	-	-	450	µA
PLL configuration: input frequency 32.768 kHz; output frequency 100 MHz							
$t_{lock(PLL)}$	PLL lock time	-	[1]	-	-	6250	µs
$I_{DD(PLL)}$	PLL current	when locked	[1][3]	-	-	560	µA

[1] Data based on characterization results, not tested in production.

[2] PLL set-up requires high-speed start-up and transition to normal mode. Lock times are only valid when high-speed start-up settings are applied followed by normal mode settings. The procedure for setting up the PLL is described in the BLM32F40AXX user manual.

[3] PLL current measured using lowest CCO frequency to obtain the desired output frequency.

Table 22. Dynamic characteristics of the PLL[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Reference clock input							
F_{in}	input frequency	-		32.768 kHz	-	25 MHz	-
Clock output							
f_o	output frequency	for PLL clkout output	[3]	1.2	-	150	MHz
d_o	output duty cycle	for PLL clkout output		46	-	54	%
f_{CCO}	CCO frequency			-	-	150	MHz
Lock detector output							
$\Delta_{lock(PFD)}$	PFD lock criterion		[4]	1	2	4	ns
Dynamic parameters at $f_{out} = f_{CCO} = 100$ MHz; standard bandwidth settings							
$J_{rms\text{-}interval}$	RMS interval jitter	$f_{ref} = 10$ MHz	[5][6]	-	15	30	ps
$J_{pp\text{-}period}$	peak-to-peak, period jitter	$f_{ref} = 10$ MHz	[5][6]	-	40	80	ps

[1] Data based on characterization results, not tested in production.

[2] Output jitter depends on the frequency of input jitter and is equal to or less than the input jitter.

[3] Excluding under- and overshoot which may occur when the PLL is not in lock.

[4] A phase difference between the inputs of the PFD (clkref and clkfb) smaller than the PFD lock criterion means lock output is HIGH.

[5] Actual jitter dependent on amplitude and spectrum of substrate noise.

[6] Input clock coming from a crystal oscillator with less than 250 ps peak-to-peak period jitter.

11.6 IRC

Table 23. Dynamic characteristic: IRC oscillator

$1.62\ V \leq V_{DD} \leq 3.6\ V$.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	$T_{amb} = 25\ °C$	[2]	12 –1 %	12	12 +1 %	MHz
		$-40\ °C \leq T_{amb} \leq +105\ °C$	[3]	12 –3.5 %	12	12 +3 %	MHz
		$0\ °C \leq T_{amb} \leq +85\ °C$	[3]	12 –2 %	12	12 +2.5 %	MHz

[1] Typical ratings are not guaranteed. The value listed is at room temperature (25 °C).

[2] Tested in production.

[3] Guaranteed by characterization, not tested in production.

11.7 RTC oscillator

See Section 13.5 for connecting the RTC oscillator to a crystal or an external clock source.

Table 24. Dynamic characteristic: RTC oscillator

$1.62\ V \leq V_{DD} \leq 3.6\ V$[1]

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_i	input frequency	-		-	32.768	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.8 Watchdog oscillator

Table 25. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter		Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal watchdog oscillator frequency	[2]	-	500	-	kHz
D_{clkout}	clkout duty cycle		48	-	52	%
J_{PP-CC}	peak-peak period jitter	[3][4]	-	1	20	ns
t_{start}	start-up time	[4]	-	4	-	µs

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +105 °C) is ±40 %.

[3] Actual jitter dependent on amplitude and spectrum of substrate noise.

[4] Guaranteed by design. Not tested in production samples.

11.9 I²C-bus

Table 26. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +105 °C; 1.62 V ≤ V_{DD} ≤ 3.6 V.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus	0	1	MHz
t_f	fall time	[4][5][6][7]	of both SDA and SCL signals Standard-mode	-	300	ns
			Fast-mode	20 + 0.1 × C_b	300	ns
			Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus	0.26	-	µs
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] Guaranteed by design. Not tested in production.

[2] Parameters are valid over operating temperature range unless otherwise specified. See the I²C-bus specification *UM10204* for details.

[3] tHD;DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall times are allowed.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 μs and 0.9 μs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

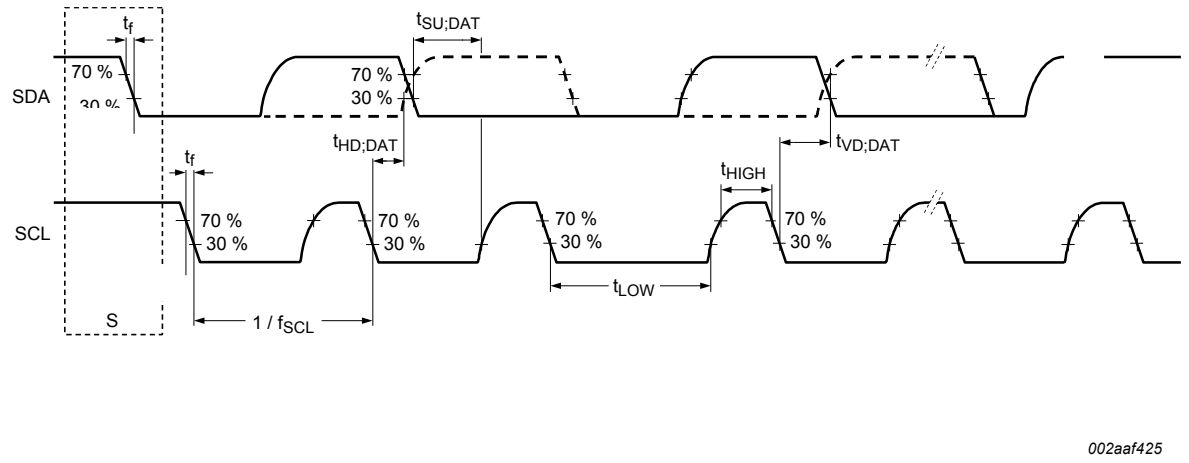


Fig 20. I²C-bus pins clock timing

11.10 SPI interfaces

The actual SPI bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI master mode is 71 Mbit/s, and the maximum supported bit rate for SPI slave mode is 21 Mbit/s.

Table 27. SPI dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; C_L = 30 pF balanced loading on all pins; SLEW = standard mode. Parameters sampled at the 50 % level of the rising or falling edge.

Symbol	Parameter	Conditions		Min	Max	Unit
SPI master 1.62V ≤ VDD ≤ 2.0 V						
t_{DS}	data set-up time	CCLK = 1 MHz to 12 MHz		0	-	ns
		CCLK = 48 MHz to 60 MHz		0	-	ns
		CCLK = 96 MHz		0	-	ns
t_{DH}	data hold time	CCLK = 1 MHz to 12 MHz		14	-	ns
		CCLK = 48 MHz to 60 MHz		12	-	ns
		CCLK = 96 MHz		9	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz		0	7	ns
		CCLK = 48 MHz to 60 MHz		0	2	ns
		CCLK = 96 MHz		0	2	ns
SPI slave 1.62V ≤ VDD ≤ 2.0 V						
t_{DS}	data set-up time	CCLK = 1 MHz to 12 MHz		22	-	ns
		CCLK = 48 MHz to 60 MHz		4	-	ns
		CCLK = 96 MHz		4	-	ns
t_{DH}	data hold time	CCLK = 1 MHz to 12 MHz		0	-	ns
		CCLK = 48 MHz to 60 MHz		0	-	ns
		CCLK = 96 MHz		0	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz		46	70	ns
		CCLK = 48 MHz to 60 MHz		30	37	ns
		CCLK = 96 MHz		30	36	ns
SPI master 2.7 V ≤ VDD ≤ 3.6 V						
t_{DS}	data set-up time	CCLK = 1 MHz to 12 MHz		0	-	ns
		CCLK = 48 MHz to 60 MHz		0	-	ns
		CCLK = 96 MHz		0	-	ns
t_{DH}	data hold time	CCLK = 1 MHz to 12 MHz		10	-	ns
		CCLK = 48 MHz to 60 MHz		8	-	ns
		CCLK = 96 MHz		7	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz		0	6	ns
		CCLK = 48 MHz to 60 MHz		0	1	ns
		CCLK = 96 MHz		0	1	ns
SPI slave 2.7V ≤ VDD ≤ 3.6 V						
t_{DS}	data set-up time	CCLK = 1 MHz to 12 MHz		21	-	ns
		CCLK = 48 MHz to 60 MHz		4	-	ns
		CCLK = 96 MHz		3	-	ns

Table 27. SPI dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; C_L = 30 pF balanced loading on all pins; SLEW = standard mode. Parameters sampled at the 50 % level of the rising or falling edge.

Symbol	Parameter	Conditions		Min	Max	Unit
t_{DH}	data hold time	CCLK = 1 MHz to 12 MHz		0	-	ns
		CCLK = 48 MHz to 60 MHz		0	-	ns
		CCLK = 96 MHz		0	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz		36	61	ns
		CCLK = 48 MHz to 60 MHz		21	22	ns
		CCLK = 96 MHz		20	21	ns

[1] *Based on characterization; not tested in production.*

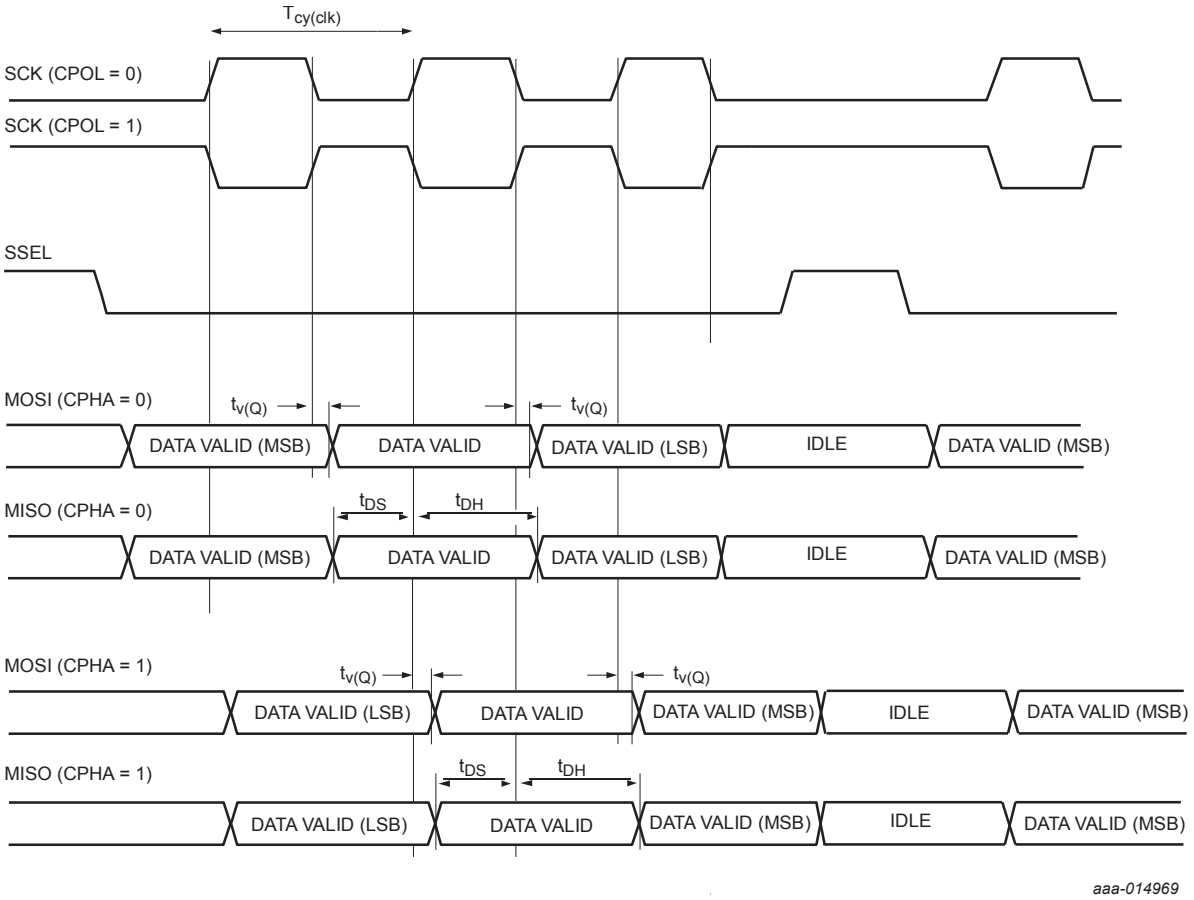


Fig 21. SPI master timing

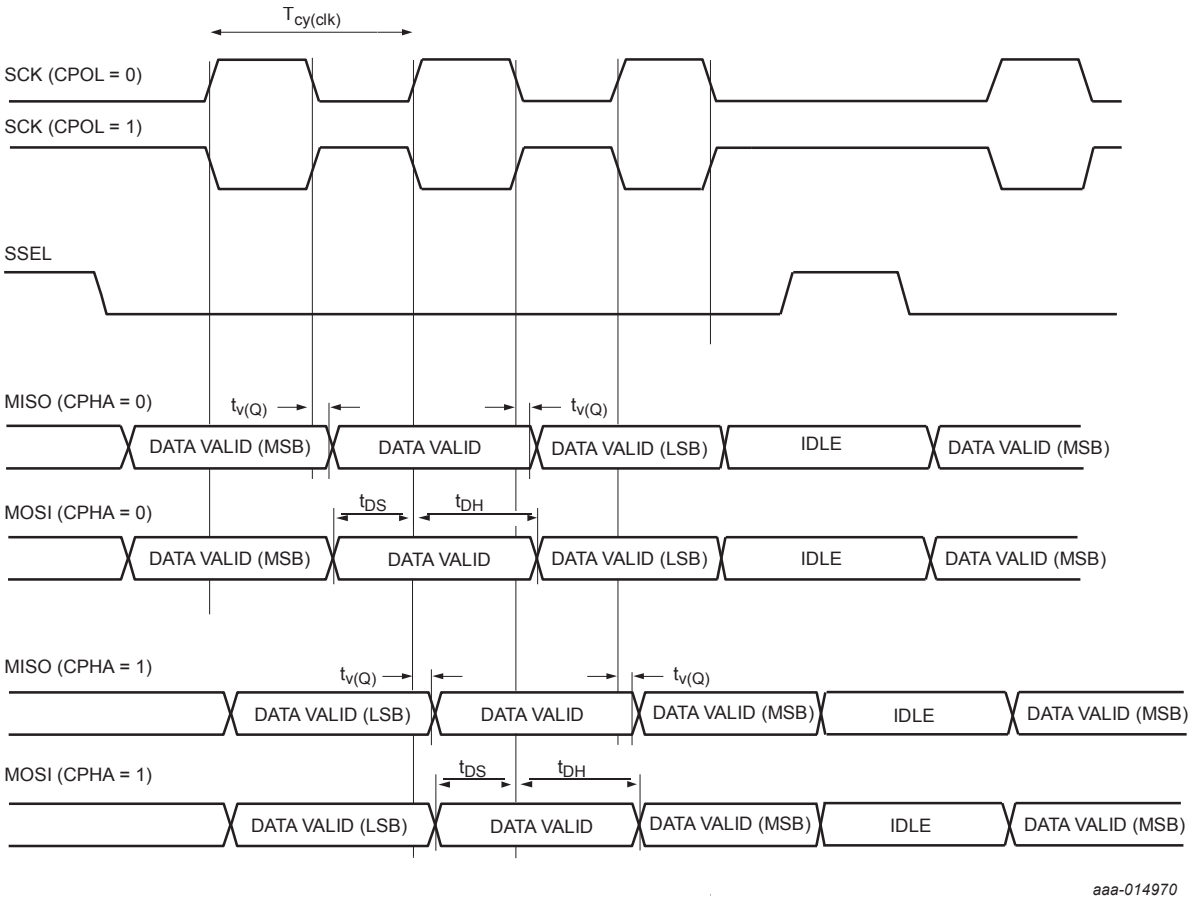


Fig 22. SPI slave timing

11.11 USART interface

The actual USART bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for USART master and slave synchronous modes is 24 Mbit/s.

Table 28. USART dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; 1.62 V ≤ V_{DD} ≤ 3.6 V; C_L = 30 pF balanced loading on all pins; SLEW = standard mode. Parameters sampled at the 50% level of the falling or rising edge.

Symbol	Parameter	Conditions	Min	Max	Unit
USART master (in synchronous mode) 1.62V ≤ VDD ≤ 2.0 V					
$t_{su(D)}$	data input set-up time	CCLK = 1 MHz to 12 MHz	65	-	ns
		CCLK = 48 MHz to 60 MHz	35	-	ns
		CCLK = 96 MHz	34	-	ns
$t_{h(D)}$	data input hold time	CCLK = 1 MHz to 12 MHz	0	-	ns
		CCLK = 48 MHz to 60 MHz	0	-	ns
		CCLK = 96 MHz	0	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz	0	8	ns
		CCLK = 48 MHz to 60 MHz	0	2	ns
		CCLK = 96 MHz	0	2	ns
USART slave (in synchronous mode) 1.62V ≤ VDD ≤ 2.0 V					
$t_{su(D)}$	data input set-up time	CCLK = 1 MHz to 12 MHz	18	-	ns
		CCLK = 48 MHz to 60 MHz	5	-	ns
		CCLK = 96 MHz	4	-	ns
$t_{h(D)}$	data input hold time	CCLK = 1 MHz to 12 MHz	0	-	ns
		CCLK = 48 MHz to 60 MHz	0	-	ns
		CCLK = 96 MHz	0	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz	50	65	ns
		CCLK = 48 MHz to 60 MHz	35	40	ns
		CCLK = 96 MHz	30	36	ns
USART master (in synchronous mode) 2.7V ≤ VDD ≤3.6V					
$t_{su(D)}$	data input set-up time	CCLK = 1 MHz to 12 MHz	61	-	ns
		CCLK = 48 MHz to 60 MHz	22	-	ns
		CCLK = 96 MHz	21	-	ns
$t_{h(D)}$	data input hold time	CCLK = 1 MHz to 12 MHz	0	-	ns
		CCLK = 48 MHz to 60 MHz	0	-	ns
		CCLK = 96 MHz	0	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz	0	7	ns
		CCLK = 48 MHz to 60 MHz	1	2	ns
		CCLK = 96 MHz	1	2	ns

Table 28. USART dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; 1.62 V ≤ V_{DD} ≤ 3.6 V; C_L = 30 pF balanced loading on all pins; SLEW = standard mode. Parameters sampled at the 50% level of the falling or rising edge.

Symbol	Parameter	Conditions	Min	Max	Unit
USART slave (in synchronous mode) 2.7V ≤ VDD ≤ 3.6 V					
$t_{su(D)}$	data input set-up time	CCLK = 1 MHz to 12 MHz	21	-	ns
		CCLK = 48 MHz to 60 MHz	5	-	ns
		CCLK = 96 MHz	4	-	ns
$t_{h(D)}$	data input hold time	CCLK = 1 MHz to 12 MHz	0	-	ns
		CCLK = 48 MHz to 60 MHz	0	-	ns
		CCLK = 96 MHz	0	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz	37	62	ns
		CCLK = 48 MHz to 60 MHz	22	25	ns
		CCLK = 96 MHz	19	21	ns

[1] *Based on characterization; not tested in production.*

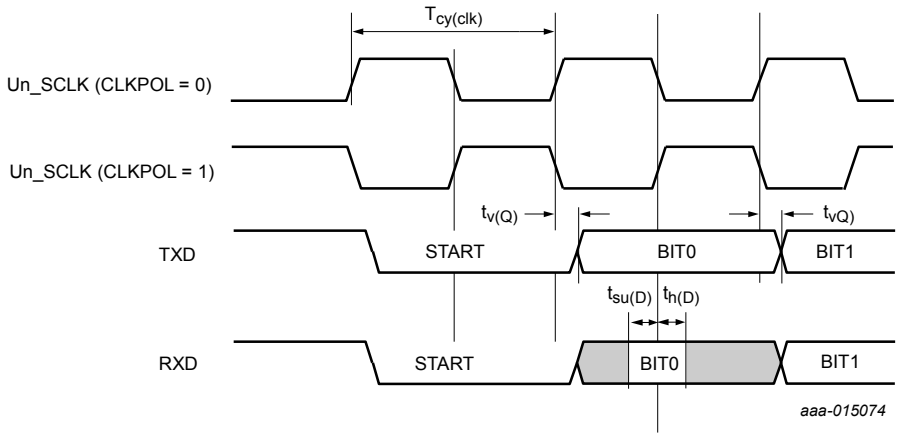


Fig 23. USART timing

11.12 SCTimer/PWM output timing

Table 29. SCTimer/PWM output dynamic characteristics

T_{amb} = −40 °C to 105 °C; 1.62 V ≤ V_{DD} ≤ 3.6 V C_L = 30 pF. Simulated skew (over process, voltage, and temperature) of any two SCT fixed-pin output signals; sampled at 10 % and 90 % of the signal level; values guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{sk(o)}$	output skew time	-	-	-	3.0	ns

12. Analog characteristics

12.1 BOD

Table 30. BOD static characteristics

T_{amb} = 25 °C; based on characterization; not tested in production.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 0					
		assertion		-	2.05	-	V
		de-assertion		-	2.20	-	V
V_{th}	threshold voltage	interrupt level 1					
		assertion		-	2.45	-	V
		de-assertion		-	2.60	-	V
		reset level 1					
		assertion		-	1.85	-	V
		de-assertion		-	2.00	-	V
V_{th}	threshold voltage	interrupt level 2					
		assertion		-	2.75	-	V
		de-assertion		-	2.90	-	V
		reset level 2					
		assertion		-	2.00	-	V
		de-assertion		-	2.15	-	V
V_{th}	threshold voltage	interrupt level 3					
		assertion		-	3.05	-	V
		de-assertion		-	3.20	-	V
		reset level 3					
		assertion		-	2.30	-	V
		de-assertion		-	2.45	-	V

12.2 12-bit ADC characteristics

Table 31. 12-bit ADC static characteristics

T_{amb} = −40 °C to +105 °C; 1.62 V ≤ V_{DD} ≤ 3.6 V; VREFP = V_{DDA}; V_{SSA} = VREFN = GND. ADC calibrated at T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
V_{IA}	analog input voltage		[3]	0	-	V_{DDA}	V
C_{ia}	analog input capacitance		[4]	-	5	-	pF
$f_{clk(ADC)}$	ADC clock frequency				-	80	MHz
f_s	sampling frequency			-	-	5.0	Msamples/s
E_D	differential linearity error	V_{DDA} = VREFP = 1.62 V	[1][5]	-	±3	-	LSB
		V_{DDA} = VREFP = 3.6 V			±2		LSB
$E_{L(adj)}$	integral non-linearity	V_{DDA} = VREFP = 1.62 V	[1][6]	-	±5	-	LSB
		V_{DDA} = VREFP = 3.6 V		-	±2	-	LSB
E_O	offset error	calibration enabled	[1][7]	-	±5.6	-	mV
$V_{err(FS)}$	full-scale error voltage	V_{DDA} = VREFP = 1.62 V	[1][8]	-	±3		LSB
		V_{DDA} = VREFP = 3.6 V		-	±3		LSB
Z_i	input impedanc	f_s = 5.0 Msamples/s	[9][10]	17.0	-	-	kΩ

[1] Based on characterization; not tested in production.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] The input resistance of ADC channels 6 to 11 is higher than ADC channels 0 to 5.

[4] C_{ia} represents the external capacitance on the analog input channel for sampling speeds of 5.0 Msamples/s. No parasitic capacitances included.

[5] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 24.

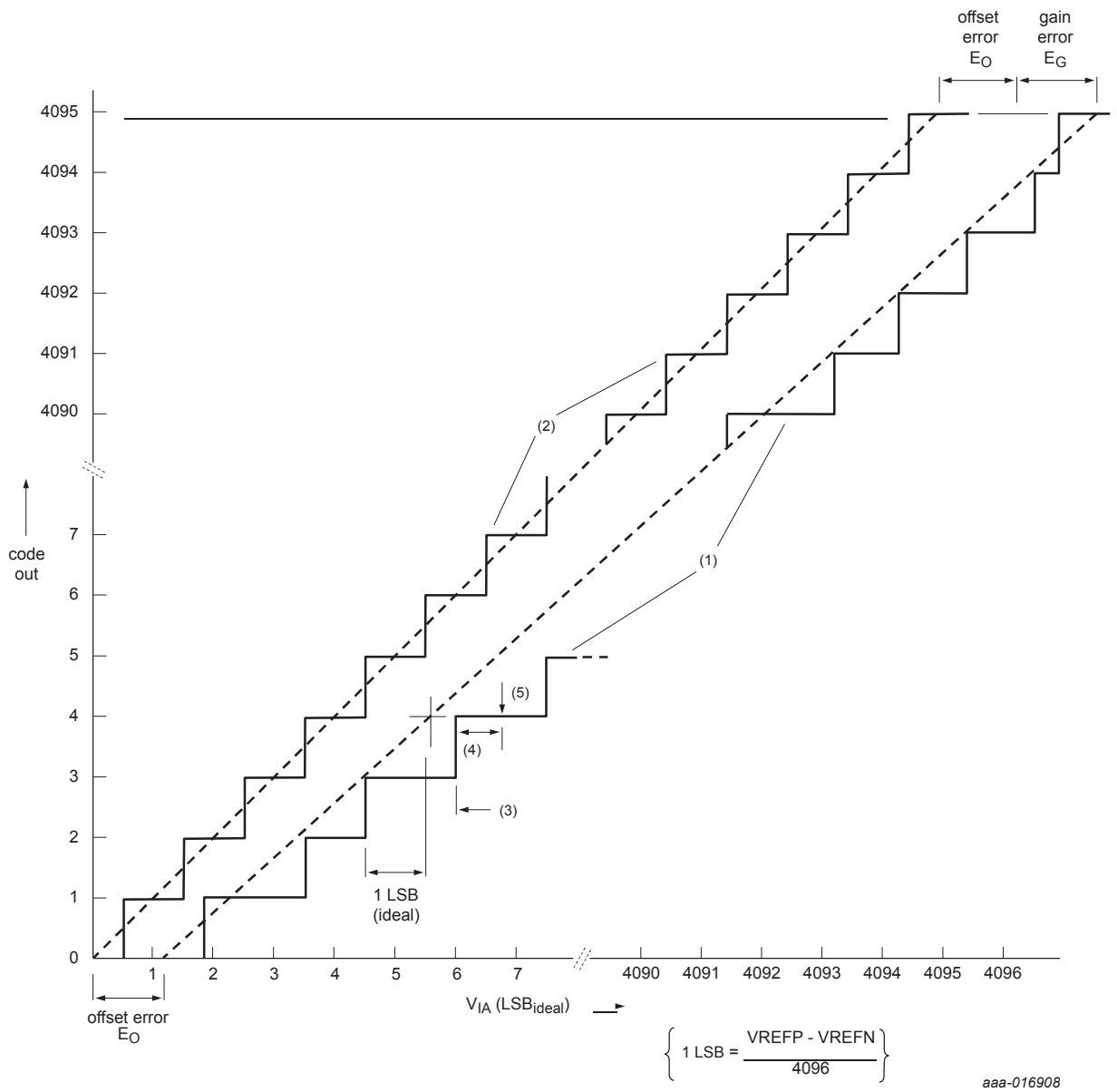
[6] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 24.

[7] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 24.

[8] The full-scale error voltage or gain error (E_G) is the difference between the straight-line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 24.

[9] T_{amb} = 25 °C; maximum sampling frequency f_s = 5.0 Msamples/s and analog input capacitance C_{ia} = 5 pF.

[10] Input impedance Z_i is inversely proportional to the sampling frequency and the total input capacity including C_{ia} and C_{io}: $Z_i \propto 1 / (f_s \times C_i)$. See Table 16 for C_{io}. See Figure 25.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 24. 12-bit ADC characteristics

Table 32. ADC sampling times[1]

-40 °C ≤ T_{amb} ≤ 85 °C; 1.62 V ≤ V_{DDA} ≤ 3.6 V; 1.62 V ≤ V_{DD} ≤ 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 12 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	20	-	-	ns
		0.05 kΩ ≤ Z_o < 0.1 kΩ		23	-	-	ns
		0.1 kΩ ≤ Z_o < 0.2 kΩ		26	-	-	ns
		0.2 kΩ ≤ Z_o < 0.5 kΩ		31	-	-	ns
		0.5 kΩ ≤ Z_o < 1 kΩ		47	-	-	ns
		1 kΩ ≤ Z_o < 5 kΩ		75	-	-	ns
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 10 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	15	-	-	ns
		0.05 kΩ ≤ Z_o < 0.1 kΩ		18	-	-	ns
		0.1 kΩ ≤ Z_o < 0.2 kΩ		20	-	-	ns
		0.2 kΩ ≤ Z_o < 0.5 kΩ		24	-	-	ns
		0.5 kΩ ≤ Z_o < 1 kΩ		38	-	-	ns
		1 kΩ ≤ Z_o < 5 kΩ		62	-	-	ns
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 8 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	12	-	-	ns
		0.05 kΩ ≤ Z_o < 0.1 kΩ		13	-	-	ns
		0.1 kΩ ≤ Z_o < 0.2 kΩ		15	-	-	ns
		0.2 kΩ ≤ Z_o < 0.5 kΩ		19	-	-	ns
		0.5 kΩ ≤ Z_o < 1 kΩ		30	-	-	ns
		1 kΩ ≤ Z_o < 5 kΩ		48	-	-	ns
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 6 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	9	-	-	ns
		0.05 kΩ ≤ Z_o < 0.1 kΩ		10	-	-	ns
		0.1 kΩ ≤ Z_o < 0.2 kΩ		11	-	-	ns
		0.2 kΩ ≤ Z_o < 0.5 kΩ		13	-	-	ns
		0.5 kΩ ≤ Z_o < 1 kΩ		22	-	-	ns
		1 kΩ ≤ Z_o < 5 kΩ		36	-	-	ns
ADC inputs ADC_11 to ADC_6 (slow channels); ADC resolution = 12 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	43	-	-	ns
		0.05 kΩ ≤ Z_o < 0.1 kΩ		46	-	-	ns
		0.1 kΩ ≤ Z_o < 0.2 kΩ		50	-	-	ns
		0.2 kΩ ≤ Z_o < 0.5 kΩ		56	-	-	ns
		0.5 kΩ ≤ Z_o < 1 kΩ		74	-	-	ns
		1 kΩ ≤ Z_o < 5 kΩ		105	-	-	ns

Table 32. ADC sampling times[1] *...continued*

-40 °C ≤ T_{amb} ≤ 85 °C; 1.62 V ≤ V_{DDA} ≤ 3.6 V; 1.62 V ≤ V_{DD} ≤ 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ADC inputs ADC_11 to ADC_6 (slow channels); ADC resolution = 10 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	35	-	-	ns
		0.05 kΩ ≤ Z_o < 0.1 kΩ		38	-	-	ns
		0.1 kΩ ≤ Z_o < 0.2 kΩ		40	-	-	ns
		0.2 kΩ ≤ Z_o < 0.5 kΩ		46	-	-	ns
		0.5 kΩ ≤ Z_o < 1 kΩ		61	-	-	ns
		1 kΩ ≤ Z_o < 5 kΩ		86	-	-	ns
ADC inputs ADC_11 to ADC_6 (slow channels); ADC resolution = 8 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	27	-	-	ns
		0.05 kΩ ≤ Z_o < 0.1 kΩ		29	-	-	ns
		0.1 kΩ ≤ Z_o < 0.2 kΩ		32	-	-	ns
		0.2 kΩ ≤ Z_o < 0.5 kΩ		36	-	-	ns
		0.5 kΩ ≤ Z_o < 1 kΩ		48	-	-	ns
		1 kΩ ≤ Z_o < 5 kΩ		69	-	-	ns
ADC inputs ADC_11 to ADC_6 (slow channels); ADC resolution = 6 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	20	-	-	ns
		0.05 kΩ ≤ Z_o < 0.1 kΩ		22	-	-	ns
		0.1 kΩ ≤ Z_o < 0.2 kΩ		23	-	-	ns
		0.2 kΩ ≤ Z_o < 0.5 kΩ		26	-	-	ns
		0.5 kΩ ≤ Z_o < 1 kΩ		36	-	-	ns
		1 kΩ ≤ Z_o < 5 kΩ		51	-	-	ns

[1] Characterized through simulation. Not tested in production.

[2] The ADC default sampling time is 2.5 ADC clock cycles. To match a given analog source output impedance, the sampling time can be extended by adding up to seven ADC clock cycles for a maximum sampling time of 9.5 ADC clock cycles. See the TSAMP bits in the ADC CTRL register.

[3] Z_o = analog source output impedance.

12.2.1 ADC input impedance

Figure 25 shows the ADC input impedance. In this figure:

- ADCx represents slow ADC input channels 6 to 11.
- ADCy represents fast ADC input channels 0 to 5.
- R_1 and R_{sw} are the switch-on resistance on the ADC input channel.
- If fast channels (ADC inputs 0 to 5) are selected, the ADC input signal goes through R_{sw} to the sampling capacitor (C_{ia}).
- If slow channels (ADC inputs 6 to 11) are selected, the ADC input signal goes through $R_1 + R_{sw}$ to the sampling capacitor (C_{ia}).
- Typical values, R_1 = 487 Ω, R_{sw} = 278 Ω
- See Table 16 for C_{io}.
- See Table 31 for C_{ia}.

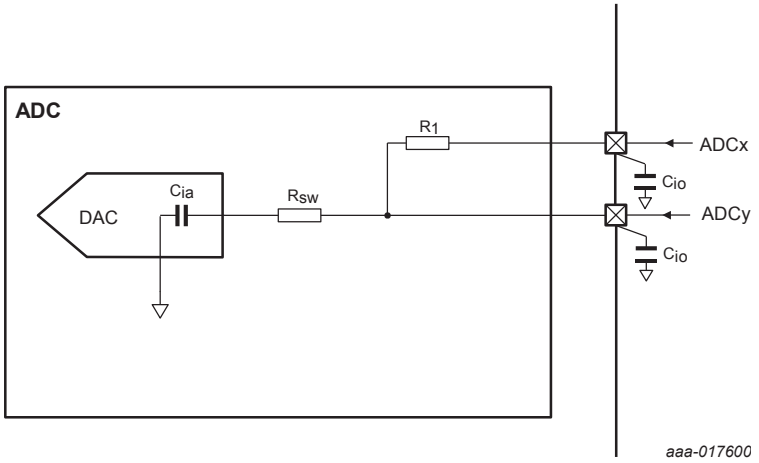


Fig 25. ADC input impedance

13. Application information

13.1 Start-up behavior

Figure 26 shows the start-up timing after reset. The IRC 12 MHz oscillator provides the default clock at Reset and provides a clean system clock shortly after the supply pins reach operating voltage.

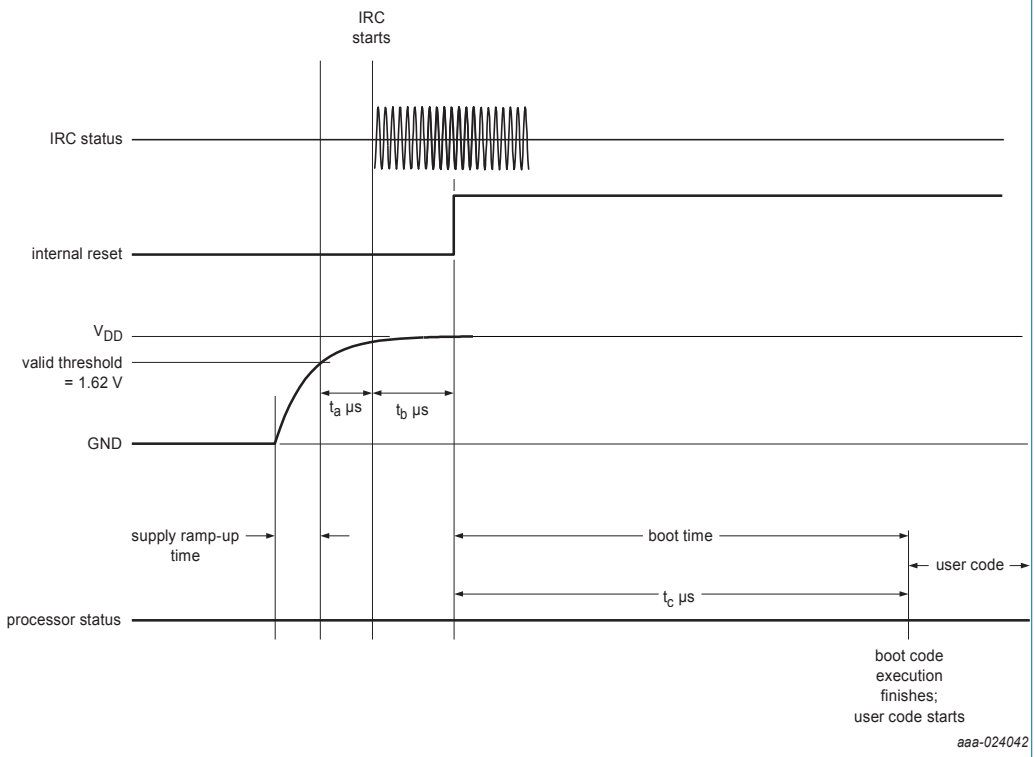


Fig 26. Start-up timing

Table 33. Typical start-up timing parameters

Parameter	Description	Value
t_a	IRC start time	≤ 20 µs
t_b	Internal reset de-asserted	151 µs
t_c	Boot time	68 µs

13.2 Standard I/O pin configuration

Figure 27 shows the possible pin modes for standard I/O pins:

- Digital output driver: with configurable open-drain output.
- Digital input: pull-up resistor (PMOS device) enabled/disabled.
- Digital input: pull-down resistor (NMOS device) enabled/disabled.
- Digital input: repeater mode enabled/disabled.
- Digital input: programmable input digital filter and input inverter.
- Analog input: selected through IOCON register.

The default configuration for standard I/O pins is input with pull-up resistor enabled. The weak MOS devices provide a drive capability equivalent to pull-up and pull-down resistors.

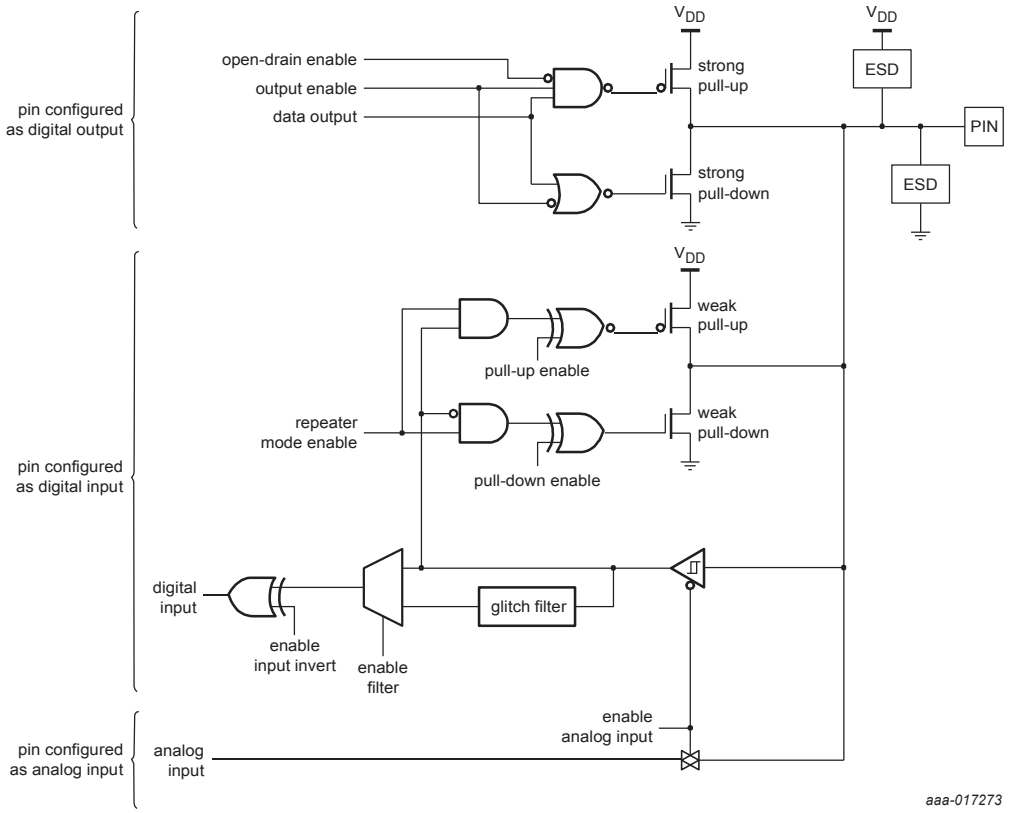
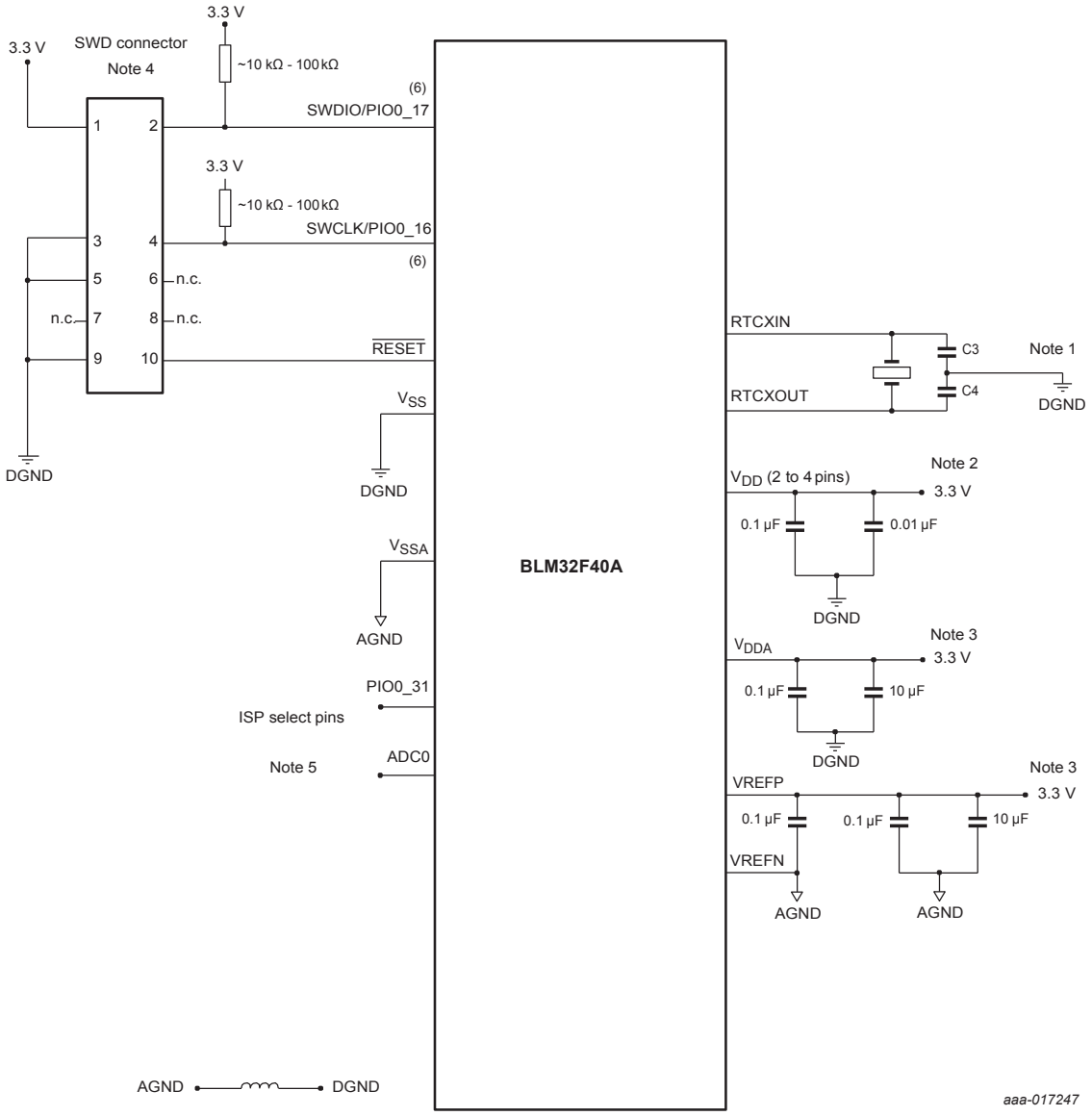


Fig 27. Standard I/O pin configuration

13.3 Connecting power, clocks, and debug functions



(1) See Section 13.5 “RTC oscillator” for the values of C3 and C4.

(2) Position the decoupling capacitors of 0.1 µF and 0.01 µF as close as possible to the V_{DD} pin. Add one set of decoupling capacitors to each V_{DD} pin.

(3) Position the decoupling capacitors of 0.1 µF as close as possible to the VREFN and V_{DDA} pins. The 10 µF bypass capacitor filters the power line. Tie V_{DDA} and VREFP to V_{DD} if the ADC is not used. Tie VREFN to V_{SS} if ADC is not used.

(4) Uses the ARM 10-pin interface for SWD.

(5) When measuring signals of low frequency, use a low-pass filter to remove noise and to improve ADC performance. Also see Ref. 3.

(6) External pull-up resistors on SWDIO and SWCLK pins are optional because these pins have an internal pull-up enabled by default.

Fig 28. Power, clock, and debug connections

13.4 I/O power consumption

I/O pins can contribute to the overall static and dynamic power consumption of the part.

If pins are configured as digital inputs with the pull-up resistor enabled, a static current can flow depending on the voltage level at the pin. This current can be calculated using the parameters I_{pu} and I_{pd} given in Table 16.

If pins are configured as digital outputs, the static current is derived from parameters IOH and IOL shown in Table 16, and any external load connected to the pin.

When an I/O pin switches in an application, it contributes to the dynamic power consumption because the VDD supply provides the current to charge and discharge all internal and external capacitive loads connected to the pin.

The contribution from the I/O switching current I_{sw} can be calculated as follows for any given switching frequency f_{sw} if the external capacitive load (C_{ext}) is known (see Table 16 for the internal I/O capacitance):

$$I_{sw} = V_{DD} \times f_{sw} \times (C_{io} + C_{ext})$$

13.5 RTC oscillator

In the RTC oscillator circuit, only the crystal (XTAL) and the capacitances C_{X1} and C_{X2} need to be connected externally on the RTCXIN and RTCXOUT pins. See Figure 29.

An external clock can be connected to RTCX1 if RTCX2 is left open. The recommended amplitude of the clock signal is $V_{i(RMS)}$ = 100 mV to 200 mV with a coupling capacitance of 5 pF to 10 pF.

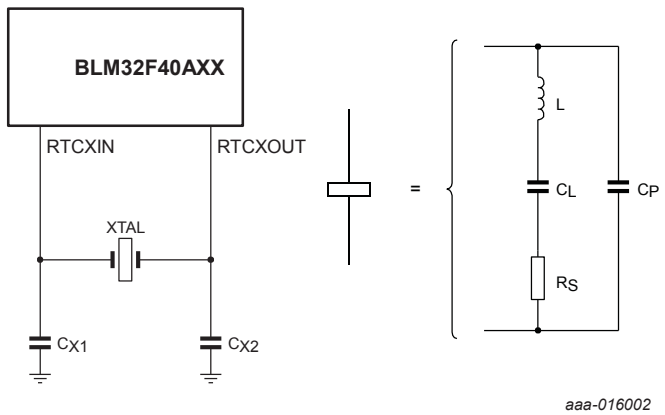


Fig 29. RTC oscillator components

For best results, it is very critical to select a matching crystal for the on-chip oscillator. Load capacitance (C_L), series resistance (R_S), and drive level (D_L) are important parameters to consider while choosing the crystal. After selecting the proper crystal, the external load capacitor C_{X1} and C_{X2} values can also be generally determined by the following expression:

$$C_{X1} = C_{X2} = 2C_L - (C_{Pad} + C_{Parasitic})$$

Where:

C_L - Crystal load capacitance

C_{Pad} - Pad capacitance of the RTCXIN and RTCXOUT pins (~3 pF).

$C_{Parasitic}$ – Parasitic or stray capacitance of external circuit.

Although $C_{Parasitic}$ can be ignored in general, the actual board layout and placement of external components influences the optimal values of external load capacitors. Therefore, it is recommended to fine tune the values of external load capacitors on actual hardware board to get the accurate clock frequency. For fine tuning, output the RTC Clock to one of the GPIOs and optimize the values of external load capacitors for minimum frequency deviation.

Table 34. Recommended values for the RTC external 32.768 kHz oscillator C_L, R_S, D_L, and C_{X1}/C_{X2} components

Crystal load capacitance C_L	Maximum crystal series resistance R_S	Maximum crystal drive level D_L	External load capacitors C_{X1}/C_{X2}
12.5 pF	< 70 kΩ	0.5 μW	22 pF, 22 pF

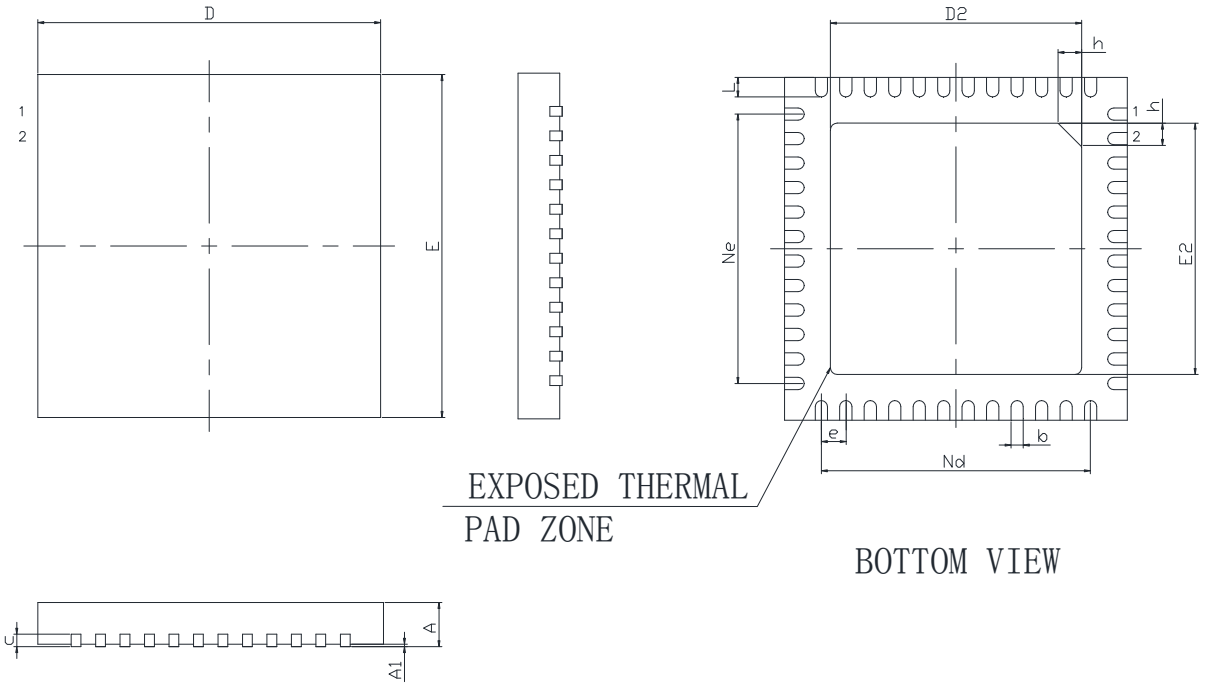
Remark: The crystals with lower CL (< 12.5 pF) values are not recommended.

13.5.1 RTC Printed Circuit Board (PCB) design guidelines

- Connect the crystal and external load capacitors on the PCB as close as possible (within 20 mm) to the oscillator input and output pins of the chip.
- The length of traces in the oscillation circuit should be as short as possible and must not cross other signal lines.
- Ensure that the load capacitors CX1, CX2, and CX3, in case of third overtone crystal usage, have a common ground plane.
- Loops must be made as small as possible to minimize the noise coupled in through the PCB and to keep the parasitics as small as possible.
- Lay out the ground (GND) pattern under crystal unit.
- Do not lay out other signal lines under crystal unit for multi-layered PCB.

14. Package outline

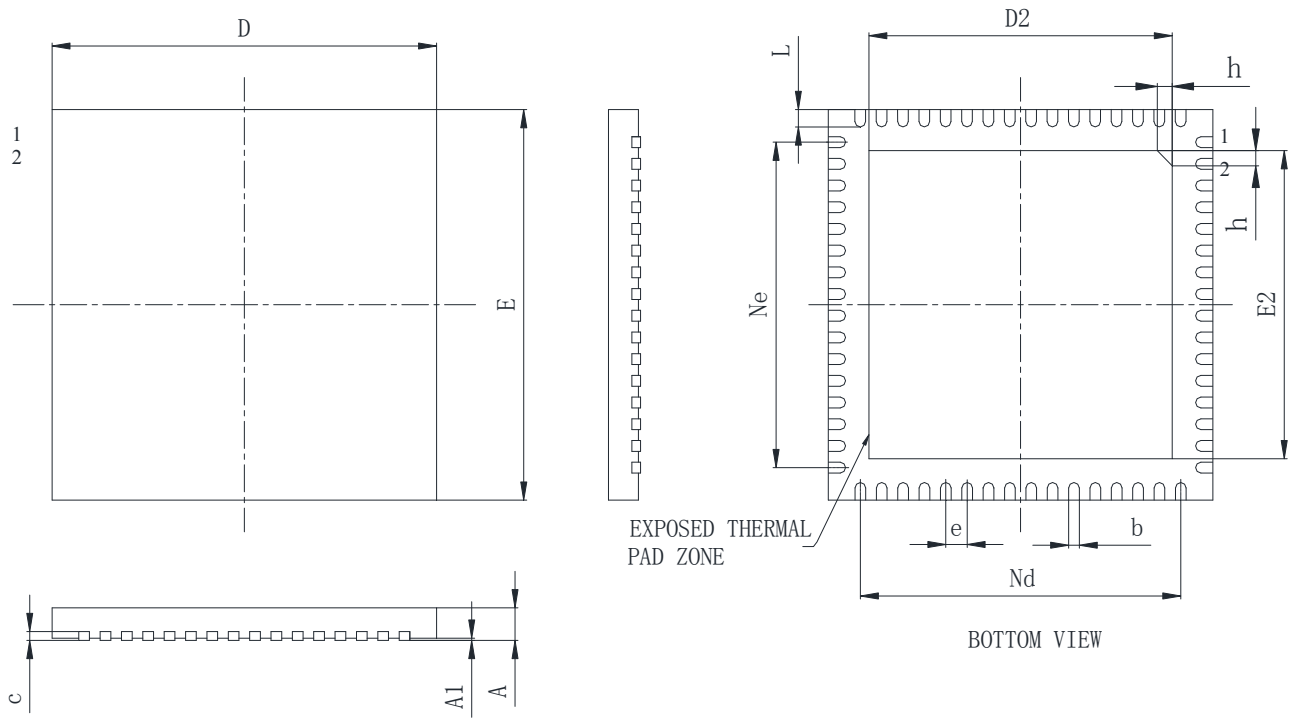
QFN48: 6.0x 6.0 x 0.85 mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.75	0.85	0.85
A1	--	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.23
D	5.90	6.00	6.10
D2	4.10	4.20	4.30
e	0.40 BSC		
Ne	4.40 BSC		
Nd	4.40 BSC		
E	5.90	6.00	6.10
E2	4.10	4.20	4.30
L	0.35	0.40	0.45
h	0.30	0.35	0.40

Fig 30. QFN48 Package outline

QFN64: body 9.0 x 9.0x 0.85 mm

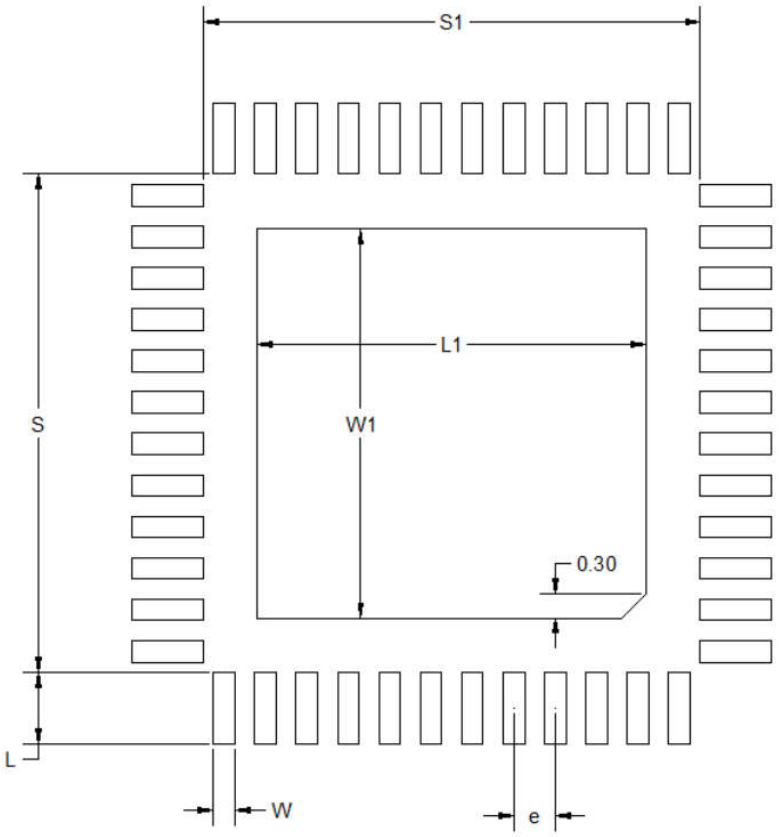


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	--	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	8.90	9.00	9.10
D2	7.00	7.10	7.20
e	0.50 BSC		
Ne	7.50 BSC		
Nd	7.50 BSC		
E	8.90	9.00	9.10
E2	7.00	7.10	7.20
L	0.35	0.40	0.45
h	0.30	0.35	0.40

Fig 31. QFN64 Package outline

15. PCB Land Pattern Dimensions

Footprint information for reflow PCB Land Pattern of QFN48 package

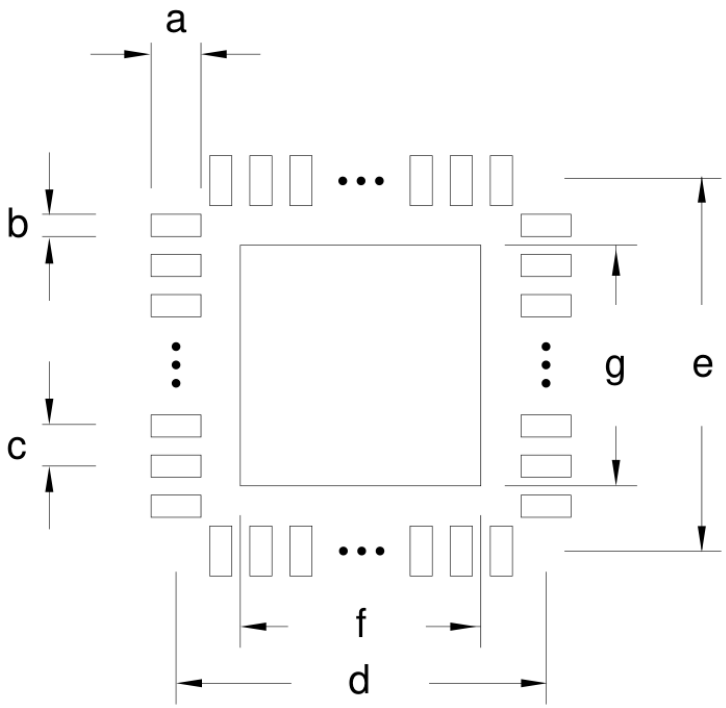


QFN48 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Dim. (mm)
S1	4.95	e	0.40
S	4.95	W	0.20
L1	4.20	L	0.85
W1	4.20		

Fig 32. QFN48 PCB Land Pattern footprint

Footprint information for reflow PCB Land Pattern of QFN64 package



QFN64 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Dim. (mm)
a	0.75	e	8.90
b	0.25	f	7.10
c	0.50	g	7.10
d	8.90		

Fig 33. QFN64 PCB Land Pattern footprint

16. Abbreviations

Table 35. Abbreviations

Acronym	Description
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
API	Application Programming Interface
DMA	Direct Memory Access
GPIO	General Purpose Input/Output
IRC	Internal RC
LSB	Least Significant Bit
MCU	MicroController Unit
PLL	Phase-Locked Loop
SPI	Serial Peripheral Interface
TTL	Transistor-Transistor Logic
USART	Universal Asynchronous Receiver/Transmitter

17. References

[1] BLM32F40AXX User manual UM10850:

http://www.blestech.com/documents/user_manual/UM10850.pdf

[2] BLM32F40AXX Errata sheet:

http://www.blestech.com/documents/errata_sheet/ES_BLM32F40AXX.pdf

[3] Technical note ADC design guidelines:

http://www.blestech.com/documents/technical_note/TN00009.pdf

18. Revision history

32-bit ARM Cortex-M4/M0+ microcontroller

Table 36. Revision history *...continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLM32F40AXX v2.3	20180703	Product data sheet	-	BLM32F40AXX v2.2
Modification:	• Update	Modify clerical error		
BLM32F40AXX v2.2	20171118	Product data sheet	-	BLM32F40AXX v2.1
Modification:	• Update PCB Land Pattern of QFN64 package			
BLM32F40AXX v2.1	20171102	Product data sheet		BLM32F40AXX v2.0
Modification:	• Product packaging changes to QFN48 and QFN64			
BLM32F40AXX v2.0	20170426	Product data sheet	-	BLM32F40AXX v1.1
Modification:	• Updated the ADC conversion rate from 4.8 Msamples/s to 5.0 Msamples/s. • Added Section 7.14 “Pin interrupt/pattern engine”. • Added Section 7.18.6 “Repetitive Interrupt Timer (RIT)”. • Updated Table 12 “Static characteristics: Power consumption in deep sleep, power down, and deep power-down modes” on page 44. • Updated Table 15 “Static characteristics: pin characteristics” on page 49: – T_{amb} = −40 °C to +105 °C, unless otherwise specified. 1.62 V ≤ V_{DD} ≤ 3.6 V. – updated min and max values. • Added Section 11.1 “Power-up ramp conditions”. • Added Section 11.9 “SPI interfaces”, Section 11.10 “USART interface”, and Section 11.11 “SCTimer/PWM output timing”. • Updated Section 11.5 “IRC”: – added temperature conditions: T_{amb} = 25 °C, −40 °C ≤ T_{amb} ≤ +105 °C – updated min and max values. • Added Table 14 “Typical peripheral power consumption”. • Added Table 28 “12-bit ADC static characteristics”: – T_{amb} = −40 °C to +105 °C. – Values for E_D, $E_{L(adj)}$, E_O, and $V_{err(FS)}$. • Added Section 12.2.1 “ADC input impedance” • Updated Figure 26 “Standard I/O pin configuration” on page 71 • Minor updates to Section 13.3 “I/O power consumption”.			
BLM32F40AXX v1.1	20161117	Product data sheet	-	BLM32F40AXX v1.0
Modification:	• Minor editorial update in Section 1.			
BLM32F40AXX v1.0	20161106	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www. blestech.com.

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21. Contents

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