HW4_Report

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1. Describe the input fields of each pipeline register
Ans:

register	**input field**
IFID	instruction
IDEX	9 bit control signal(including 3 bits op code) RSdata RTdata sign-extend rt rd shift amount function code
EXMEM	4 bit control signal result of ALU RTdata the destination of writeback
MEMWB	the signal of MemToReg and RegWrite read data from data memory RTdata the destination of writeback

2. Explain your control signals in the sixth cycle(both test data test_1.txt and test_2.txt are needed)
Ans:

Test1	
RegWrite	0
ALUSrc	1
RegDst	0
ALUOp	010(RType)
func	0000(and)
MemWrite	0
MemRead	0
MemToReg	0

Test2	
RegWrite	1
ALUSrc	1
RegDst	0
ALUOp	011(addi)
func	0010(add)
MemWrite	0
MemRead	0
MemToReg	0