

Naif Tarafdar

CONTACT INFORMATION

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RESEARCH INTERESTS

Data centers, heterogeneous computing, field-programmable gate-arrays (FPGAs), virtualization, abstraction layers, compute clusters, high-performance computing

EDUCATION

Ph.D. in Computer Engineering September, 2016 - Present
University of Toronto *Toronto, Ontario, Canada*
Dissertation: “Developing a Hardware Stack for Heterogeneous Data Centers”
Advisor: Paul Chow

M.A.Sc in Computer Engineering September, 2014 - September, 2016
University of Toronto *Toronto, Ontario, Canada*
Thesis: “Enabling Flexible Network FPGA Clusters in a Heterogeneous Data Center”
Advisor: Paul Chow

B.A.Sc with Honours in Computer Engineering September, 2009 - May, 2013
University of Toronto *Toronto, Ontario, Canada*

INDUSTRY AND RESEACH EXPERIENCE

Xilinx Research San Jose, California, USA
Visiting Scholar *July, 2018*
(*Verilog, C++, C, Vivado HLS, Python*)
I worked on integrating an optimized Xilinx Machine Learning Engine into my PhD research of a multi-FPGA and CPU framework.

Xilinx Research San Jose, California, USA
Machine Learning Intern *August, 2017 - December, 2017*
(*Verilog, C++, C, Vivado HLS, Python, TensorFlow, Caffe*)
I designed, synthesized, and emulated, machine learning cores for high throughput, low-latency applications. I also worked on integrating these cores into popular software frameworks to make these cores accessible to software developers.

IBM Canada Toronto, Ontario, Canada
Hardware Acceleration Lab Intern *May, 2012 - September, 2013*
(*Verilog, C++, OpenCL*)
I optimized large-scale software projects CPU optimizations with the use of hardware accelerators and low-level software optimizations.

AWARDS & SCHOLARSHIPS

Queen Elizabeth II/Victoria Noakes Graduate Scholarship in Science and Technology
\$15,000 2018
Awarded for excellence in graduate studies.

Ontario Graduate Scholarship - \$15,000 2016
Awarded for excellence in graduate studies.

Edward S Rogers Sr. Graduate Scholarships - \$27,400 2016
Awarded for excellence in graduate studies.

Edward S Rogers Sr. Admission Scholarship - \$4000

2009

Entry scholarship awarded to Undergrads at the University of Toronto.

CONFERENCE
PUBLICATIONS

N. Tarafdar, T. Lin, N. Eskandari, D. Lion, A. Leon-Garcia, and P. Chow. *Heterogeneous Virtualized Network Function Framework in the Data Center*. In 27th International Conference on Field Programmable Logic and Applications (FPL 2017), September 2017.

T. Lin, **N. Tarafdar**, B. Park, P. Chow, and A. Leon-Garcia. *Enabling Network Function Virtualization over Heterogeneous Resources*. In The 19th Asia-Pacific Network Operations and Management Symposium (APNOMS2017), Seoul, South Korea, September 2017.

N. Tarafdar, T. Lin, E. Fukuda, H. Bannazadeh, A. Leon-Garcia, and P. Chow. *Enabling Flexible Network FPGA Clusters in a Heterogeneous Cloud Data Center*. In International Symposium on Field-Programmable Gate Arrays (FPGA). ACM, February 2017.

S. Byma, **N. Tarafdar**, T. Xu, H. Bannazadeh, A. Leon-Garcia, and P. Chow. *Expanding Open-Flow Capabilities with Virtualized Reconfigurable Hardware*. In International Symposium on Field-Programmable Gate Arrays (FPGA). ACM, February 2015.

M. Sadoghi, R. Javed, **N. Tarafdar**, H. Singh, R. Palaniappan, H.A Jacobsen. *Multi-query stream processing on FPGAs*. In International Conference on Data Engineering (ICDE). IEEE, 2012.

JOURNAL
PUBLICATIONS

N. Tarafdar, N. Eskandari, V. Sharma, C. Lo, and P. Chow. *Galapagos: A Full Stack Approach to FPGA Integration in the Cloud*. In IEEE Micro Special Issue: Hardware Acceleration, 2018. TO APPEAR

N. Tarafdar, N. Eskandari, T. Lin, and P. Chow. *Designing for FPGAs in the Cloud*. In IEEE Design & Test, 35(1):23-29, February 2018.

BOOK CHAPTERS

N. Tarafdar, T. Lin, D. Ly-Ma, D. Rozkho, A. Leon-Garcia, and P. Chow. *Building the Infrastructure for Deploying FPGAs in the Cloud*. In Hardware Accelerators in Data Centers, chapter 2, pages 9-33, Springer, 2018.

WORKSHOP
PUBLICATIONS

E. Fukuda, **N. Tarafdar**, I.C Chen, and P. Chow. *Distributed Stream Processing Platform for CPU-FPGA Heterogeneous Data Centers*. In Summer United Workshops on Parallel, Distributed and Cooperative Processing (SWoPP), page 5 pages, July 2017.

E. Fukuda, **N. Tarafdar**, and P. Chow. *Accelerating Apache Drill with FPGA*. Apache: Big Data North America, May 2016.

POSTER
PRESENTATIONS

N. Tarafdar, N. Eskandari, and P. Chow. *Galapagos: A Full Stack Approach to FPGA Integration in the Cloud*. In Xilinx Developer's Forum (XDF), San Jose, October 2018.

N. Tarafdar, T. Lin, H. Bannazadeh, A. Leon-Garcia, and P. Chow. *Heterogeneous Virtualized Network Function Chaining in the Data Center*. In IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM'17) Demo Night, May 2017.

N. Tarafdar, E. Fukuda, J. Chen, and P. Chow. *Heterogeneous Virtualized Network Function Chaining in the Data Center*. In IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM'17) Demo Night, May 2017.

E. Fukuda, **N. Tarafdar**, and P. Chow. *Organizing FPGAs in the Cloud for Distributed Applications*. 2016 SAVI AGM poster presentation, July 2016.

N. Tarafdar, R. Pavone, K. Yuan, E. Fukuda, T. Lin, H. Bannazadeh, A. Leon-Garcia, and P. Chow. *OpenCLoud: A Virtualized Heterogeneous Platform*. The CMC Microsystems 2015 Annual Symposium TEXPO Demonstration, September 2015.

Stuart Byma, **N. Tarafdar**, T. Xu, H. Bannazadeh, A. Leon-Garcia, and P. Chow. *Expanding Open-Flow Capabilities with Virtualized Reconfigurable Hardware*. 2015 SAVI AGM poster presentation, July 2015

E. Fukuda, **N. Tarafdar**, and P. Chow. *Interactive Large-scale Data Analysis on Virtual FPGAs in the Cloud*. 2015 SAVI AGM poster presentation, July 2015.

PROJECTS

Galapagos

Custom License

A full hardware stack for creating and deploying multi-FPGA and CPU applications. The stack allows users with different levels of proficiency target multi-FPGA and CPU applications at scale quickly. The stack also is flexible and can be adapted to target different network architectures and protocols.

Available: <https://github.com/tarafdar/galapagos>

HUMBoldt

Custom License

A communication layer between multi-CPU and FPGAs implemented using a subset of MPI. MPI cores built in hardware as Vivado HLS libraries are used to communicate using the network stack provided by the Galapagos project. This allows users to communicate amongst kernels implemented in CPUs and FPGAs by standardizing a protocol.

Available: <https://github.com/eskandarinariman/HMPI>

CLMonte

MIT License

OpenCL implementation of photon simulation using Monte Carlo method. This is used for applications like photodynamic cancer therapy. We implemented this on GPUs, CPUs and FPGAs for acceleration to get a high quality result quickly.

Available: <https://github.com/tarafdar/CLMonte>

TEACHING EXPERIENCE

Computer Programming

Teaching Assistant

ECE297

Second Year Undergraduate Course

Digital Systems Design

Teaching Assistant

ECE532

Fourth Year Undergraduate and Graduate Course

Digital Logic and Computer Hardware

Teaching Assistant

ECE241, ECE253, CSC258

Second Year Undergraduate Courses

Digital Design for System-on-Chip

Teaching Assistant

ECE1373

Graduate Course