

## Mario J. Badr

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CONTACT INFORMATION	The Edward S. Rogers Department of Electrical and Computer Engineering Room 1107, Sandford Fleming Bldg. 10 King's College Road, Toronto, ON M5S 3G4 Canada University of Toronto	
RESEARCH INTERESTS	Many/multi-core architectures, cache coherence, interconnection networks, application modelling, design space exploration.	
INDUSTRY EXPERIENCE	<b>Qualcomm Research Silicon Valley</b> <i>Intern (C++, OpenCL, Hexagon, CMake)</i> Used the Multicore Asynchronous Runtime Environment (MARE) to develop a heterogeneous application with multiple domain-specific kernels. Provided feedback to the MARE team on performance issues and bottlenecks.	Santa Clara, California, USA <i>May, 2015 - August, 2015</i>
	<b>Environment Canada</b> <i>Intern (Java, XML)</i> Implemented new features and bug fixes for the NinJo workstation, a tool for meteorologists. Notable projects include upgrading the visualization framework for lightning strikes to be faster and use significantly less memory, incorporating storm cell data for Canada, and helping to create a configurable view of weather data for a given storm cell.	Toronto, Ontario, Canada <i>June, 2009 - August, 2010</i>
AWARDS	<b>ECE Department TA Award</b> Awarded by student vote for the best three teaching assistants in the Electrical and Computer Engineering department for the Fall semester.	<i>2016</i>
	<b>Roberto Padovani Intern Scholarship - \$5,000</b> Awarded to seven Qualcomm Research interns across the globe for outstanding technical contributions made during their internship.	<i>2015</i>
	<b>Thomas Noakes &amp; Queen Elizabeth II Graduate Scholarship - \$15,000</b> Awarded for excellence in science and technology.	<i>2015</i>
	<b>TA Teaching Excellence Award - \$200</b> Awarded to four recipients across the three University of Toronto campuses based on nominations, references, and teaching philosophy.	<i>2015</i>
PEER-REVIEWED PUBLICATIONS	Joshua San Miguel, <b>Mario Badr</b> , and Natalie Enright Jerger. <i>Load Value Approximation</i> . In Proceedings of the International Symposium on Microarchitecture (MICRO), December 2014. (acceptance rate: 19%)	
	<b>Mario Badr</b> and Natalie Enright Jerger. <i>SynFull: Synthetic Traffic Models Capturing a Full Range of Cache Coherence Behaviour</i> . In Proceedings of the International Symposium on Computer Architecture (ISCA), June 2014. (acceptance rate: 18%)	
REFEREED WORKSHOPS & POSTERS	<b>Workshop Paper</b> Ajaykumar Kannan, <b>Mario Badr</b> , Parisa Khadem Hamedani and Natalie Enright Jerger. <i>Of-flooding to the GPU: An Objective Approach</i> . In Proceedings of the International Workshop on Parallelism in Mobile Platforms (PRISM), June 2015.	
	<b>Poster</b> Joshua San Miguel, <b>Mario Badr</b> , and Natalie Enright Jerger. <i>Load Value Approximation</i> . At the International Symposium on Microarchitecture (MICRO), December 2014.	

PRESENTATIONS	<b>Mario Badr</b> and Natalie Enright Jerger. <i>SynFull: Traffic Models Capturing Cache Coherence Behaviour</i> . At the International Symposium on Computer Architecture (ISCA), June 2014.
	<b>Mario Badr</b> and Natalie Enright Jerger. <i>SynFull: Synthetic Traffic Models That Capture Cache Coherent Behaviour</i> . At the University of Toronto ECE Graduate Symposium (Connections), May 2014. Awarded <i>Best Oral Presentation</i> .
	<b>Mario Badr</b> and Natalie Enright Jerger. <i>Realistic Synthetic Traffic</i> At the University of Toronto ECE Graduate Symposium (Connections), May 2012.
SOFTWARE ARTIFACTS	<b>SynFull</b> <span style="float: right;"><i>MIT License</i></span> Implementation of a statistical simulation methodology for design-space exploration of Networks-on-Chip. The artifact includes R scripts for generating models based on network traces. In addition, a C++ executable can load the models to generate synthetic traffic.
TEACHING EXPERIENCE	<b>Engineering Strategies and Practice</b> <span style="float: right;">1st Year Undergraduates, T-Program</span> <i>Teaching Assistant</i> <span style="float: right;"><i>Tutorials</i></span> Supervised students through the design process for a given project and provided feedback on written design documents, with a focus on stimulating an engineering methodology to design.
	<b>Computer Fundamentals</b> <span style="float: right;">1st Year Undergraduates, T-Program</span> <i>Teaching Assistant</i> <span style="float: right;"><i>Tutorials, Computer Lab</i></span> Taught the fundamentals of computer programming in C, including data structures, recursion, and sorting algorithms. Also delivered the 2013 Exam Jam review session, covering multiple prior exam questions in detail.
	<b>Programming Fundamentals</b> <span style="float: right;">2nd Year Undergraduates</span> <i>Teaching Assistant, Substitute Lecturer</i> <span style="float: right;"><i>Tutorials</i></span> Taught the fundamentals of C++ and object-oriented programming, including value versus reference semantics and memory management on the stack and heap. Delivered two lectures on recursion using an in-depth maze example with a step-by-step visualization of the maze traversal.
	<b>Communication and Design</b> <span style="float: right;">2nd Year Undergraduates</span> <i>Teaching Assistant, Course Development</i> <span style="float: right;"><i>Tutorials, Computer Lab</i></span> Mentored student groups in the implementation of an application that visualizes and finds routes in a city map. Developed six new tutorials in 2017 to help students with software engineering. Developed a new graphics library to simplify visualization for students, allowing them to focus on higher-level features.
	<b>Computer Organization</b> <span style="float: right;">3rd Year Undergraduates</span> <i>Teaching Assistant</i> <span style="float: right;"><i>Computer Lab</i></span> Supervised and helped students implement a simple von Neumann processor using verilog.
	<b>Computer Architecture</b> <span style="float: right;">4th Year Undergraduates &amp; Graduates</span> <i>Teaching Assistant</i> <span style="float: right;"><i>Computer Lab</i></span> Taught computer architecture concepts, including caches, pipelining, out-of-order cores, and cache coherence.
UNIVERSITY SERVICE	<b>Appointed Graduate Representative</b> <span style="float: right;">2015-2016</span> Executive Committee of Faculty Council - Faculty of Applied Science & Engineering
	<b>Graduate Representative</b> <span style="float: right;">2015-2016</span> Faculty Council - Faculty of Applied Science & Engineering
	<b>President</b> <span style="float: right;">2015-2016</span> Electrical and Computer Engineering Graduate Students' Society

PROFESSIONAL DEVELOPMENT	<b>Bargaining Support Committee Member</b> Canadian Union of Public Employees	January - April 2014
	<b>Department Steward</b> Canadian Union of Public Employees	2013-2014
	<b>Social Event Coordinator</b> Electrical and Computer Engineering Graduate Students' Society	2012-2013
	<b>Teaching in Higher Education</b> One semester course Learned more about teaching theories and styles and was observed by peers while teaching a tutorial on Computer Architecture. Also developed a course syllabus for a fictitious course.	2015
	<b>Prospective Professors in Training</b> <i>Thirteen Seminars, One semester course</i> Began preparations for becoming a professor in academia, attending several seminars and preparing a preliminary teaching dossier and research statement. Also completed a course on Teaching Engineering in Higher Education.	2014-2015
	<b>Mini-MBA</b> <i>Ten Classes</i> Gained an understanding of fundamental business concepts and applied what I learned in a group-based case competition.	2015
	<b>Oral Presentation Skills</b> <i>Five Classes</i> Examined presentation structure and the use of visual aids. Exchanged feedback with peers and the instructor on individual oral presentations.	2014
	<b>Prewriting Strategies for Developing and Organizing Your Ideas</b> <i>Four Classes</i> Learned several new strategies for developing and organizing ideas before (and during) the writing process.	2014
	<b>NSERC Proposal Workshop</b> <i>Three Classes</i> Examined features of good and bad proposal writing, and exchanged feedback with peers on our own NSERC proposals.	2014
	<b>Teaching Fundamentals Certificate</b> <i>Six Workshops</i> Improved my teaching skills with workshops on pedagogy, research, academic integrity, and students in difficulty.	2012-2013
EDUCATION	<b>Ph.D., Computer Engineering</b> <i>University of Toronto</i> Dissertation: "Novel Evaluation Methodologies for Future Architectures" Advisor: Natalie Enright Jerger	September, 2013 - Present <i>Toronto, Ontario, Canada</i>
	<b>M.A.Sc, Computer Engineering</b> <i>University of Toronto</i> Thesis: "Synthetic Traffic Models that Capture Cache Coherence Behaviour" Advisor: Natalie Enright Jerger	January 2014 <i>Toronto, Ontario, Canada</i>
	<b>B.A.Sc, Electrical Engineering</b> <i>University of Toronto</i>	May 2011 <i>Toronto, Ontario, Canada</i>