Naif Tarafdar

CONTACT INFORMATION

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EDUCATION

Ph.D. in Computer Engineering September, 2016 - Present
University of Toronto *Toronto, Ontario, Canada*
Dissertation: "Developing a Hardware Stack for Heterogeneous Data Centers"
Advisor: Paul Chow

M.A.Sc in Computer Engineering September, 2014 - September, 2016
University of Toronto *Toronto, Ontario, Canada*
Thesis: "Enabling Flexible Network FPGA Clusters in a Heterogeneous Data Center"
Advisor: Paul Chow

B.A.Sc with Honours in Computer Engineering September, 2009 - May, 2013
University of Toronto *Toronto, Ontario, Canada*

INDUSTRY AND RESEACH EXPERIENCE

Tenstorrent Toronto, Ontario, Canada
Team Lead and Senior Staff Software Engineer *June 2023 to Present*
(C++, C, Python)
I work on the Open Source TT-Metallium Stack at all levels. At the runtime level I created direct sharded reads and writes allowing users to write a tensor onto the distributed plane of L1 memory across many cores. I also lead the team responsible for data movement operations (e.g Slice, Sharding, Pad, etc.).

Groq Toronto, Ontario, Canada
Compiler Engineer *December, 2021 - June 2023*
(C++, C, LLVM, MLIR, Python)
I worked on implementing a tensor level partitioning analysis. With the tensor level partitioning our support for large graphs has increased to support networks such as Llama.

Xilinx Research San Jose, California, USA
Machine Learning Intern *August, 2017 - December, 2017*
(Verilog, C++, C, Vivado HLS, Python, TensorFlow, Caffe)
I designed, synthesized, and emulated, machine learning cores for high throughput, low-latency applications. I also worked on integrating these cores into popular software frameworks to make these cores accessible to software developers.

IBM Canada Toronto, Ontario, Canada
Hardware Acceleration Lab Intern *May, 2012 - September, 2013*
(Verilog, C++, OpenCL)
I optimized large-scale software projects CPU optimizations with the use of hardware accelerators and low-level software optimizations.

CONFERENCE PUBLICATIONS

N. Eskandari, **N. Tarafdar**, D. Ly-Ma, P. Chow. *A Modular Heterogeneous Stack for Deploying FPGAs and CPUs in the Data Center* In International Symposium on Field-Programmable Gate Arrays (FPGA). ACM, February 2019.

N. Tarafdar, T. Lin, N. Eskandari, D. Lion, A. Leon-Garcia, and P. Chow. *Heterogeneous Virtualized Network Function Framework in the Data Center.* In 27th International Conference on Field Programmable Logic and Applications (FPL 2017), September 2017.

T. Lin, **N. Tarafdar**, B. Park, P. Chow, and A. Leon-Garcia. *Enabling Network Function Virtualization over Heterogeneous Resources.* In The 19th Asia-Pacific Network Operations and Management Symposium (APNOMS2017), Seoul, South Korea, September 2017.

N. Tarafdar, T. Lin, E. Fukuda, H. Bannazadeh, A. Leon-Garcia, and P. Chow. *Enabling Flexible Network FPGA Clusters in a Heterogeneous Cloud Data Center.* In International Symposium on Field-Programmable Gate Arrays (FPGA). ACM, February 2017.

S. Byma, **N. Tarafdar**, T. Xu, H. Bannazadeh, A. Leon-Garcia, and P. Chow. *Expanding OpenFlow Capabilities with Virtualized Reconfigurable Hardware.* In International Symposium on Field-Programmable Gate Arrays (FPGA). ACM, February 2015.

M. Sadoghi, R. Javed, **N. Tarafdar**, H. Singh, R. Palaniappan, H.A Jacobsen. *Multi-query stream processing on FPGAs.* In International Conference on Data Engineering (ICDE). IEEE, 2012.

Journal Publications

N. Tarafdar, N. Eskandari, V. Sharma, C. Lo, and P. Chow. *Galapagos: A Full Stack Approach to FPGA Integration in the Cloud.* In IEEE Micro Special Issue: Hardware Acceleration, 2018.

N. Tarafdar, N. Eskandari, T. Lin, and P. Chow. *Designing for FPGAs in the Cloud.* In IEEE Design & Test, 35(1):23-29, February 2018.

Book Chapters

N. Tarafdar, T. Lin, D. Ly-Ma, D. Rozkho, A. Leon-Garcia, and P. Chow. *Building the Infrastructure for Deploying FPGAs in the Cloud.* In Hardware Accelerators in Data Centers, chapter 2, pages 9-33, Springer, 2018.

Workshop Publications

E. Fukuda, **N. Tarafdar**, I.C Chen, and P. Chow. *Distributed Stream Processing Platform for CPU-FPGA Heterogeneous Data Centers.* In Summer United Workshops on Parallel, Distributed and Cooperative Processing (SWoPP), page 5 pages, July 2017.

E. Fukuda, **N. Tarafdar**, and P. Chow. *Accelerating Apache Drill with FPGA.* Apache: Big Data North America, May 2016.

Poster Presentations

N. Tarafdar, G. Di Guglielmo, P.C Harris, J.D Krupa, V. Loncar, D.S Rankin, N. Tran, Z. Wu, Q. Shen, P. Chow. *Aigean: An Open Framework for Machine Learning on Heterogeneous Clusters* In 2020 IEEE 28th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM.

N. Tarafdar, N. Eskandari, and P. Chow. *Galapagos: A Full Stack Approach to FPGA Integration in the Cloud.* In Xilinx Developer's Forum (XDF), San Jose, October 2018.

N. Tarafdar, T. Lin, H. Bannazadeh, A. Leon-Garcia, and P. Chow. *Heterogeneous Virtualized Network Function Chaining in the Data Center.* In IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM'17) Demo Night, May 2017.

N. Tarafdar, E. Fukuda, J. Chen, and P. Chow. *Heterogeneous Virtualized Network Function Chaining in the Data Center.* In IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM'17) Demo Night, May 2017.

E. Fukuda, **N. Tarafdar**, and P. Chow. *Organizing FPGAs in the Cloud for Distributed Applications.* 2016 SAVI AGM poster presentation, July 2016.

N. Tarafdar, R. Pavone, K. Yuan, E. Fukuda, T. Lin, H. Bannazadeh, A. Leon-Garcia, and P. Chow. *OpenCLoud: A Virtualized Heterogeneous Platform.* The CMC Microsystems 2015 Annual Symposium TEXPO Demonstration, September 2015.

Stuart Byma, **N. Tarafdar**, T. Xu, H. Bannazadeh, A. Leon-Garcia, and P. Chow. *Expanding OpenFlow Capabilities with Virtualized Reconfigurable Hardware.* 2015 SAVI AGM poster presentation, July 2015

E. Fukuda, **N. Tarafdar**, and P. Chow. *Interactive Large-scale Data Analysis on Virtual FPGAs in the Cloud.* 2015 SAVI AGM poster presentation, July 2015.

Projects

Galapagos *Custom License*
A full hardware stack for creating and deploying multi-FPGA and CPU applications. The stack allows users with different levels of proficiency target multi-FPGA and CPU applications at scale quickly. The stack also is flexible and can be adapted to target different network architectures and protocols.
Available: *https://github.com/tarafdar/galapagos*

HUMBoldt *Custom License*
A communication layer between multi-CPUs and FPGAs implemented using a subset of MPI. MPI cores built in hardware as Vivado HLS libraries are used to communicate using the network stack provided by the Galapagos project. This allows users to communicate amongst kernels implemented in CPUs and FPGAs by standardizing a protocol.
Available: *https://github.com/eskandarinariman/HMPI*

CLMonte *MIT License*
OpenCL implementation of photon simulation using Monte Carlo method. This is used for applications like photodynamic cancer therapy. We implemented this on GPUs, CPUs and FPGAs for acceleration to get a high quality result quickly.
Available: *https://github.com/tarafdar/CLMonte*