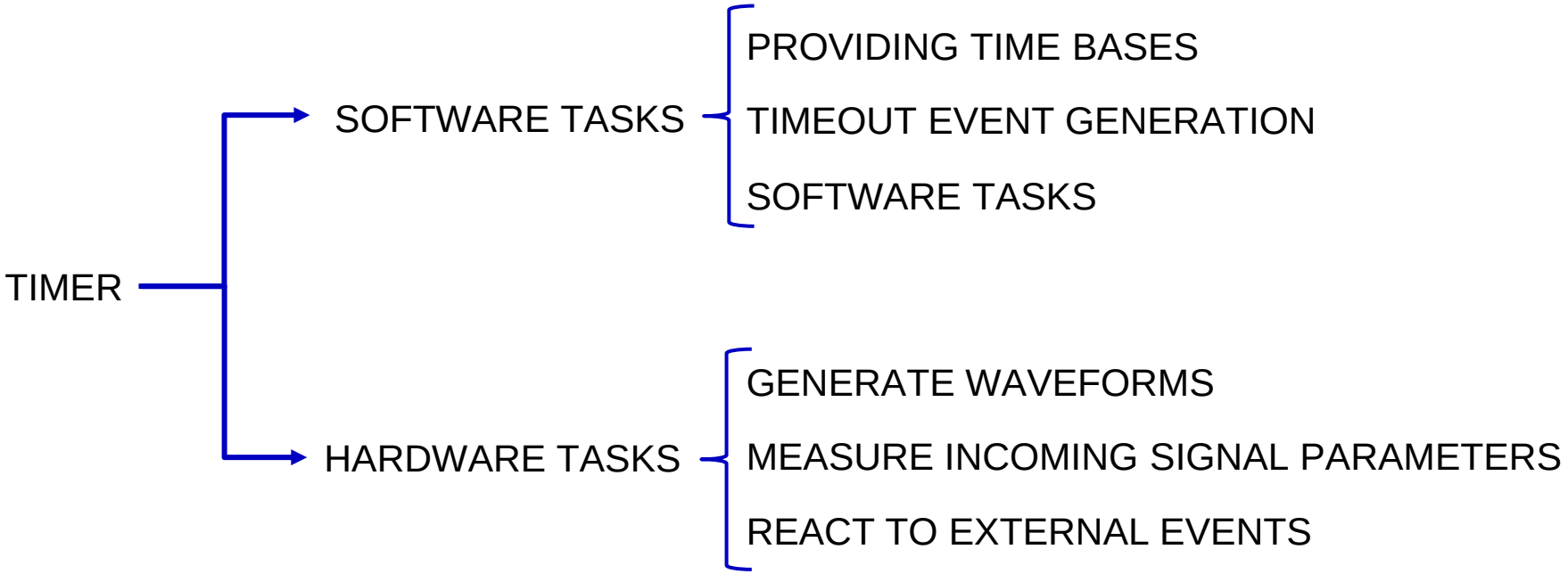
Iran University of
Science and Technology

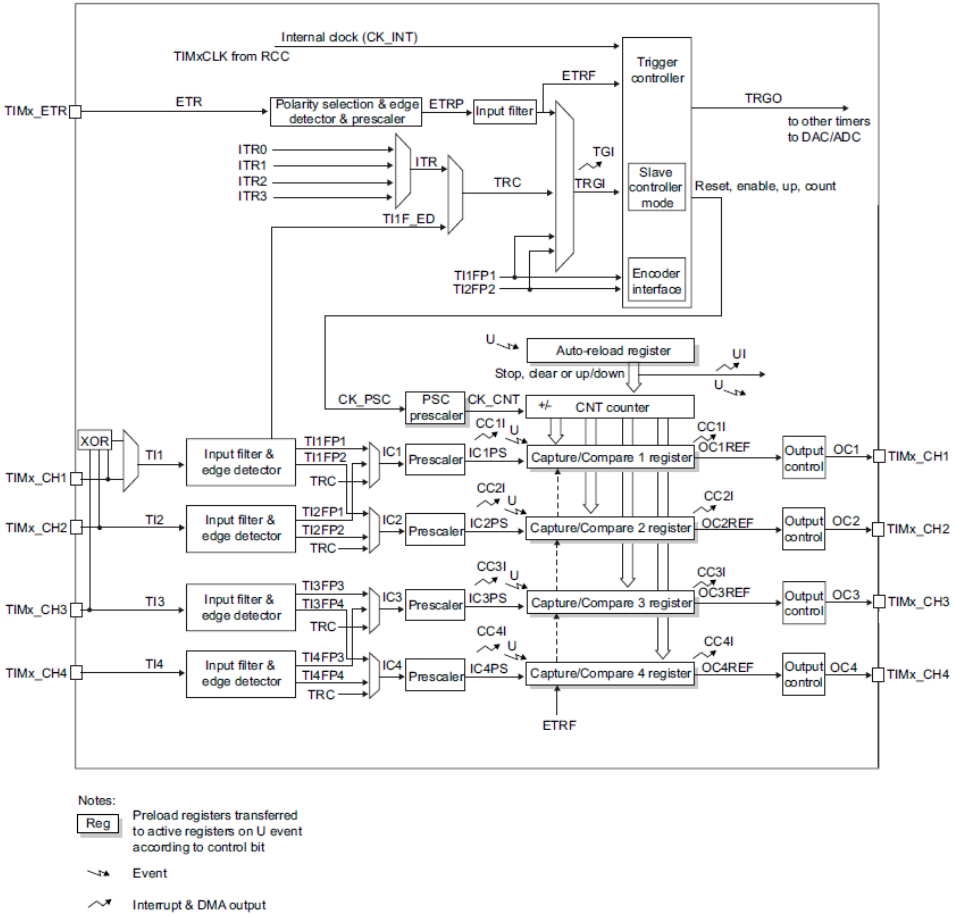
Microcontroller

Department of Electrical Engineering
Iran University of Science and Technology

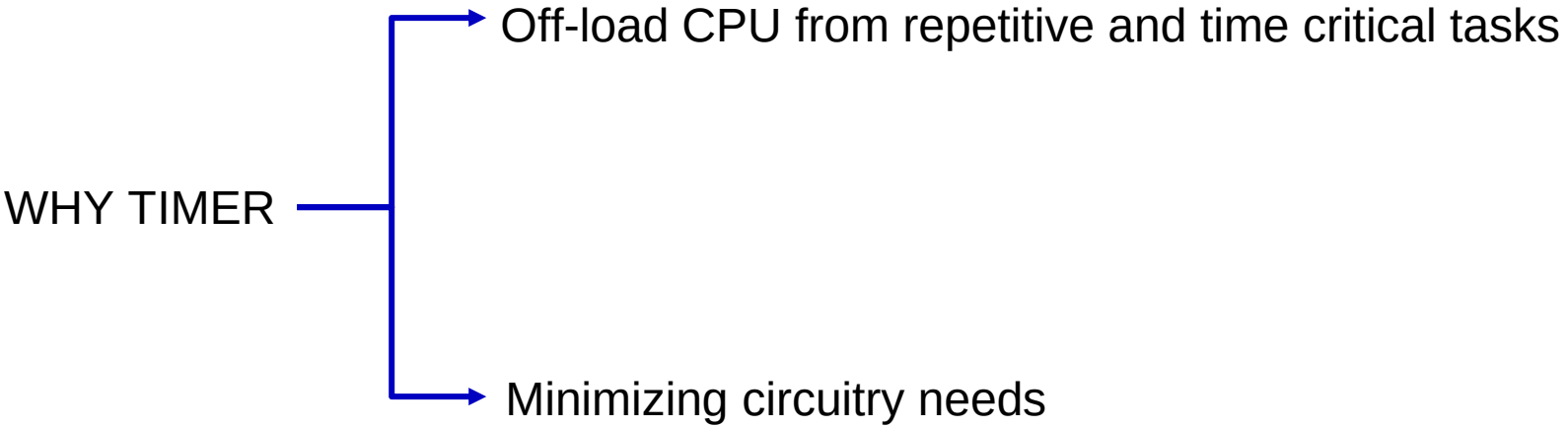
TIMER


TIMER
SOFTWARE TASKS
PROVIDING TIME BASES
TIMEOUT EVENT GENERATION
SOFTWARE TASKS
HARDWARE TASKS
GENERATE WAVEFORMS
MEASURE INCOMING SIGNAL PARAMETERS
REACT TO EXTERNAL EVENTS

TIMER


Internal clock (CK_INT)
TIMxCLK from RCC
TIMx_ETR
ETR
Polarity selection & edge detector & prescaler
ETRP
Input filter
ETRF
Trigger controller
TRGO
to other timers to DAC/ADC
ITR0
ITR1
ITR2
ITR3
ITR
TRC
TGI
TRGI
Slave controller mode
Reset, enable, up, count
TI1F_ED
TI1FP1
TI2FP2
Encoder interface
U
Auto-reload register
UI
Stop, clear or up/down
CK_PSC
PSC prescaler
CK_CNT
+/-
CNT counter
XOR
TI1
Input filter & edge detector
TI1FP1
TI1FP2
TRC
IC1
Prescaler
IC1PS
CC1I
Capture/Compare 1 register
CC1I
OC1REF
Output control
OC1
TIMx_CH1
TIMx_CH1
TI2
Input filter & edge detector
TI2FP1
TI2FP2
TRC
IC2
Prescaler
IC2PS
CC2I
Capture/Compare 2 register
CC2I
OC2REF
Output control
OC2
TIMx_CH2
TIMx_CH2
TIMx_CH3
TI3
Input filter & edge detector
TI3FP3
TI3FP4
TRC
IC3
Prescaler
IC3PS
CC3I
Capture/Compare 3 register
CC3I
OC3REF
Output control
OC3
TIMx_CH3
TIMx_CH4
TI4
Input filter & edge detector
TI4FP3
TI4FP4
TRC
IC4
Prescaler
IC4PS
CC4I
Capture/Compare 4 register
CC4I
OC4REF
Output control
OC4
TIMx_CH4
ETRF
Notes:
Reg
Preload registers transferred to active registers on U event according to control bit
Event
Interrupt & DMA output

TIMER



* All STM32 timers are based on the same scalable architecture.

TIMER

KEY FEATURES

- All timers are based on the same scalable architecture
  - Number of IO
  - 16 bit
  - Features
- Multiple timers can be linked and synchronized
- Each timer channel in configurable independently
- Multiple interconnect with other peripherals

TIMER

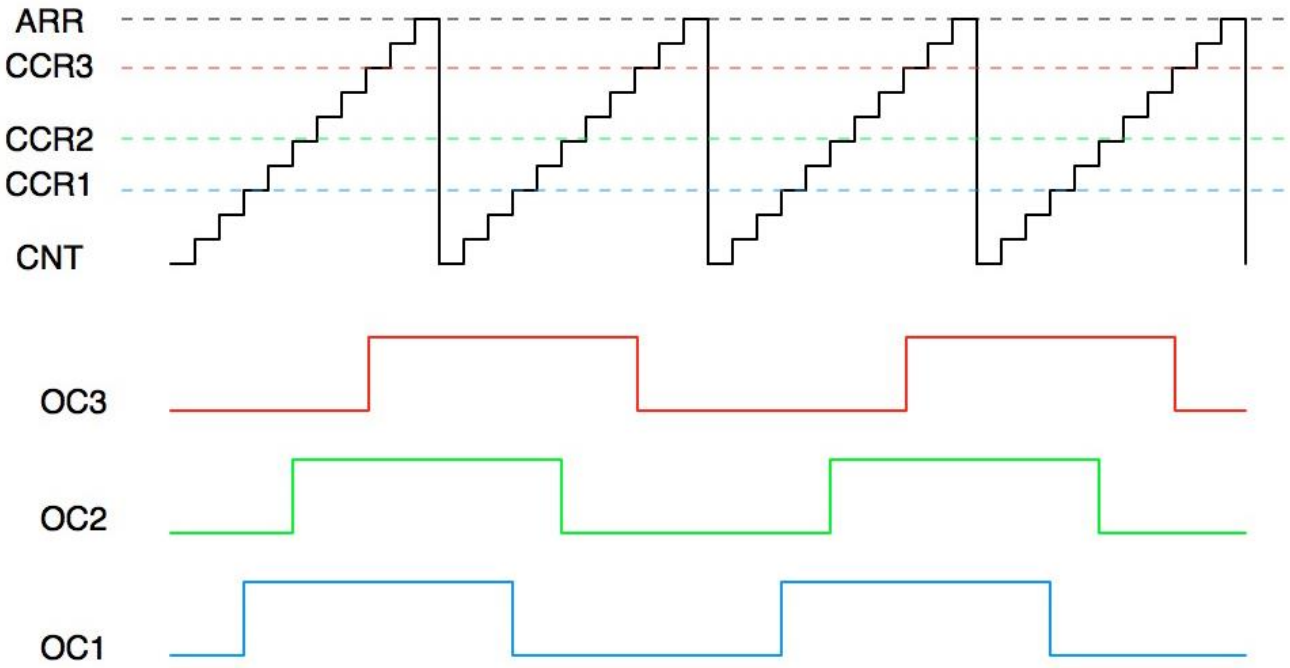
- TIMERS
  - General-purpose timers (TIM2 to TIM5)
    - Up to 4 independent channels for:
      - – Input capture
      - – Output compare
      - – PWM generation
      - – One-pulse mode output
  - General-purpose timers (TIM9 to TIM14)
  - Advanced-control timers (TIM1 and TIM8)
    - All above and Complementary outputs with programmable dead-time
  - Basic timers (TIM6 and TIM7)
    - generic timers for time-base generation

TIMER-OUTPUT COMPARE

- OUTPUT COMPARE
  - Output compare timing
  - Output compare active
  - Output compare inactive
  - Output compare toggle
    - OCxRef toggles when the counter (CNT) matches the capture/compare register (CCRx).
  - Output compare forced active/inactive

TIMER-OUTPUT COMPARE TOGGLE

Three-phase pulse train from the Output Compare Channels of a general purpose timer



TIMER-OUTPUT COMPARE

To configure the timer in one of these modes:

1. Select the clock source.
2. Write the desired data in the ARR and CCRx registers.
3. Configure the output mode:
   a) Select the output compare mode: timing / active / inactive / toggle.
   b) In case of active, inactive and toggle modes, select the polarity by writing CCxP in CCER register.
   c) Disable the preload feature for CCx by writing OCxPE in CCMRx register.
   d) Enable the capture / compare output by writing CCxE in CCER register.
4. Enable the counter by setting the CEN bit in the TIMx_CR1 register.
5. Set the CCxIE / CCxDE bit if an interrupt / DMA request is to be generated.

1.Select the clock source.

RCC_APB1ENR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		DAC EN	PWR EN	BKP EN	Res.	CAN EN	Res.	USB EN	I2C2 EN	I2C1 EN	UART5 EN	UART4 EN	USART3 EN	USART2 EN	Res.
		rw	rw	rw		rw		rw	rw	rw	rw	rw	rw	rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI3 EN	SPI2 EN	Reserved		WWD GEN	Reserved		TIM14 EN	TIM13 EN	TIM12 EN	TIM7 EN	TIM6 EN	TIM5 EN	TIM4 EN	TIM3 EN	TIM2 EN
rw	rw			rw			rw	rw	rw	rw	rw	rw	rw	rw	rw

1.Select the clock source.

TIMx_PSC

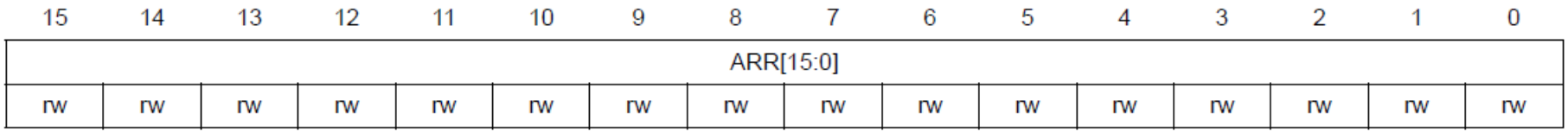
PSC[15:0]: Prescaler value
The counter clock frequency (CK_CNT) is equal to fCK_PSC / (PSC[15:0] + 1).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSC[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

2. Write the desired data in the ARR and CCRx registers.

TIMx_ARR

ARR[15:0]: Auto-reload value



2. Write the desired data in the ARR and CCRx registers.

TIMx_CCR1

CCR1[15:0]: Capture/Compare 1 value

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCR1[15:0]															
rw/ro	rw/ro	rw/ro	rw/ro	rw/ro	rw/ro	rw/ro	rw/ro	rw/ro	rw/ro	rw/ro	rw/ro	rw/ro	rw/ro	rw/ro	rw/ro

3. Configure the output mode:

a) Select the output compare mode: toggle.

TIMx_CCMR1

OC1M: Output compare 1 mode
011: Toggle - OC1REF toggles when TIMx_CNT=TIMx_CCR1.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OC2 CE	OC2M[2:0]			OC2 PE	OC2 FE	CC2S[1:0]		OC1 CE	OC1M[2:0]			OC1 PE	OC1 FE	CC1S[1:0]	
IC2F[3:0]				IC2PSC[1:0]					IC1F[3:0]			IC1PSC[1:0]			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

3. Configure the output mode:

b) select the polarity by writing CCxP in CCER register.

TIMx_CCER

CC1P: Capture/Compare 1 output polarity
CC1 channel configured as output:
0: OC1 active high.
1: OC1 active low.

15 14	13	12	11 10	9	8	7 6	5	4	3 2	1	0
Reserved	CC4P	CC4E	Reserved	CC3P	CC3E	Reserved	CC2P	CC2E	Reserved	CC1P	CC1E
	rw	rw		rw	rw		rw	rw		rw	rw

3. Configure the output mode:

c) Disable the preload feature

TIMx_CCMR1

OC1PE: Output compare 1 preload enable
0: Preload register on TIMx_CCR1 disabled.
1: Preload register on TIMx_CCR1 enabled

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OC2 CE	OC2M[2:0]			OC2 PE	OC2 FE	CC2S[1:0]		OC1 CE	OC1M[2:0]			OC1 PE	OC1 FE	CC1S[1:0]	
IC2F[3:0]				IC2PSC[1:0]				IC1F[3:0]				IC1PSC[1:0]			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

3. Configure the output mode:

d) Enable the capture / compare output

TIMx_CCER

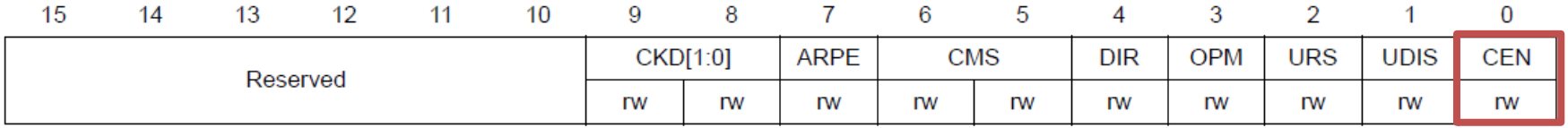
CC1E: Capture/Compare 1 output enable
CC1 channel configured as output:
0: Off - OC1 is not active.
1: On - OC1 signal is output on the corresponding output pin

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		CC4P	CC4E	Reserved		CC3P	CC3E	Reserved		CC2P	CC2E	Reserved		CC1P	CC1E
		rw	rw			rw	rw			rw	rw			rw	rw

4. Enable the counter

TIMx_CR1

CEN: Counter enable
0: Counter disabled
1: Counter enabled



15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						CKD[1:0]		ARPE	CMS		DIR	OPM	URS	UDIS	CEN
						rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

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