A Digital-Controller Parameter-Tuning Approach, Application to a Switch-Mode Power Supply

Xuefang Lin-Shi, Florent Morel, *Student Member, IEEE*, Bruno Allard, *Senior Member, IEEE*,
Dominique Tournier, Jean-Marie Rétif
AMPERE, CNRS UMR 5005, INSA-Lyon
Building L. De Vinci, 20 avenue A. Einstein, F-69621 Villeurbanne Cedex, France
Email: {xuefang.shi, florent.morel, bruno.allard, dominique.tournier, jean-marie.retif}@insa-lyon.fr
Shuibao Guo, Yanxia Gao
Institute of Electrical and Control Engineering, Shanghai University
149 Yanchang Road, 200072 Shanghai, China
Email: shuibao.guo@insa-lyon.fr, eegoanna@163.com

***Abstract*— Analogue control of monolithic DC/DC converters is technologically coming to a limit due to high switching frequency and a request for large regulation bandwidth. Digital control is now experimented for low-power low-voltage switch-mode power supply. Digital implementation of analogue solutions does not prove real performances. This paper compares a classical digital controller to a candidate alternative strategy. Sensitivity functions are used to compare controller performances. An off-line approach using fuzzy logic to quantify controller performances and a genetic algorithm to obtain an optimal controller is presented. A so-called RST algorithm optimized with this approach shows better performances.**

I. Introduction

For many years now, there is a trend to embed power management unit inside portable devices like cellphone, personal digital assistant or MP3-player. Most portable devices use a battery of voltage between 5.5V when in charge, 3.3V during discharge lifetime and down to 2.7V when empty. Devices embed various functions supplied from various voltages. Processors require 1.8V down to 1.2V while backlight led system require 20V at least. Non isolated DC/DC converters are considered in place of low-drop out regulators for the sake of efficiency. This paper will now address only step-down conversion and associated buck architecture or step-down switch-mode power supply (SMPS).

An example of full-analogue synchronous buck converter is pictured in Fig. 1. Except the passive L-C output filter, all blocks are integrated monolithically using CMOS standard technology [1], [2]. A 2-pole/2-zero compensator is implemented to achieve a maximal regulation bandwidth, maximal transient performance and maximal accuracy.

A 100MHz SMPS, 80% peak efficiency, 20MHz regulation bandwidth is presented in [3]. The design is compatible with standard CMOS process. Whatever the analogue control presents some limitations. First of all, the design of the compensator is not automated and the design engineer needs to take care of a trade-off between performances, accuracy and stability [4]. When R-C constant have been set, manufacturing introduces deviation with respect to design values and calibrations are required. The robustness is not sufficient, so a lot of efforts are put on alternative approaches as digital control.

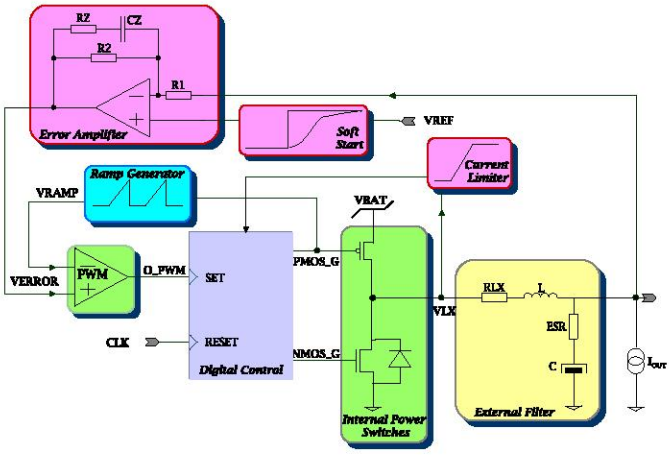

Fig. 1. Schematic synchronous step-down SMPS

Digital control is not new in the field of Power Electronics. It is often associated with DSP or other processor-like implementation [5]–[8]. Generally the digital control system presents sufficient resources to accommodate the modest switching frequency of the converter, in the kHz range. In embedded applications, switching frequencies in the MHz and plus range are necessary in order to reduce the size of passive components [9].

Due to the cost/complexity constrains existing in small-power dc-dc converters with integrated digital controller, most published papers consider a discrete-time scheme equivalent to the analogue compensator (such as PID controller) [10], [11].

In order to satisfy the constrains on the load variation to achieve high transient performance and accuracy, an auto-tuning process should be introduced. Some publications about auto-tuning of digital PID controller for DC/DC converters can be found in [12]–[14]. However, most of the solutions are on-line tuning, so they require an increase of the silicon area of the IC controller. The practical use in very high frequency

1-4244-0755-9/07/$20.00 ©2007 IEEE

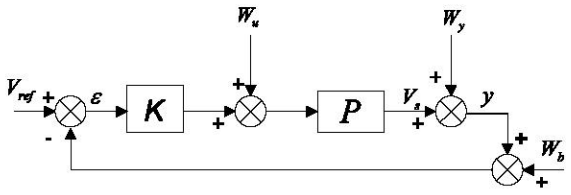

Fig. 2. Block diagram of the SMPS

(>500kHz) and very low power (<1W) is still questionable.

In this paper, an off-line tuning RST controller is presented. With similar complexity as a classical PID controller, a so-called RST controller presents more degrees of freedom for improving nominal and robust performances and rejection of disturbances [15]. Based on pole placement combined with the shaping of sensitivity functions, the paper investigates an off-line automated approach by using fuzzy logic and genetic algorithm to correctly specify the desired performances by adjusting the sensitivity functions in the frequency domain where it is necessary. As the automated parameter determination is performed off-line, there is no need supplementary silicon area for the auto-tuning scheme.

The paper is organized as follows: Section II reviews sensitivity functions and the application of the sensitivity function analysis on a buck converter. Section III introduces a digital PID controller for comparison purpose. The robust RST digital controller and the off-line automated tuning approach are described in Section IV. Simulation results are detailed in Section V.

II. Sensitivity Functions

In order to quantify system dynamics, robustness and noise rejection properties of tested controllers, sensitivity functions are introduced.

Fig. 2 represents the model of a SMPS (P) and its controller (K) when adding a control noise W_u (e.g. PWM noise), an output noise W_y (e.g. load variations) and a measurement noise W_b (e.g. A/D converter noise).

From Fig. 2, it comes the following relation that leads to the sensitivity functions.

$$y = \Gamma.V_{ref} + S_{yy}.W_y + S_{yb}.W_b + S_{yu}.W_u \quad (1)$$

$$\Gamma = \frac{KP}{1+KP} = \frac{L_{yy}}{1+L_{yy}} \quad (2)$$

$$S_{yy} = \frac{1}{1+KP} = \frac{1}{1+L_{yy}} \quad (3)$$

$$S_{yb} = \frac{-KP}{1+KP} = \frac{-L_{yy}}{1+L_{yy}} \quad (4)$$

$$S_{yu} = \frac{P}{1+KP} = \frac{P}{1+L_{yy}} \quad (5)$$

where Γ is the closed loop transfer function, S_{yy}, S_{yb} and S_{yu} are respectively the output-to-output, measure-to-output and control-to-output sensitivity functions.

Constraints or disturbance rejections are naturally expressed in terms of frequency sensitivity shapes. For a given controller, the sensitivity functions allow to evaluate the controller behavior in relation to the desired attenuation constraints.

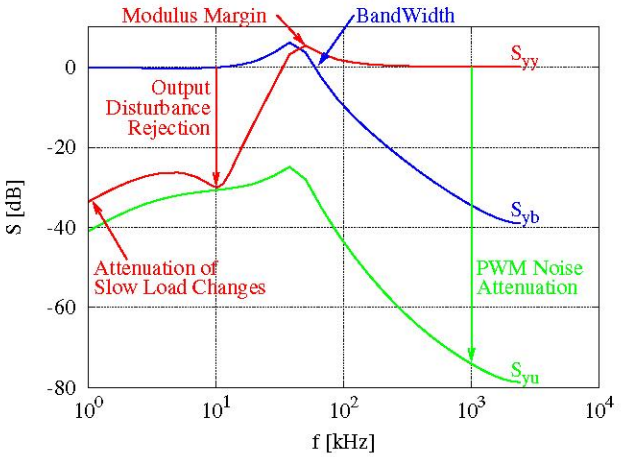

Fig. 3. Example of Sensitivity Functions

Fig. 3 is an example of the gain plot of sensitivity functions. PWM and output noise attenuations are pointed considering a 1MHz PWM frequency and a 1kHz output disturbance resonance. The gradient of S_{yy} at low frequency determines the dynamic behavior of the system. The bandwidth of S_{yb} defines the influence of measurement noise on the output voltage and the closed loop bandwidth since it has the same transfer function as Γ expect for the sign. The gain of S_{yu} verifies the rejection of control perturbations such as the PWM-related noises.

In addition, from the maximum value of S_{yy}, the modulus margin can be determined. Indeed, it can be shown that the maximum value of S_{yy} is proportional to the inverse of the modulus margin [16]. The modulus margin ΔM is defined as the minimum distance of L_{yy} with respect to the critical locus (-1) in the Nyquist plan. The modulus margin and delay margin quantify the robustness of the modeling uncertainties. The delay margin $\Delta\tau$ is deduced from the phase margin $\Delta\Phi$ by $\Delta\tau = \frac{\Delta\Phi}{\omega_\Phi}$, where ω_Φ is the pulsation of phase margin determination.

In order to ensure robustness, the modulus margin ΔM is kept higher than 0.5 and the delay margin must be higher than the sampling period (to ensure that the delay induced by controller computing time does not lead to unstable operation).

III. PID Control

The PID controller is presented for comparison purpose with the RST controller. A digitally controlled buck converter operating in continuous conduction mode (CCM) can be regarded as a second order discrete-time system [17]:

$$P(z) = \frac{b_1 z + b_2}{z^2 + a_1 z + a_2} \quad (6)$$

A discrete-time PID controller can be written as:

$$K_{PID}(z) = \frac{r_0 z^2 + r_1 z + r_2}{(z-1)(z+s_1)} \quad (7)$$

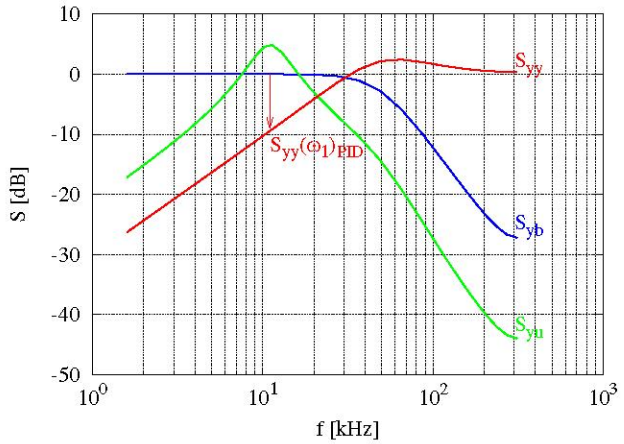

Fig. 4. Sensitivity functions for the PID controlled system

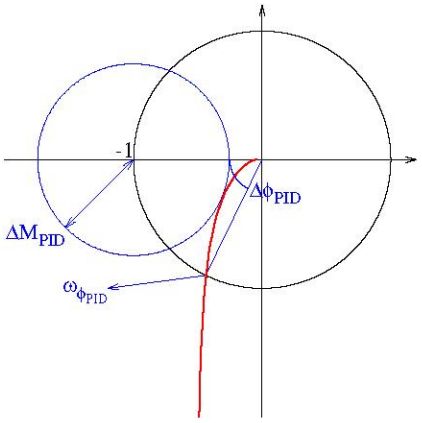

Fig. 5. Nyquist plot of L_{yy} for the PID controlled system

where r_0, r_1, r_2, s_1 are the controller parameters to be determined.

By cancelling the poles of $P(z)$ with the zeros of $K(z)$, the closed-loop reference for the output voltage transfer function is:

$$\begin{aligned}\Gamma &= \frac{KP}{1+KP} \\ &= \frac{r_0 b_1 z + r_0 b_2}{z^2 + (s_1 - 1 + r_0 b_1)z + (r_0 b_2 - s_1)} \\ &= \frac{r_0 b_1 z + r_0 b_2}{z^2 + p_1 z + p_2}\end{aligned} \tag{8}$$

where p_1 and p_2 are defined by the desired closed-loop dynamics which correspond to second order dynamics with a pulsation ω_{cl} and a damping ratio ξ_{cl}. The conditions for the cancellation of the poles of $P(z)$ by the zeros of $K(z)$ are:

$$\begin{aligned}r_0 &= \frac{1 + p_1 + p_2}{b_1 + b_2} \\ r_1 &= a_1 r_0 \\ r_2 &= a_2 r_0 \\ s_1 &= r_0 b_2 - p_2\end{aligned} \tag{9}$$

The circuit elements are L = 10μH, C = 22μF, R = 3Ω, V_{BAT} = 3V and the sampling frequency is set to f_e = 625kHz. The desired closed-loop pulsation must be smaller than the Nyquist frequency, so it is set to 311850rd/s corresponding to 4.5 times the open-loop pulsation. With the closed-loop damping ratio of 0.7, the controller parameters are $r_0 = 5.23$, $r_1 = -10.1$, $r_2 = 4.93$ and $s_1 = -0.471$. The corresponding sensitivity functions and Nyquist plot of L_{yy} are presented respectively in Fig. 4 and Fig. 5. For an output disturbance with a pulsation of ω_1 (LC filter resonance), the gain of S_{yy} on ω_1 gives the information on the disturbance rejection. In the studied case, $\omega_1 = 11$kHz. It can be seen that $S_{yy}(\omega_1)$ is about -8dB. Concerning the stability robustness, the modulus, phase and delay margins are $\Delta M_{PID} = 0.75$, $\Delta\Phi_{PID} = 64°$, $\Delta\tau_{PID} = 3.63T_e$. Due to the sampling effect,

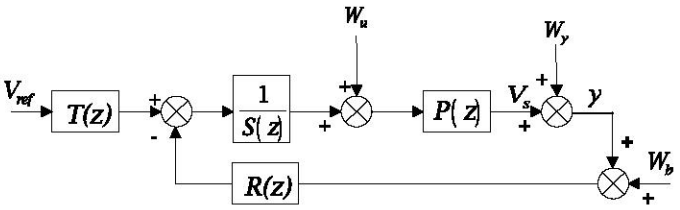

Fig. 6. RST control structure

sensitivity functions are plotted until the Nyquist frequency. As the PWM frequency is set equal to the sampling frequency f_e, the PWM noise rejection can not be appreciated. The overall tuning of the PID controller is quite classical.

IV. Robust RST Control

RST control realizes a relevant approach for linear Single Input Single Output (SISO) systems [15]. A RST controller is considered here in order to obtain a better output disturbance rejection while keeping a good PWM noise rejection and a good robustness. The structure of a RST control is presented in Fig. 6.

If the discrete time SMPS model is described by the transfer function $P(z) = \frac{B(z)}{A(z)}$, where $B(z)$ and $A(z)$ are polynomials, the sensitivity functions can be expressed as:

$$S_{yy} = \frac{AS}{AS + BR} \tag{10}$$

$$S_{yb} = \frac{-BR}{AS + BR} \tag{11}$$

$$S_{yu} = \frac{BS}{AS + BR} \tag{12}$$

From these expressions, it can be noted that the three sensitivity functions have the same denominator $D = AS + BR$ which determines the closed-loop poles. It can be noted that sensitivity functions are independent of $T(z)$.

The knowledge of acceptable disturbances leads to design the RST controller in terms of pole and zero assignments. Some fixed parts can be specified for the polynomials $S(z)$

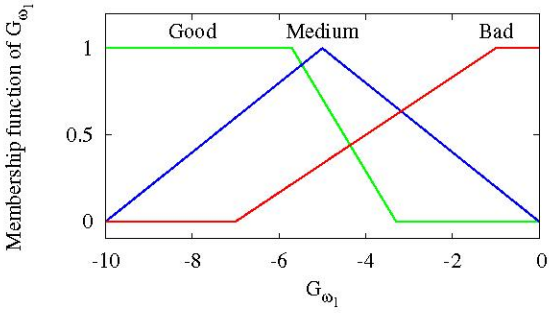

Fig. 7. Input membership function for G_{ω_1}

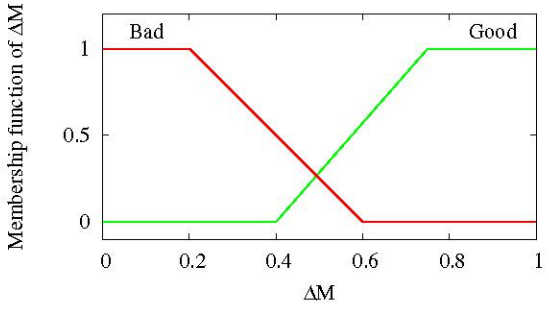

Fig. 8. Input membership function for ΔM

and $R(z)$. For example, to insure the output accuracy, a pole for z=1 in S(z) is necessary for static error elimination. The closed-loop poles are chosen either for filtering effects in certain frequency regions or for improving the robustness of the closed-loop system. For an output disturbance at pulsation ω_1, the lower the gain of S_{yy} the better the attenuation of the output disturbance rejection. However it can be shown that the larger the attenuation of S_{yy} at ω_1, the larger the area of S_{yy} over the zero value [15]. It can induce a increase in the maximum value of S_{yy}. As the maximum value of S_{yy} is inversely proportional to ΔM, a larger output noise rejection leads to a worse robustness.

How to determine a controller which offers a trade-off between the robustness and a good rejection of disturbances? This can be described as an optimization problem by defining a cost function which qualifies the controller robustness and noise rejection properties.

Fuzzy logic is suitable to qualify the robustness of a controller and noise rejection properties [18]. Indeed the frontier between a good controller and a bad controller is not strict. For example, if one considers the modulus margin is correct if it is higher than 0.5, it is clear that a controller will not be qualified with a bad robustness getting to good by crossing this value. With membership functions of fuzzy logic, the controller quality can be evaluated continually from bad to good across medium.

An example of membership functions qualifying the gain at ω_1 (G_{ω_1}) and the modulus margin (ΔM) is shown in Fig. 7 and Fig. 8. G_{ω_1} is normalized over {-10 0} and ΔM uses its natural scale. The output membership function is given

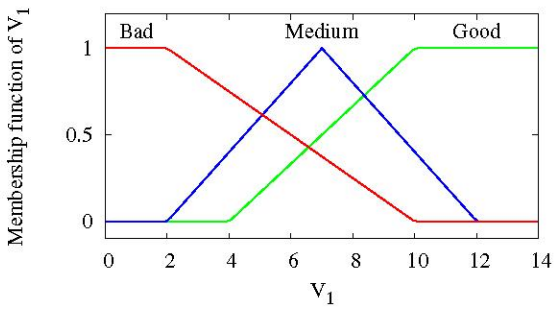

Fig. 9. Output membership functions

TABLE I
FUZZY RULES USED

G_{ω_1} / ΔM	**Bad**	**Medium**	**Good**
Bad	Bad	Bad	Medium
Good	Bad	Medium	Good

in Fig. 9. The stability robustness can be expressed by fuzzy rules defined in Tab. I. After "disfuzzyfication", the robustness analysis is quantified by the function V_1 = f(G_{ω_1},ΔM) which corresponds to a surface as presented in Fig. 10. It can be seen that for ΔM > 0.5, the lower the values of G_{ω_1} the better the output function V_1.

In the same way, other membership functions and fuzzy rules in relation with delay margin and other sensitivity functions can be defined to quantify constraints of robustness and satisfy the requirements of disturbance rejection performances. A weighted sum of all fuzzy functions defines the quality function to maximize.

The optimization problem is addressed by a genetic algo-

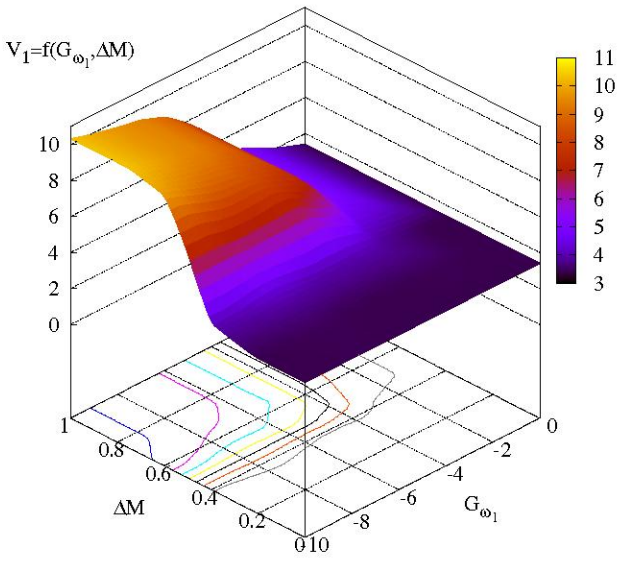

Fig. 10. Fuzzy function V_1

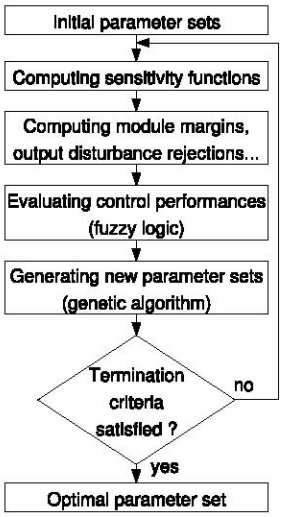

Fig. 11. Off line approach used to determine controller parameters

rithm which is a stochastic tool based on the mechanism of natural selection. Each variables X_i (*chromosomes*) are coded on n_i bits between a minimum value min_i and a maximum one max_i. An initial population of strings (*individual*) is arbitrarily created. Genetic algorithm makes it change by using three main operations: reproduction, crossover and mutation in order to maximise an objective function (*fitness value*) [19]. The performed computation time can be important but it is off-line, so that is not a limitation for real-time implementation.

The offline approach used to determine controller parameters is summarized in Fig. 11. This optimization problem is solved in the Matlab/Similink environment.

For SMPS application, the denominator of the sensitivity function S_{yy} is chosen as follows to determine a RST controller which presents a good robustness and a good attenuation of the influence of the output disturbance at $\omega_1 = 11$kHz.

$$D(z) = (1 - c_0 z^{-1})(1 + c_1 z^{-1} + c_2 z^{-2}) \qquad (13)$$

where c_0 is between 0.1 to 0.99, $(1 + c_1 z^{-1} + c_2 z^{-2})$ corresponds to a pair of complex zeros for which the frequency band and the damping ratio are between $\omega_0 = 1 \cdot 10^5$rad/s to $3 \cdot 10^5$rad/s and ξ_0 = 0.3 to 1 c_0, ω_0 and ξ_0 constitute three degrees of freedom (or *chromosomes*) for the optimization problem. For each combination of c_0, ω_0 and ξ_0 (i.e. each *individual* for the genetic algorithm), the fuzzy logic quantifiers the quality function (or *fitness value*). The genetic algorithm then finds the optimal solution for c_0, ω_0 and ξ_0 over twenty generations with about thirty individuals for $n_i = 16$, crossover probability = 0.9 and mutation probability =0.02.

The individuals which have been tested by the genetic algorithm are plotted in Fig. 12. The corresponding optimal polynomial $R(z)$, $S(z)$ and $T(z)$ are calculated by solving the Bezout equation [15].

$$\begin{aligned} R(z) = &\quad 16.03\, z^2 - 28.21\, z + 12.82 \\ S(z) = &\quad z^2 - 0.82\, z - 0.18 \end{aligned} \qquad (14)$$

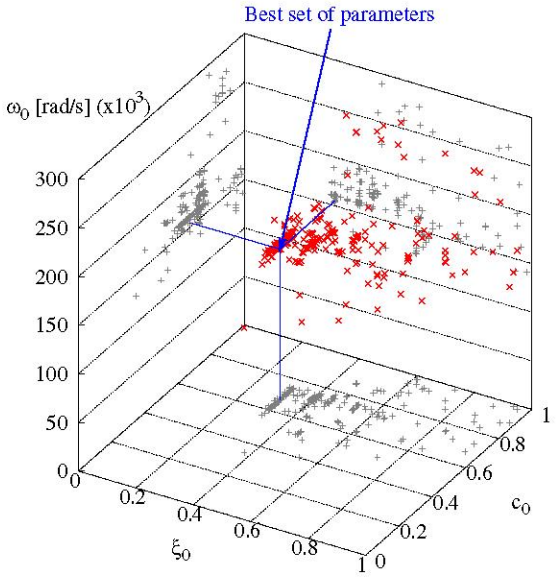

Fig. 12. Individuals which have been tested by the genetic algorithm

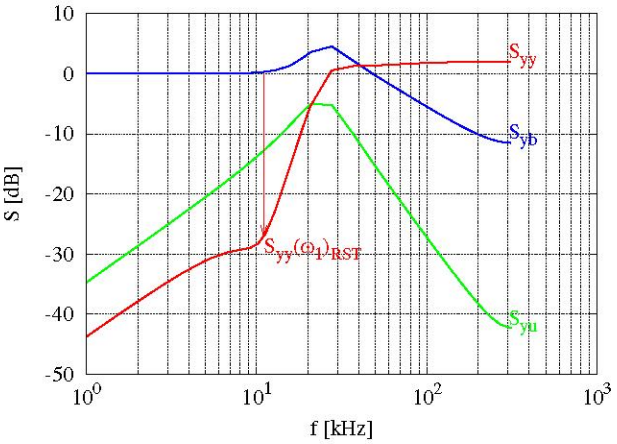

Fig. 13. Sensitivity functions for RST controller

$$T(z) = 35.11\, z^3 - 86.84\, z^2 + 72.62\, z - 20.24$$

Since, the obtained controller is described by (14), the hardware implementation is quite simple: it just need a few memories, multipliers and adders.

The corresponding sensitivity functions and Nyquist plot of L_{yy} are respectively given in Fig. 13 and 14.

The gain of S_{yy} at ω_1 (LC filter resonance) is -27dB against -8dB for the PID controller. The good robustness is keep with $\Delta M_{RST} = 0.79$, $\Delta\Phi_{RST} = 51°$ and $\Delta\tau_{RST} = 2.16 T_e$.

V. Simulation Results

The simulations are performed using Simulink (Fig. 15). The buck SMPS is modeled by a hybrid model [4]. The PID controller and RST controller are computed with fixed-point algorithm. The analog-to-digital converter model has a 10-bit resolution and takes into account quantization, delay and saturation effects. The DPWM model has a 8-bit resolution.

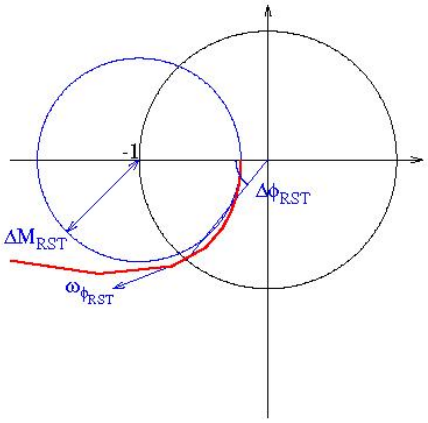

Fig. 14. Nyquist plot of L_{yy} for RST controlled system

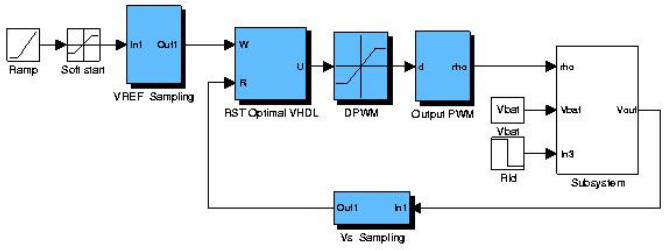

Fig. 15. Simulink model of the RST digital controller for the buck converter

The output voltages are compared during a step change of load from 10Ω to 3Ω in Fig. 16. The load transient response of RST controller is superior to PID controller since it results in shorter rise time and produces smaller undershoot.

VI. Conclusion

This paper details an off-line automated design of a RST digital controller. Robust RST controller offers better performances compared to a classical digital PID controller. As the design approach is based on robustness, neither parameters uncertainty (due to aging or manufacturing disparity) nor neglected physical phenomena will lead to an unstable system. An real time auto tuning or parameter estimator is not necessary, so RST implementation can be simply achieved using one A-to-D converter and standard CMOS logic. Experimental study are currently performed using an Actel ProAsic3 FPGA board plus an additional analog I/O board. It will be possible to estimate the impact of fixed point computing and monolithic integration from experimental results as FPGA design can be translated at no cost into an ASIC. PID like RST controller requires a fast A-to-D converter. It will probably be the bigger energy consumer in the digital control. Energy consumption is one of the most important criteria when considering digital controllers instead of analog controllers in embedded devices. So this point will be considered in future works.

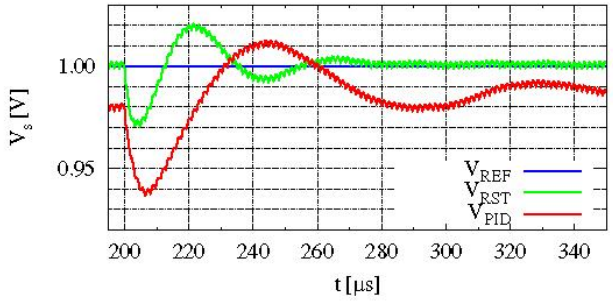

Fig. 16. Comparison of output voltage responses to load perturbation for the RST and PID controller

References

[1] V. Kursun, S. Narendra, V. K. De, and E. Friedman, "High input voltage step-down dc/dc converters for integration in a low voltage cmos process," *Proc. of IEEE ISCAS*, 2004.

[2] H. Deng, X. Duan, Y. Ma, A. Huang, and D. Chen, "Monolithically integrated boost converter based on 0.5um cmos process," *IEEE Transactions on Power electronics*, vol. 20, no. 3, pp. 628–638, 2005.

[3] V. Pinon, B. Allard, and C. Garnier, "High-frequency monolithic dc/dc converter for system-on-chip power management high-frequency monolithic dc/dc converter for system-on-chip power management," *Proceedings of IEEE ISPSD, Naples, June*, 2006.

[4] S. Trochut, B. Allard, X. Lin-Shi, and J. M. Rétif, "Control design for integrated switch-mode power supplies : a new challenge ?" *Proc. of the IEEE Power Electronics Specialist's Conference*, 2004, cdrom.

[5] T. Martin and S. Ang, "Digital control for switching converters," *Proc of IEEE ISIE*, vol. 2, pp. 480–484, 1995.

[6] H. Matsuo, Y. Mimura, Y. Nakao, F. Kurokawa, and M. Sasaki, "Novel digital controller for the pwm and/or pfm controlled dwitching dc/dc converters," *Proc of IEEE INTELEC*, vol. 2, pp. 65–68, 2001.

[7] J. L. G. Hung and R. Nelms, "Pid controller modifications to improve steady-state performance of digital controllers for buck and boost converters," *Proc of IEEE APEC*, vol. 1, pp. 381–388, 2002.

[8] D. Maksimovic, R. Zane, and R. Erickson, "Impact of digital control in power electronics," *Proc of IEEE ISPSD*, pp. 13–22, 2004.

[9] S. Musunuri, P. Chapman, J. Zou, and C. Liu, "Design issues for monolithic dc-dc converters," *IEEE Transactions on Power electronics*, vol. 20, no. 3, pp. 639–649, 2005.

[10] G. Wei and M. Horowitz, "A fully digital, energy-efficient, adaptative power-supply regulator," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 4, pp. 520–528, 1999.

[11] B. J. Patella, A. Prodic, A. Zirger, and D. Maksimovic, "High-frequency digital pwm controller ic for dc-dc converters," *IEEE Transactions on Power electronics*, vol. 18, no. 1, pp. 438–446, 2003.

[12] W. Stefanutti, P. Mattavelli, S. Saggini, and M. Ghioni, "Autotuning of Digitally Controlled Buck Converters Based on Relay Feedback," in *Power Electronics Specialists Conference, 2005. PESC '05. IEEE 36th*, Recife, 2005, pp. 2140–2145.

[13] Z. Zhao, H. Li, A. Feizmohammadi, and A. Prodic, "Limit-cycle Based Auto-tuning System for Digitally Controlled Low-power SMPS," in *Applied Power Electronics Conference and Exposition, 2006. APEC'06. Twenty-First Annual IEEE*, Mar. 19–23, 2006, pp. 1143–1147.

[14] W. Xiao and W. G. Dunford, "Fuzzy logic auto-tuning applied on DC-DC converter," in *Industrial Electronics Society, 2004. IECON 2004. 30th Annual Conference of IEEE*, vol. 3, Nov. 2–6, 2004, pp. 2661–2666.

[15] I. Landau, *Identification et commande des systèmes*. Hermes, 1993, 2nd edition.

[16] I. LANDAU and A. KARIMI, "Robust digital control using pole placement with sensitivity function shaping method," *Int. J. Robust Nonlinear Control*, no. 8, pp. 191–210, 1998.

[17] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Kluwer, 2001, 2nd edition.

[18] C.C.Lee, "Fuzzy logic in control systems: Fuzzy logic controller-part i," *IEEE Trans. On system, Man and Cybernetics*, vol. 20, no. 2, pp. 404–408, 1990.

[19] D.Beasley and al., "An overview of genetic algorithms: Part 1, fundamentals," *University Computing*, vol. 15, no. 2, pp. 58–69, 1993.