Design of an Integrated Fast Battery Charger Controller on a FPGA Board

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***Abstract*-This paper presents the implementation on a Field Programmable Gate Array (FPGA) of an integrated battery charger controller for Electrical Vehicle (EV) application. The control strategy is based on cascaded loops where the currents controllers of the inner loops are integrated on a FPGA and the voltage controller of the outer loop is implemented on a processor board. The aim is to take benefits from the two devices advantages. An advanced RST controller is used to control the sinusoidal currents. The FPGA simulation results are compared to Matlab/Simulink simulations.**

I. INTRODUCTION

Nowadays, the high level of industrial applications, such as power electronics or drive applications requires technologies which allow implementing control algorithms. These technologies must ensured reliability of the control, accuracy, efficiency, flexibility and fast real time computation. During the last few years, two main digital devices technologies are used to control industrial control systems:

- Software digital control,
- Hardware digital control.

The pure software platforms are microcontrollers and Digital Signal Processor (DSP). They integrate a performing microprocessor core and many peripherals necessary to control the target in real time. Microcontrollers are based on Reduced Instruction Set Computer (RISC) core 16-bits or 32-bits with different kind of peripherals. A RISC represents a Central Processing Unit (CPU) design method to simplify instructions providing higher performance by executing instructions very quickly. Conversely, a DSP contains a high performance processor core based on hardware accelerator computing blocks and some peripherals [1]. Thanks to the two components improvements, the differences between the two concepts have been reduced. The main advantages of software digital devices are an easy adaptability, a large flexibility, immunity to the noise and stability to component variations. In spite of all these advantages, software digital controllers have fixe architectures leading to serialize the control algorithm's treatment limiting the sampling frequency in some applications [2].

Hardware digital platforms are generally based on Field Programmable Gate Arrays (FPGAs) technology. The concept is to pre-designed elementary cells and interconnections which are programmed and interconnected by the designer [3]. This approach allows design errors which had only been recognized at late step of development to be corrected, by simply reprogramming the FPGA thereby allowing the interconnectivity of the components to be changed as required [4]. Associated to fast analog digital converters (ADCs) and despite their complexities, control algorithms are computed in few microseconds by the FPGA. It also allows the implementation of different control functions for a full SoC (System on Chip) integration [5]. Research has been done with success on the modeling and experiment in real time for many electrical power systems using FPGA [6]-[10].

In order to friendly design new controllers and validate the concept, a new FPGA board made by dSPACE is used in this work. This board allows communication with a DSP or a processor through a PHS bus. The FPGA controller is developed with Matlab/Simulink tool and Xilinx blockset library. This tool simplifies the control implementation for designers with no need to VHDL code except for complex functions.

This paper presents the implementation of a fast battery charger controller on an FPGA and a processor boards. The paper is organized as follow. In section II, the system and its analytic model are presented. We consider the control of the specific power converter topology that can be used both for charge or traction in an Electrical Vehicle (EV) [11]-[12]. This power converter is designed to reduce the number of passive and active devices and therefore to minimize volume, weight and global cost. In section III, the design of the FPGA-based current controller is presented. After a short hardware description, an advanced RST controller design is detailed. This controller is synthesized considering a sinusoidal reference. This provides a nearly zero tracking error for sinusoidal current references. Section IV shows a comparaison between Matlab/Simulink and FPGA simulations. Finally, the last section gives some perspective of future work.

II. FAST BATTERY CHARGER MODEL

The battery charger topology studied in this paper is designed to reduce the number of power electronics devices by using the same power converter for different functions. In charging mode, this converter can be connected to the grid in a single-phase or a three-phase configuration. For both

possibilities, the phases of the EV electric machine are used as filtering power inductors. The overall problem is presented in [13]-[14] and the traction mode operation is described in [15]. In this paper, the control of the AC/DC converter in the three-phase connection mode to the grid is studied. In this configuration called fast charger mode, it is possible to obtain an entire battery charge in 30 minutes against around 8 hours in the slow charge mode corresponding to a single-phase connection of the power converter to the grid.

The architecture of the system is shown in Fig.1. This architecture has two distinct parts: the power circuit and the real time control that will be described in the next section.

The power converter is a two three-phase interleaved PFC (Power Factor Corrector), where each phase of the AC grid is connected to two parallel PFC converters. This connection is realized through the midpoint of each winding of the electric motor. This average state space model is as follows:

$$\dot{\boldsymbol{X}} = \boldsymbol{A_c X} + \boldsymbol{B_c}(\boldsymbol{X})\boldsymbol{u} + \boldsymbol{D_c} \tag{1}$$

$$\boldsymbol{Y} = \boldsymbol{CX}, \quad (\boldsymbol{C} = \mathbf{I_6}) \tag{2}$$

with,

$$\boldsymbol{X} = [i_{1a}\ i_{2a}\ i_{1b}\ \ i_{2b}\ i_{1c}\ i_{2c}\ U_{dc}]^T \tag{3}$$

$$\boldsymbol{A_c} = -\boldsymbol{R_s}\begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} & Y_{15} & Y_{16} & 0 \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} & Y_{25} & Y_{26} & 0 \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} & Y_{35} & Y_{36} & 0 \\ Y_{14} & Y_{13} & Y_{34} & Y_{44} & Y_{45} & Y_{46} & 0 \\ Y_{51} & Y_{52} & Y_{53} & Y_{54} & Y_{55} & Y_{56} & 0 \\ Y_{61} & Y_{62} & Y_{63} & Y_{64} & Y_{65} & Y_{66} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1/R_{load}r_sC \end{bmatrix} \tag{4}$$

and

$$\boldsymbol{B_c} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} & Y_{15} & Y_{16} & 0 \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} & Y_{25} & Y_{26} & 0 \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} & Y_{35} & Y_{36} & 0 \\ Y_{14} & Y_{13} & Y_{34} & Y_{44} & Y_{45} & Y_{46} & 0 \\ Y_{51} & Y_{52} & Y_{53} & Y_{54} & Y_{55} & Y_{56} & 0 \\ Y_{61} & Y_{62} & Y_{63} & Y_{64} & Y_{65} & Y_{66} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1/C \end{bmatrix}$$

$$\times \begin{bmatrix} U_{dc} & 0 & 0 & 0 & 0 & 0 \\ 0 & U_{dc} & 0 & 0 & 0 & 0 \\ 0 & 0 & U_{dc} & 0 & 0 & 0 \\ 0 & 0 & 0 & U_{dc} & 0 & 0 \\ 0 & 0 & 0 & 0 & U_{dc} & 0 \\ 0 & 0 & 0 & 0 & 0 & U_{dc} \\ -i_{1a} & -i_{2a} & -i_{1b} & -i_{2b} & -i_{1c} & -i_{2c} \end{bmatrix} \tag{5}$$

$$\boldsymbol{D_c} = -[V_a\ \ V_a\ \ V_b\ \ V_b\ \ V_c\ \ V_c]^T \tag{6}$$

where $\boldsymbol{X}$ represents the state vector, $\boldsymbol{u}$ is the control vector, i.e. the six half bridge duty cycles, equal to $[d_{1a}\ d_{2a}\ d_{1b}\ d_{2b}\ d_{1c}\ d_{2c}]^T$. $\boldsymbol{D_c}$ is a measurable disturbance (grid voltage V_a, V_b and V_c) and $\boldsymbol{R_s}$ is the matrix of the stator resistance. R_{load}, r_s, C are the load charge, the stator resistance and DC bus capacity.

In $\boldsymbol{A_c}$ and $\boldsymbol{B_c}$, terms $\boldsymbol{Y_k}$ used are admittances. The control matrix $\boldsymbol{B_c}$ depends on the DC bus voltage variable U_{dc}, this matrix is multiplied by the control vector $\boldsymbol{u}$ gathering the duty cycles d_k of each power converter half-bridge. The system is therefore non-linear.

It's conceptually very interesting to use the winding of the electric machine to filter the currents drawn by the power converter but this leads to a different and more complicated control than for a classical PFC converter that uses separated inductors. In fact, the state space model of the system defined by equations (1) to (6), shows coupling terms due to mutual inductances between the machine windings.

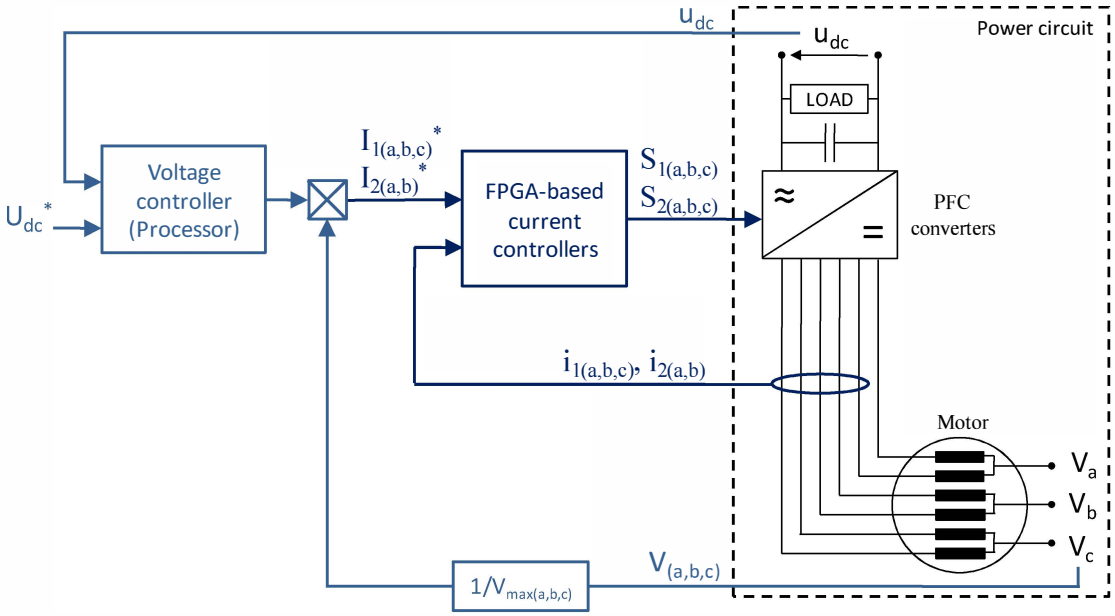

Fig. 1. Proposed control system

III. FPGA-BASED CURRENT CONTROL

A. Introduction

The control architecture developed for this converter is a cascaded loop, as shown in Fig.1. The voltage regulator must maintain the DC bus voltage U_{dc} at a defined constant value whatever the load variations. The output of the voltage controller gives the amplitudes of current references. This value is multiplied by unity sinusoidal waveforms calculated from the grid voltages V_a, V_b, V_c. The results are respectively the current references $I_{1,2a}^*$, $I_{1,2b}^*$, $I_{1,2c}^*$. Then, the FPGA-based controller generates the 6 duty cycles (i.e. input vector u) and thus the 12 switching control signals $S_{1(a,b,c)}$ and $S_{2(a,b,c)}$.

The current error must be as low as possible for two reasons. First, because if the same current flows in the half windings of each machine phase; we can obtain the required elimination of the rotating magnetic field at the stator level. Next, we must ensure compliance of the battery charger with the international standard IEC 61000-3-4 that gives the maximum levels for the current harmonics absorbed to the grid. An almost unity power factor is therefore required and can be obtained by correctly controlling AC currents grid ($i_{1(a,b,c)}$, $i_{2(a,b,c)}$) in order to follow the sinewave references.

B. Properties of FPGA Board

As presented in Fig.2, the basic architecture of a FPGA contains configurable logic blocks (CLBs) and I/O blocks. This structure allows modification in a circuit's functionality without replacing hardware. A specific circuit is implemented as a specific configuration of the internal logic cells [16]. The configurable logic blocks are connected together via a switched network, this interconnection network is programmable by user. The external connections between the internal architecture and the external environment are realized by I/O pins. The basic structure also integrates DSP blocks which are not represented on the picture. The DSP blocks perform tasks such as resource-saving multiplications.

The proposed currents control is implemented on a Xilinx VIRTEX®-5 FPGA board associated with 6 ADC/DAC, 16 digital I/O channels and a connection to the processor board DS1006 of the DSPACE system via a PHS bus. Table I gives some specifications of the VIRTEX®-5 FPGA.

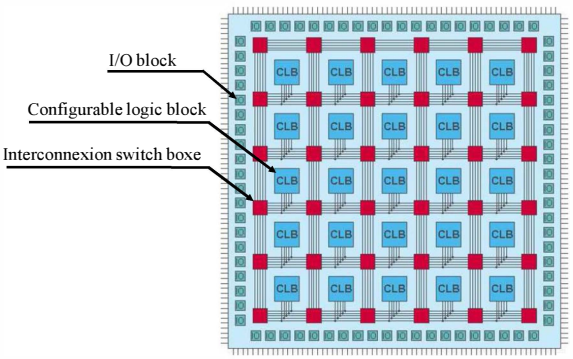

Fig. 2.FPGA's basic architecture

TABLE I
FPGA'S SPECIFICATIONS

Number of I/O	640
Number of Logic cells	94 298
Number of DSP blocks	640
Clock frequency	100 MHz
Memory size (RAM blocks)	8784 kBits

The FPGA board is programmed via the RTI FPGA Programming Blockset from dSPACE and the Xilinx System Generator. An integrated library giving many functions is available and complex HDL code can also be integrated in a self designed Black Box.

This tool allows testing the interactions between the processor program and the FPGA design using an offline simulation before experiments. The interactions between processor and FPGA boards are realized through 32 buffers In/Out channels and 128 registers In/Out channels. A register has a data width of 32 bits. In addition to all these performances, this board was chosen because it allows the generation of at least 12 synchronizes switching control signals.

C. Current Control Design

This section presents the design of the current control using an advanced RST controller. Complementary information about the design method of RST controllers have been presented in [17]. As mentioned before, the studied system Equ. (1) has coupled and non-linear state equations. In the proposed controller design, the mutual inductances of the electrical motor are not considered and measurable disturbances are supposed compensated. Fig. 3 shows the block diagram of the simplify system for the current loop. These assumptions are used only to design the controller. From these hypotheses, the transfer functions of the system are as follows:

$$\frac{i_k}{\tilde{V}} = \frac{1}{r_s + L_k p} \quad \text{where} \quad k = [1a, 2b, 1b, 2b, 1c, 2c] \tag{7}$$

$$\frac{U_{dc}}{i_{dc}} = \frac{R_{load}}{1 + R_{load} C p} \tag{8}$$

$$i_{dc} = -(i_{1a} d_{1a} + i_{2a} d_{2a} + i_{1b} d_{1b} + i_{2b} d_{2b} + i_{1c} d_{1c} + i_{2c} d_{2c}) \tag{9}$$

i_{dc} represents the DC link current, L_k the proper inductance of each phase, R_{load} the resistive load and C the DC bus capacitor.

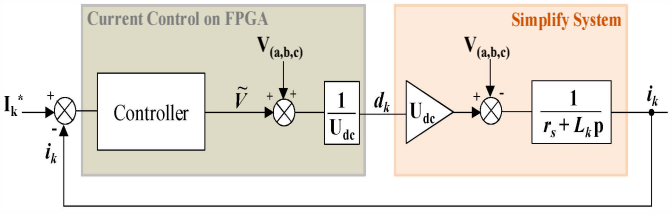

Fig. 3.Block diagram of the current control loop

The state space model presented in the previous sections has 7 state variables. However, it should be noted that the system have only 6 degrees of freedom. In the case of a balance system, the following expression allows to reduce the number of state variables:

$$\sum i_k = 0 \tag{10}$$

Consequently, in the proposed control scheme, only 5 currents and one voltage controllers are used as shown in Fig.4.

The design of the proposed advanced RST controller, used for the currents control, introduces the current references waveforms at the design step. The aim is to obtain a better tracking of the sinusoidal references and therefore to minimize the dynamic error. The design procedure is composed of 3 steps as follows:

Step 1: Discrete time open-loop transfer function

The open-loop transfer function of a first order system is as follows:

$$H(z^{-1}) = \frac{B}{A} = K\frac{(1-a)z^{-1}}{1-az^{-1}} = \frac{B^-B^+}{A^-A^+} \tag{11}$$

where $a = e^{-Ts/\tau}$, T_s is the sampling time, $\tau = L_k/r_s$ is the system time constant. Polynomials of the open-loop transfer function are defined such as B^- and A^- contain all the unstable and extra zeros and pure delays of the plant that will not be compensated. B^+ and A^+ contain all the other terms. In our case, A^-, A^+, B^- and B^+ are defined as follows:

$$\begin{aligned} A^- &= 1 - az^{-1} \\ A^+ &= 1 \\ B^- &= K(1-a)z^{-1} \\ B^+ &= 1 \end{aligned} \tag{12}$$

Step 2: Auxiliary Diophantine equation

To design the controller by pole placement, a transfer model of the closed-loop system is searched from the following expression:

$$F_m(z^{-1}) = \frac{B_m(z^{-1})}{A_m(z^{-1})} \tag{13}$$

As shown on Fig. 5, the closed-loop transfer function is defined as:

$$\frac{y(z^{-1})}{y_c(z^{-1})} = \frac{BT}{AS+BR} \tag{14}$$

then, the equality between Equ. (13) and Equ. (14) must be performed. $F_m(z^{-1})$ is chosen arbitrarily in order to impose the

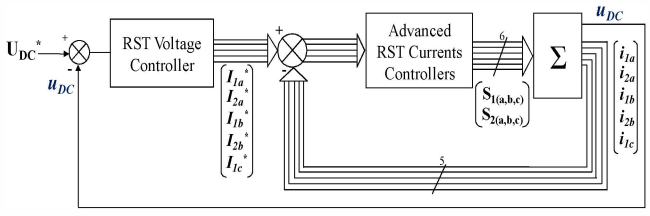

Fig. 4.Control block diagram

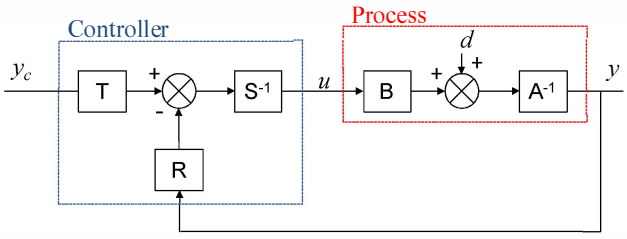

Fig. 5. RST controller schema block

desired closed-loop poles, with the constraint that $B_m(z^{-1})$ has to contain as a factor, the pure delay of the system, its unstable zeros (uncompensable) and zeros that the designer decides not to compensate, i.e. $B^-(z^{-1})$.

$$B_m = B^- B'_m \tag{15}$$

According to Equ. (14), the partial transfer function from reference y_c to error signal $\varepsilon(z^{-1}) = y_c(z^{-1}) - y(z^{-1})$ is given by:

$$\frac{\varepsilon(z^{-1})}{y_c(z^{-1})} = 1 - F_m(z^{-1}) = \frac{A_m - B_m}{A_m} \tag{16}$$

In order to cancel steady state errors in response to a sinusoidal reference, it follows that magnitude of the transfer function ε/y_c at a given angular frequency ω_s must be null:

$$\left|\frac{\varepsilon(z^{-1})}{y_c(z^{-1})}\right|_{z=e^{j\omega T_s}} = \left|\frac{A_m - B_m}{A_m}\right|_{z=e^{j\omega T_s}} \tag{17}$$

Therefore, it is necessary to introduce a zero transmission into the transfer function for this frequency. For that, the product $(1 - e^{j\omega_s T_s} z^{-1})(1 - e^{-j\omega_s T_s} z^{-1})$ must divides $A_m - B_m$. Therefore, a unknown polynomial $L(z^{-1})$ exist such that:

$$(1 - 2cos\omega_s T_s z^{-1} + z^{-2})L + B^- B'_m = A_m \tag{18}$$

This equation is called the auxiliary Diophantine equation [18]. The unknown polynomial L and B'_m are defined as:

$$\begin{aligned} L(z^{-1}) &= l_0 + l_1 z^{-1} \\ B'_m(z^{-1}) &= b'_0 + b'_1 z^{-1} \end{aligned} \tag{19}$$

The resolution of Equ. (18) gives:

$$\begin{aligned} b'_0 &= (2e^{-\xi\omega_0 T_s}\cos(\omega_p T_s) - 2)/K(1-a) \\ b'_1 &= (e^{-\xi\omega_{n0} T_s} - 1)/K(1-a) \\ l_0 &= 1 \\ l_1 &= 0 \end{aligned} \tag{20}$$

Therefore, the polynomial $B_m(z^{-1})$ is now defined.

Step 3: Diophantine equation

The block diagram of a regular RST controller is presented in Fig. 5. The the closed-loop transfer function is given by:

$$y = \frac{BT}{AS+BR} y_c + \frac{S}{AS+BR} d \tag{21}$$

with y the output, y_c the reference and d a disturbance. Equ. (21) shows that it is necessary to take $S(1) = 0$ to reject in steady state the perturbation d. The degree of $T(z^{-1})$ is a parameter that is defined by the designer.

Degrees of S and R depend on the type of controller: proper or strictly proper. The choice of a strictly proper controller is done. So, if the degree of polynomial A is equal to n, degree of polynomials S, R and A_m are respectively equal to n+1, n and 2n+1. Thus, polynomials R, S *and* A_m are defined as follows:

$$\begin{matrix} R(z^{-1}) = r_1 z^{-1} + r_0 \\ S(z^{-1}) = (1 - z^{-1})(s'_1 z^{-1} + s'_0) \\ A_m(z^{-1}) = 1 - 2e^{-\xi\omega_0 T_s}\cos(\omega_p T_s) z^{-1} + e^{-\xi\omega_0 T_s} z^{-2} \end{matrix} \quad (22)$$

with $\omega_p = \sqrt{1-\xi^2}$. As mentioned before, the polynomials are obtained by identification of the following expression:

$$\frac{B^+B^-T}{B^+(AS'+B^-R)} = \frac{B^-B'_m}{A_m} \quad (23)$$

where $S=B^+S'$. A resume of R, S and T coefficients are done in the next table.

TABLE II
SYNTHESIS OF R, S AND T COEFFICIENTS

	Expression
r0	$(2e^{-\xi\omega_0 T_s}\cos(\omega_p T_s) + 1 + a)/K(1-a)$
r1	$(e^{-\xi\omega_0 T_s} - a)/K(1-a)$
s'0	1
s'1	-1
t0	$(2e^{-\xi\omega_0 T_s}\cos(\omega_p T_s) - 2cos(\omega_0 T_s))/K(1-a)$
t1	$(e^{-\xi\omega_0 T_s} - 1)/K(1-a)$

An example of the implementation of polynomials on the FPGA board is available in Fig.6, where a transfer O/I is presented, containing 6 multipliers, 3 additions and 2 pure delays. The implementation of the whole structure based on the same principle uses 18% of slices number, 10% of RAM memories and 10% of embedded multipliers. We can notice that the level of utilization of FPGA resources is low, although the design is not really optimized.

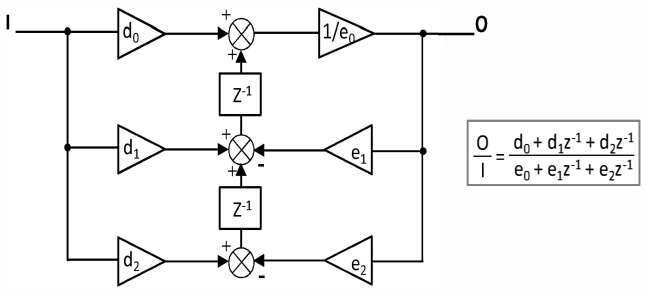

Fig. 6.Example of implementation on the FPGA

IV. SIMULATION RESULTS

As mentioned previously, before the implementation in real time, the algorithm can be tested using offline simulations. The RST currents controllers are design on the FPGA board, while the RST voltage controller is implemented on the processor board.

In this part, a comparison between floating point simulation (Matlab/ Simulink) and fixed point simulation (Matlab/ Simulink/ Xilinx System Generator XSG) is done. These simulations allow validating the control law before the experimentation. For the fixed point design, the choice of each data width is very important, at risk of losing in information and in precision. The sampled time equal to 10 µs is chosen to compute the controllers.

The value of the polynomials' coefficients and the computed disturbance are defined on the processor board and send to the FPGA via registers for modifications in real time.

Fig. 7 shows for a variation of DC link voltage U_{dc}, currents i_{1a}, i_{1b} and i_{1c} absorbed to the grid in each simulation case. By analyzing the voltage and currents responses obtained in floating point simulation and fixe point one, the global forms are equivalent and follow quiet well the references. Nevertheless, a zoom on currents i_{1a} in Fig. 7 shows that there is an amplitude error for the two configurations. These differences are due to the fact that $R(1)\neq T(1)$. This inequality could be removed by computing B`m such that R(1)=T(1). Moreover, the relative error between the reference and the controlled current are bigger for the FPGA simulation. Several ways are possible to try to reduce these errors, notably by increasing the bits number of the input/output registers.

V. CONCLUSION

This paper has presented a comparison between simulations done with Matlab/Simulink and simulations computed with both Matlab/Simulink and XSG for a AC/DC power converter, in order to validate the implementation on a FPGA board. After a short description of the fast battery charger topology, the FPGA-based currents controls have been presented, where, some specifications of the FPGA have been introduced and a method to design an advanced RST controller has been given. The comparison results presented in section IV proves that the implementation on the FPGA is quiet similar to the floating simulation, although some improvement can be done. For designers who are not specialized in HDL language or in FPGA architecture, this software is a friendly development tool.

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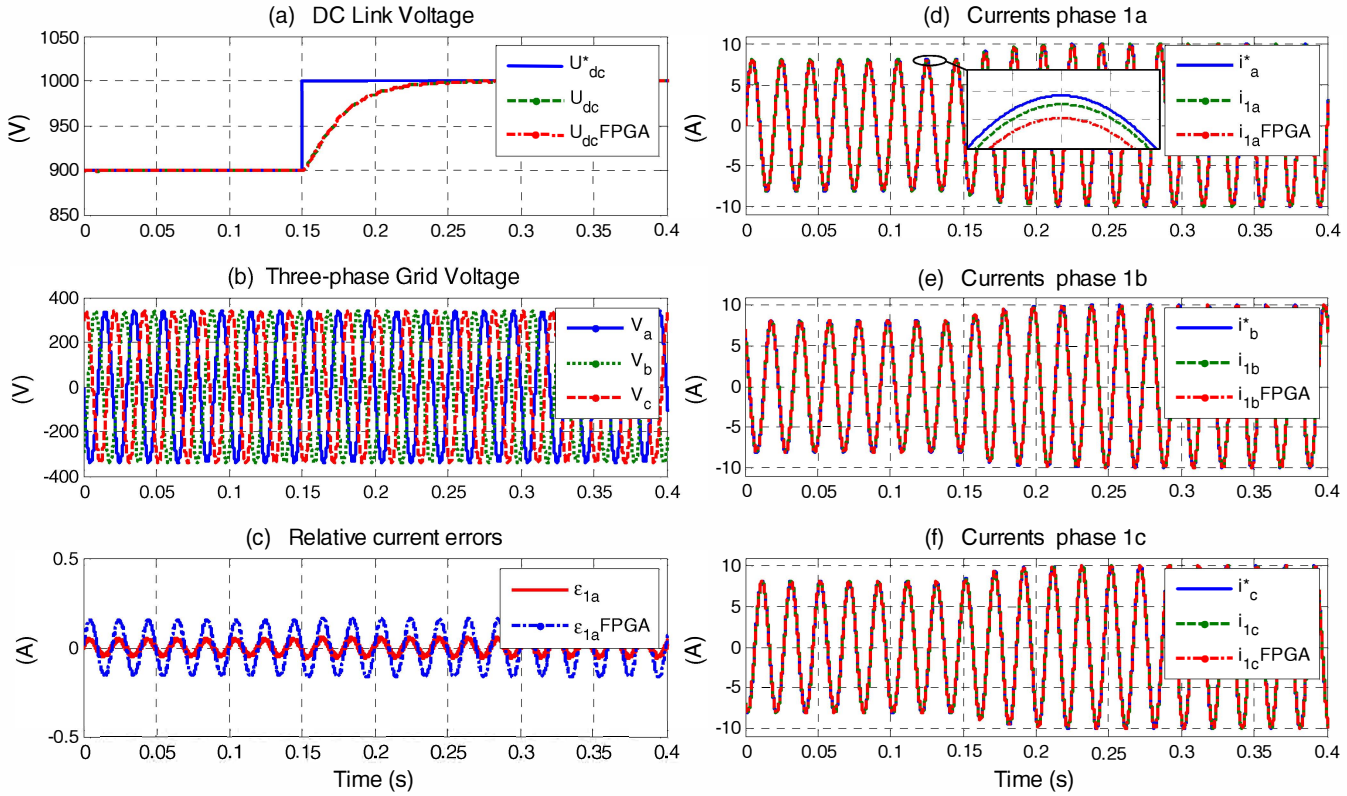

Fig. 7. Results for Matlab/Simulink simulation and FPGA simulation

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