Digital control strategies for switch-mode power supply

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***Abstract*— Analogue control of monolithic DC/DC converters is coming to a limit due to high switching frequency and a request for large regulation bandwidth. Digital control is now experimented for low-power low-voltage switch-mode power supply. Digital implementation of analogue solutions does not prove real performances. Other digital controllers have been experimented but applied to discrete converters. This paper compares a classical digital controller to a possible alternative strategy. Sensitivity functions are used to compare controller performances. RST algorithm determined by robust pole assignment shows better performances.**

I. Introduction

For many years now, there is a trend to embed power management unit inside portable devices like cellphone, personal digital assistant or MP3-player. Most portable devices use a battery ranging voltage between 5.5V when in charge, 3.3V during discharge lifetime and down to 2.7V when empty. Devices embed various functions supplied from various voltages. Processors require 1.8V down to 1.2V while backlight led system require 20V at least. Non isolated DC/DC converters are considered in place of low-drop out regulators for the sake of efficiency. This paper will now address only step-down conversion and associated buck architecture or step-down switch-mode power supply (SMPS).

A full-analogue synchronous buck converter is pictured in Fig. 1. Except the passive L-C output filter, all blocks are integrated monolithically using CMOS standard technology [1], [2]. A 2-poles/2-zeros compensator is implemented to achieve a maximal regulation bandwidth, maximal transient performance and maximal accuracy. The switching frequency must be kept unchanged for EMC filtering purpose.

[3] details a 10mW SMPS with 100MHz switching frequency and 91% peak efficiency, but poor transient performances. A 100MHz SMPS, 80% peak efficiency, 20MHz regulation bandwidth is presented in [4]. Moreover the design is compatible with standard CMOS process. Whatever analogue control presents some limitations. First of all, the design of the compensator is not automated and the design engineer needs to take care of a trade-off between performances, accuracy and stability [5]. When R-C constant have been set, manufacturing introduces deviation with respect to design values and calibrations are required. So a lot of efforts are put on alternative approaches as digital control.

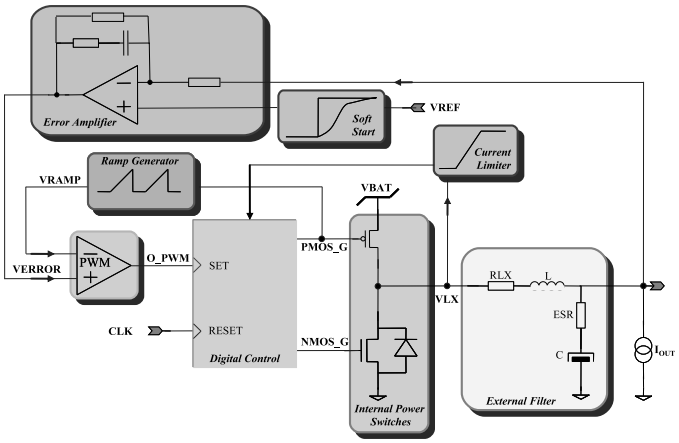

Fig. 1. Schematic synchronous step-down SMPS

Digital control is not new in the field of Power Electronics. It is often associated with DSP or other processor-like implementation [6]–[9]. Generally the digital control system presents sufficient resources to accommodate the modest switching frequency of the converter, in the kHz range. In embedded applications, switching frequencies in the MHz and plus range are necessary in order to reduce the size of passive components [10].

Basically most published papers consider a discrete-time equivalent to the analogue compensator [11], [12]. Most efforts are put on a suitable integration of A-to-D converters and the PWM function that is then called a digital PWM (DPWM). Other papers introduce a digital controller based on look-up tables [13]. Complex algorithms have been published but applications concern large-power converters where the energy consumption of the digital controller is nearly negligible with respect to the converter power losses [14]. It is not the case in a low-power sub-1V monolithic SMPS.

Digital-PWM introduces a trade-off between the operating clock frequency and the accuracy. If a ratio of 8-to-1 is selected with respect to the SMPS switching frequency, then a 10MHz converter requires a DPWM with a 80MHz bandwith, and only 255 duty ratio values are acceptable. This kind of DPWM is implemented through a cascade of CMOS inverters where each output is connected to a multiplexer. The DPWM delays an input edge and the MOSFET transistor gate signal is

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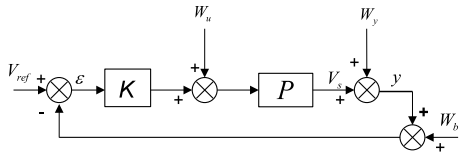

Fig. 2. Block diagram of the SMPS

obtained by logic combination of the initial edge signal with the multiplexer output [12]. The limited number of duty ratio values leads to limit-cycle behaviour of the converter and the accuracy of the output voltage may not be controlled. The A-to-D converter can be replaced by a multi-level comparator and associated to a finite state-machine controller [15]. A 50MHz digital system is necessary to control a 100kHz converter with 200Hz of regulation bandwidth.

Literature shows that DPWM-less architectures are experimented. Look-up table architecture is then an alternative worth the effort since the power consumption may be limited and at least controlled. Standard CMOS technologies offer high operating frequencies for logic blocks. It is then compatible with 100MHz converters.

This paper investigates a robust RST control in comparison with a classical PID control. RST is an efficient strategy of digital control that can be applied to monolithic step-down SMPS. Section II introduces so-called sensitivity functions as a quantification mean to compare strategies. Section III introduces a digital PID controller. Section IV introduces a so-called RST digital controller. Simulation results are detailed in Section V.

II. Sensitivity Functions

In order to quantify system dynamics, robustness and noise rejection properties of tested controllers, sensitivity functions are introduced.

Fig. 2 represents the z-domain model of SMPS (*P(z)*) and its controller (*K(z)*) when adding control noise W_u, output noise W_y and measurement noise W_b.

From Fig. 2, it comes the following relation that leads to the sensitivity functions.

$$y = \Gamma.V_{ref} + S_{yy}.W_y + S_{yb}.W_b + S_{yu}.W_u \quad (1)$$

$$\Gamma = \frac{KP}{1+KP} = \frac{L_{yy}}{1+L_{yy}} \quad (2)$$

$$S_{yy} = \frac{1}{1+KP} = \frac{1}{1+L_{yy}} \quad (3)$$

$$S_{yb} = \frac{-KP}{1+KP} = \frac{-L_{yy}}{1+L_{yy}} \quad (4)$$

$$S_{yu} = \frac{P}{1+KP} = \frac{P}{1+L_{yy}} \quad (5)$$

where Γ is the closed loop transfer function, S_{yy}, S_{yb} and S_{yu} are respectively the output-to-output, measure to output and control-to-output sensibility functions.

Constraints or disturbance rejections are naturally expressed in terms of frequency sensitivity shapes. For a given controller,

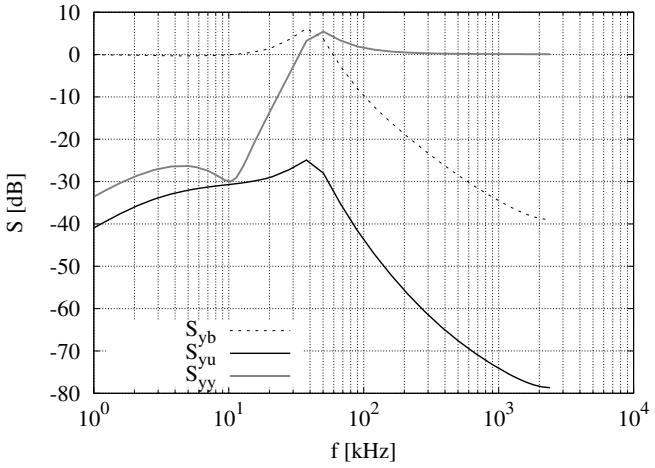

Fig. 3. Sensitivity Functions Example

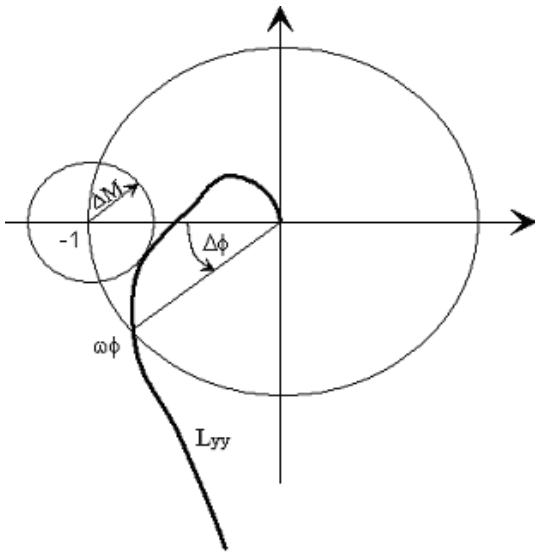

Fig. 4. Typical Nyquist plot of L_{yy}

the sensitivity functions allow to evaluate the controller behavior in relation to the desired attenuation constraints.

Fig. 3 is an example of the gain plot of sensibility functions. The gradient of S_{yy} at low frequency determines the dynamic behavior of the system. The bandwidth of S_{yb} defines the influence of noise on the output voltage and the closed loop bandwidth since it has the same transfer function as Γ expect the sign. The gain of S_{yu} verifies the rejection of control perturbations such as the PWM-related noises.

In addition, from the maximum value of S_{yy}, the margin module can be determined. The module margin ΔM is defined as the minimum distance of L_{yy} to the critical locus -1 in the Nyquist plan (Fig. 4). The module margin and delay margin quantify the robustness of the modeling uncertainties. The delay margin $\Delta\tau$ is deduced from the phase margin $\Delta\Phi$ by $\Delta\tau = \frac{\Delta\Phi}{\omega_\Phi}$.

In order to ensure robustness, the module margin ΔM is

kept higher than 0.5 and the delay margin must be higher than sampling period.

III. PID CONTROL

The PID controller is presented for comparison purpose with the RST controller. A digitally controlled buck converter operating in continuous conduction mode (CCM) can be regarded as a second order discrete-time system [16]:

$$P(z) = \frac{b_1 z + b_2}{z^2 + a_1 z + a_2} \tag{6}$$

A discrete-time PID controller can be written as:

$$K_{PID}(z) = \frac{r_0 z^2 + r_1 z + r_2}{(z-1)(z+s_1)} \tag{7}$$

where r_0, r_1, r_2, s_1 are the controller parameters to be determined.

By cancelling the poles of $P(z)$ with the zeros of $K(z)$, the closed-loop reference to output voltage transfer function is:

$$\begin{aligned} \Gamma &= \frac{KP}{1+KP} \\ &= \frac{r_0 b_1 z + r_0 b_2}{z^2 + (s_1 - 1 + r_0 b_1) z + (r_0 b_2 - s_1)} \\ &= \frac{r_0 b_1 z + r_0 b_2}{z^2 + p_1 z + p_2} \end{aligned} \tag{8}$$

p_1 and p_2 are defined by the desired closed-loop dynamics which corresponds to a second order dynamics with a pulsation ω_{cl} and a damping ratio ξ_{cl}. The conditions for the cancellation of the poles of $P(z)$ by the zeros of $K(z)$ are:

$$\begin{aligned} r_0 &= \frac{1 + p_1 + p_2}{b_1 + b_2} \\ r_1 &= a_1 r_0 \\ r_2 &= a_2 r_0 \\ s_1 &= r_0 b_2 - p_2 \end{aligned} \tag{9}$$

In order to have a large enough closed-loop bandwidth, the desired closed-loop dynamic is set to about 15 times the open-loop dynamic and a damping ratio of 0.7.

For the circuit elements with L = 10μH, C = 22μF, R = 3Ω, V_{BAT} = 3.3V, the controller parameters are: $r_0 = 431.64$, $r_1 = -860.28$, $r_2 = 428.73$ and $s_1 = -0.83$. The corresponding sensitivity functions are presented in Fig. 5.

For an output disturbance with a pulsation of ω_1 (LC filter resonance), the gain of S_{yy} on ω_1 gives the information on the disturbance rejection. In the study case, $\omega_1 = 10.568$kHz. It can be seen that $S_{yy}(\omega_1)$ is about -25dB.

Concerning the stability robustness, the module, phase and delay margins are: $\Delta M = 0.88$, $\Delta\varphi = 66.9°$, $\Delta\tau = 6.6 T_e$.

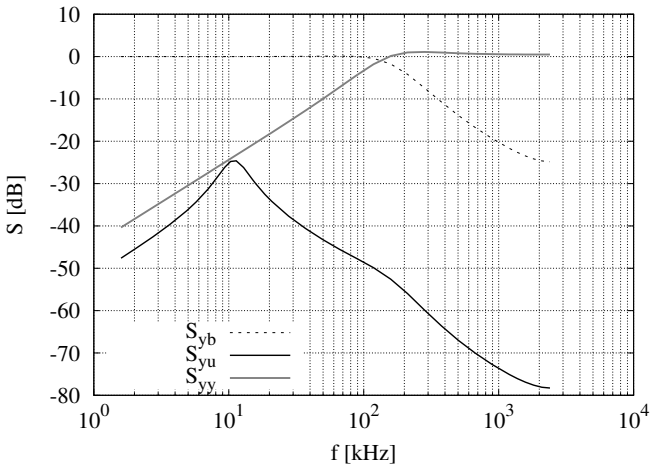

Fig. 5. Sensitivity functions for PID controlled system

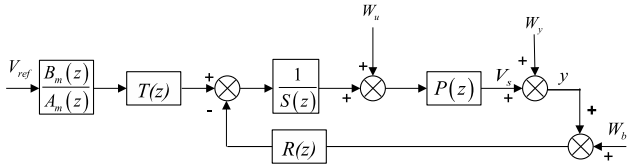

Fig. 6. RST control structure

IV. ROBUST RST CONTROL

RST control realizes a relevant approach for linear Single Input Single Output (SISO) systems [17]. The structure of a RST control is presented in Fig. 6.

The sensitivity functions can be expressed as:

$$S_{yy} = \frac{AS}{AS + BR} \tag{10}$$

$$S_{yb} = \frac{-BR}{AS + BR} \tag{11}$$

$$S_{yu} = \frac{BS}{AS + BR} \tag{12}$$

From these expressions, it can be noted that the three sensitivity functions have the same denominator $D = AS + BR$ which determines the dynamics of disturbance rejections. The knowledge of acceptable disturbances leads to design the RST controller in terms of poles and zeros assignments. For example, to insure the output accuracy, a pole for z=1 in S(z) is necessary for static error elimination.

For an output disturbance with the pulsation of ω_1, the lower gain of S_{yy} at ω_1, better the attenuation of the output disturbance rejection. However, the diminution of S_{yy} at ω_1 can induce an augmentation of the maximum value of S_{yy} which is inversely proportional to ΔM. The diminution of ΔM reduces the controller robustness.

How to determine a controller which makes a compromise between the robustness and a good rejection of disturbances? This can be translated as an optimization problem by defining

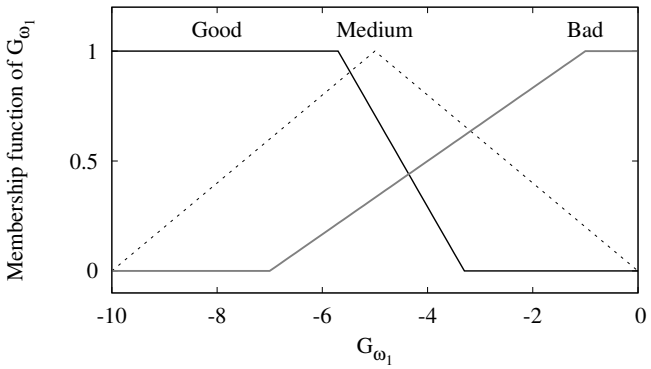

Fig. 7. Input membership function for G_{ω_1}

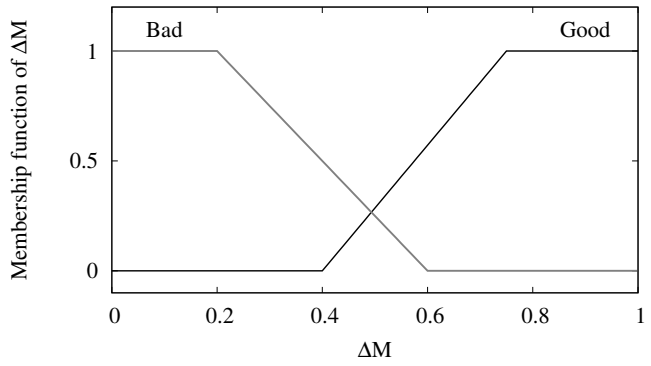

Fig. 8. Input membership function for ΔM

a cost function which qualifies the controller robustness and noise rejection properties.

Fuzzy logic is more suitable to qualify the robustness of a controller and noise rejection properties [18]. Indeed the frontier between a good controller and a bad controller is not strict. For example, if one considers the module margin is correct if it is higher than 0.5, it is clear that a controller will not be qualified as a bad robustness to good by crossing this value. With membership functions of fuzzy logic, the controller quality can be evaluated continually from bad to good across medium.

An example of membership functions qualified the gain at ω_1 (G_{ω_1}) and the module margin (ΔM) is shown in Fig. 7 and Fig. 8.

G_{ω_1} is normed on {-10 0} and ΔM uses its natural scale.

The output membership function is given in Fig. 9.

The stability robustness can be expressed by the fuzzy rules defined in Tab. I.

TABLE I
FUZZY RULES USED

G_{ω_1} / ΔM	**Bad**	**Medium**	**Good**
Bad	Bad	Bad	Medium
Good	Bad	Medium	Good

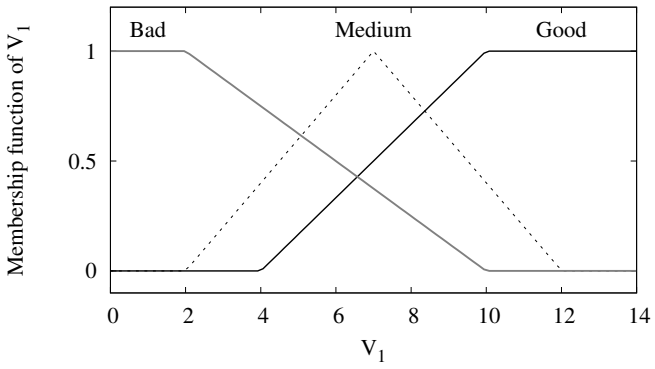

Fig. 9. Output membership functions

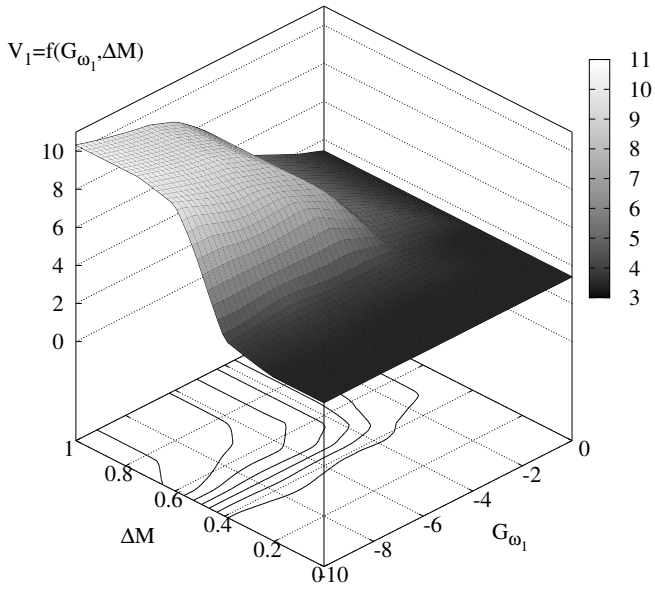

Fig. 10. Fuzzy function V_1

After "disfuzzyfication", the robustness analyse is quantified by the function V_1 = f(G_{ω_1},ΔM) which corresponds to a surface as presented in Fig. 10. It can be seen that for $\Delta M > 0.5$, the lower the values of G_{ω_1}, the better the output function V_1.

On the same way, other membership functions and fuzzy rules in relation with delay margin and with other sensitivity functions can be defined to quantify constraints of robustness and satisfies the requirements of disturbance rejection performances. The cost function to maximize is a balanced sum of all fuzzy functions. The optimization problem is realized by a stochastic genetic algorithm [19]. The computation time can be important but it is done off line, so that is not a limitation for real time implementation.

For our example, the denominator of the sensitivity function

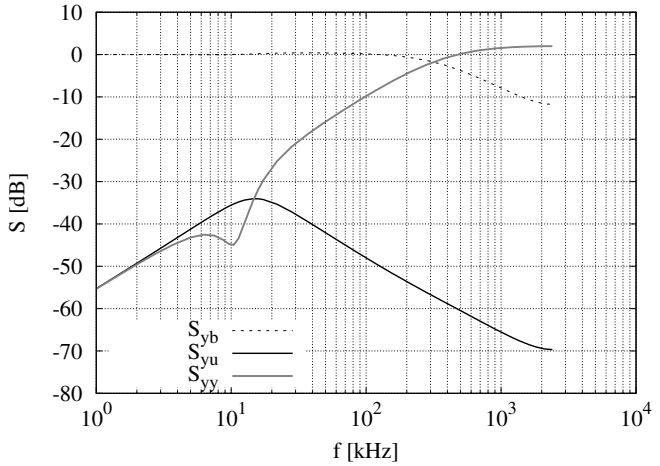

Fig. 11. Sensitivity functions for RST controller

S_{yy} is defined as follows to determine a RST controller which presents a good robustness and a good attenuation of the influence of the output disturbance at $\omega_1 = 10.568$kHz.

$$D(z) = (1 - c_0 z^{-1})(1 + c_1 z^{-1} + c_2 z^{-2}) \qquad (13)$$

where c_0, c_1 and c_2 constitute three degrees of freedom for the optimization problem. For each combination of c_0, c_1 and c_2, the fuzzy logic quantifiers evaluate the cost function. The genetic algorithm then finds the optimal solution for c_0, c_1 and c_2 over twenty generations with about thirty individuals. The corresponding optimal polynoms $R(z)$, $S(z)$ and $T(z)$ are calculated resolving the Bezout equation [17].

$$R(z) = 669.2z^2 - 1321.9z + 653 \qquad (14)$$
$$S(z) = z^2 - 1.6815z + 0.6815 \qquad (15)$$
$$T(z) = 1617.9z^3 - 4176.2z^2 + 3515.6z - 957.1 \qquad (16)$$

The corresponding sensitivity functions are given in Fig. 11.

The gain of S_{yy} on ω_1 is -39dB against -25dB for PID controller. The good robustness is keep with $\Delta M = 0.79$, $\Delta\varphi = 75.3°$ and $\Delta\tau = 3.18 T_e$.

V. Simulation Results

The simulations are done in Simulink 12. The modeling of the buck SMPS is with a hybrid model [5]. The PID controller and RST controller are modeled with standard elements of the Simulink library. Analog-to-digital converter model takes into account quantization, delay and saturation effects. The DPWM model has an 8-bit resolution [12].

After a reference tracking, a step change of load from 0 A to 0.6 A is applied at 400μs. The output voltage is compared in Fig. 13 and Fig. 14. The load transient responses of RST controller is superior to PID controller since it results in shorter rise time and produces smaller undershoot.

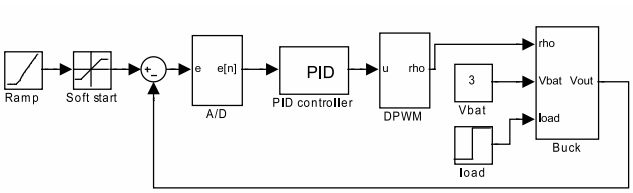

Fig. 12. Simulink model of PID digital controller for a buck converter

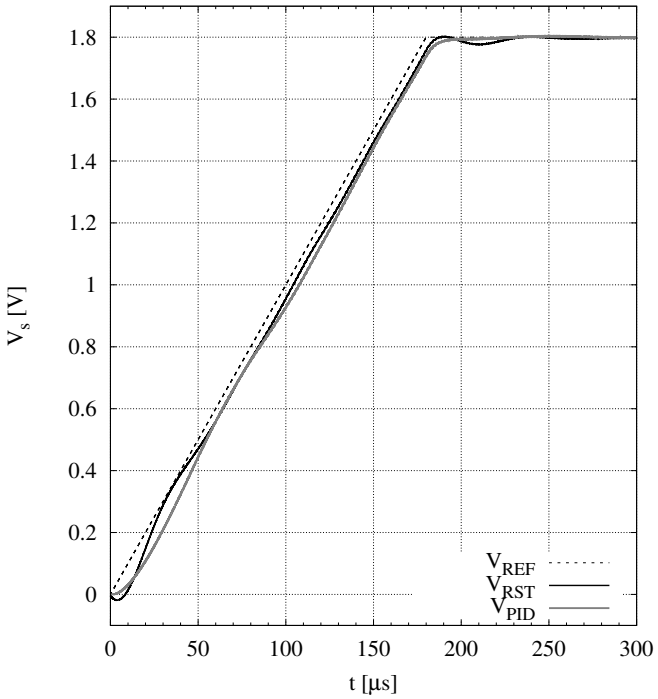

Fig. 13. Comparison of output voltage responses during reference tracking

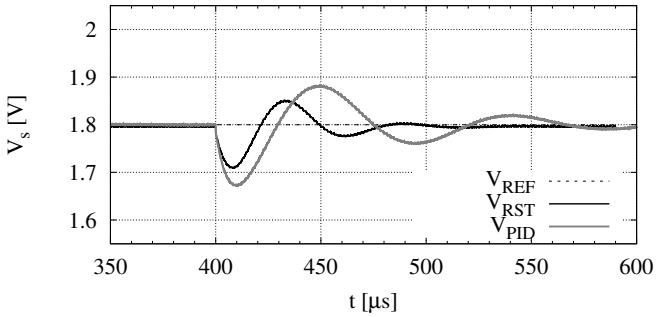

Fig. 14. Comparison of output voltage responses to load perturbation

VI. Conclusion

This paper has detailed the design of a now classical PID digital controller and one alternative as the RST strategy. RST offers better performances. Simulation results have concerned a 600kHz switching frequency converter, but results hold for higher switching frequencies. Superior performances are noted for a 10MHz buck converter. Moreover RST implementation can be achieved using one A-to-D converter and standard CMOS logic. Experimental study are currently performed using an Actel ProAsic3 FPGA board plus an additional analog I/O board. It is possible to estimate the impact of monolithic integration from experimental results as FPGA design can be translated at no cost into an ASIC version. PID like RST controller requires a fast A-to-D converter. It will probably be the angrier energy consumer in the digital control. Other alternative digital strategies are possible like hybrid approaches or direct voltage control.

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