CONTROL OF BOOST UNITY POWER FACTOR CORRECTION SYSTEMS

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Abstract

For domestic use, there are numerous switching mode power supplies, composed of a full bridge rectifier with a capacitor filter. It derives a dc voltage from the ac mains and generates a pulsed line current with high harmonic content.

This paper deals with a boost unity power factor correction system, which can be added to realise a sinusoidal line current. Two simple and fast dc capacitor voltage controllers are studied and analysed. They are compared in term of settling time, filtering of twice mains frequency and overshoots of the dc voltage under load transients. The first is based on an integral proportional controller. The second is based on identification of the disturbance and regulation using a pole placement RST controller.

The effectiveness of the proposed approach is assessed by simulations and extended to parallel connection PFC systems. A near unity power factor and very low distortion with good output voltage regulation is achieved for variable power applications.

I. Introduction

The growing number of power electronic-based equipment, both in the industrial and domestic sectors, tends to have undesirable impacts on the quality of distribution and line voltage networks. Power supply quality is specified by standards and regulations. It can be expected that the allowed distortion levels will be further reduced in the future.

There is a switched mode power supply in almost every modern domestic appliance; TV, computer, speed control regulators, electrical light dimmers and so on. Single–phase dc power supplies are usually composed of a diode rectifier with capacitor filter. This circuit generates a pulsed current with high harmonic content.

To reduce harmonic distortion, several methods are widely used, active power filters (APF), power factor correction systems (PFC), various boost topologies and others [1-3]. The boost topology is usually accomplished by inserting a boost converter between the rectifier and the filtering stage. With proper control, the boost converter permits to absorb a sinusoidal line current in phase with the supply voltage.

Generally the control of the boost converter is made up of two loops (fig. 1):
- current loop which compares the input current to the reference current. This reference is often made proportional to the input voltage.
- voltage loop which regulates the output voltage to the desired reference voltage by adjusting magnitude of the reference current.

This principle has been utilised in many commercial integrated circuits for low power (Microlinear ML4812, Unitrode UC3854, Motorola MC34261...). It has also been adapted for medium power [4][5]. These circuits present different current control strategies: zero-current switching control, average current control or instantaneous current control. The voltage control strategy usually comprises a simple proportional- integral regulator.

The current controllers display good performances, with almost a unity power factor. However, with traditional voltage controller designs, the output voltage overshoots with step changes of the load and the settling time also takes several cycles of the mains frequency.

In this paper, after a brief review of the boost-model, two dc voltage controllers are developed and compared. The goal is to improve dynamic performances and reduce the dc capacitor value of the PFC system.

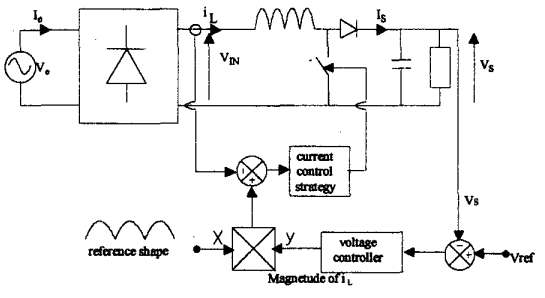

Fig. 1. Power factor correction topology

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The control objectives of the voltage loop are threefold. First, the capacitor voltage $V_S(t)$ must be regulated without bias and with fast dynamics. Second, the dc voltage fluctuations at twice network frequency must be filtered by the controller. Third, the controller must be robust against the uncertainty of the capacitor value.

Simulation results, achieved using Matlab-Simulink software are presented. Finally, the application of the PFC system at variable power is discussed. Thus, a solution to ensure a lower harmonic distortion ratio is demonstrated.

II. Boost-model and DC voltage control

The boost converter consists of two state variables: the output voltage Vs and the input current i_L as illustrated by equations (1) and (2). The quantity k is a logical variable. k representing the state of the Boost switch (k=0 switch is open, k=1 switch is closed).

$$\frac{di_L}{dt} = \frac{1}{L}V_{in} - \frac{1-k}{L}V_S \quad (1)$$

$$\frac{dV_S}{dt} = \frac{1-k}{C}i_L - \frac{V_S}{RC} \quad (2)$$

To derive the loop model we will consider, in this study, the real power balance of the PFC system (fig. 1). If the PFC operates correctly, the line current $I_e(t)$ is sinusoidal and in phase with the supply voltage $V_e(t)$.

The input power can be written as:

$$P_{in}(t) = 2V_eI_e\sin^2(\omega t) = V_eI_e(1+\cos(2\omega t)) \quad (3)$$

The power absorbed by the load is:

$$P_S(t) = V_S(t)I_S(t) = CV_S(t)\frac{dV_S(t)}{dt} + \frac{V_S^2(t)}{R} \quad (4)$$

Assuming losses in the converter are small, the power balance equation permits to write:

$$P_{in}(t) \approx P_S(t).$$

Thus, using the above relations, the voltage on the output of the capacitor can be written as :

$$V_S(t) = V_{Smean} - V_{ond}\sin(2\omega t) \text{ where } V_{ond} = \frac{P_{Smean}}{2\omega CV_S} \quad (5)$$

The dc capacitor voltage ripple presents the particularity to have double frequency of the network and a magnitude negligible compared to the average dc capacitor voltage. Note that the voltage controller can inject this ripple on the input current and causes consequently its deformation.

In the following development, we model this ripple as an external disturbance. This does not affect open loop operation. Therefore, neglecting the voltage ripple, the output power is given as:

$$P_S(t) \approx P_{in\_mean} = V_eI_e$$

$$\frac{1}{2}C\frac{dV_S^2(t)}{dt} + \frac{V_S^2(t)}{R} = P_{in\_mean}$$

Therefore, the open loop transfer function is:

$$G(s) = \frac{V_S^2}{P_{in}} = \frac{R}{Ts+1} \quad (6)$$

where $T = \frac{RC}{2}$ and s is the Laplace's operator.

The model can be represented as shown in fig. 2, where dE is the external perturbation represented by the dc capacitor voltage fluctuations due to the alternating part of $P_S(t)$.

The aim of the regulator is to adjust $V_S^2(s)$ to the reference $V_o^2(s)$ and to attenuate fluctuations of the dc capacitor voltage. For this purpose, two types of regulator will be considered and compared. The first is based on an integral-proportional controller. The second is based on identification of the disturbance and regulation using the placement RST controller.

A. Proportional-Integral controller

The used integral-proportional controller IP has the advantage of not introducing a supplementary zero in the closed loop transfer function. To attenuate the external ripple dE, a first-order low-pass filter is used (fig. 2).

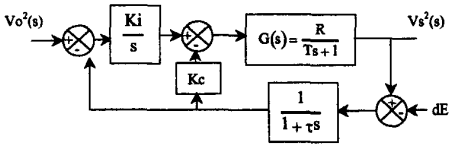


Fig. 2. DC voltage control using IP regulator

The closed loop model is:

$$V_S^2(s) = \frac{RKi(1+\tau s)}{T\tau s^3 + (T+\tau)s^2 + (1+RKc)s + RKi}V_0^2(s) + \frac{R(Ki+Kcs)}{T\tau s^3 + (T+\tau)s^2 + (1+RKc)s + RKi}dE \quad (7)$$

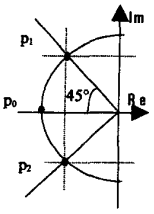
This system is third-order with two freedom degrees: Ki and Kc. The poles of the system are placed on the Butterworth circle.

$$p_0 = -\omega_0$$

$$p_1 = \omega_0 e^{j\frac{3\pi}{4}}$$

$$p_2 = \omega_0 e^{-j\frac{3\pi}{4}}$$

$$with\ \omega_O = -\frac{T+\tau}{T\tau\left(1+\sqrt{2}\right)}$$



The regulator parameters *Ki* and *Kc* are calculated to verify the following equality:

$$s^3 + \frac{T+\tau}{T\tau}s^2 + \frac{1+RKc}{T\tau}s + \frac{RKi}{T\tau} = (s-p_0)(s-p_1)(s-p_2)$$

$$Ki = \frac{(T+\tau)^3}{T^2\tau^2\left(1+\sqrt{2}\right)^3 R} \text{ et } Kc = \frac{1}{R}\left(\frac{(T+\tau)^2}{T\tau\left(1+\sqrt{2}\right)} - 1\right)$$

The choice of the low-pass filter time constant τ has an influence on the input current waveform, and on the regulator dynamics. The better the quality of input current is, the slower the regulator dynamic is. The low-pass filter time constant τ is chosen so as to attenuate the disturbance *dE* but without deteriorating regulator performance. Bad current waveform quality is characterised by a high harmonic distortion ratio (*Thd*). Thus a compromise must be found between the dynamic performances and the quality of line current. Table 1 shows the regulator performance after doubling resistive load for different cut-off frequencies of the low-pass filter *fc*.

The influence of the frequency *fc* on the performance of the IP regulator are indicated (attenuation of fluctuations, total harmonic distortion ratio (*Thd*), variation of the dc capacitor voltage for a 50% load step change (ΔV_S) and settling time (Δt)).

Table 1: IP controller performances

IP	*fc*=3.1Hz	*fc*=10Hz	*fc*=31Hz
Attenuation of regulator	-70dB	-50dB	-30dB
ΔV_S	75V	60V	40V
Settling time	0.22	0.14s	0.06s
Thd of I_{IN}	3.65	3.67	5.13

The Bode diagram showing the effect of the regulator ($H_1(s) = \frac{K_C s + Ki}{s(\tau s + 1)}$) on the dc capacitor voltage fluctuations at *fe*=100 Hz is presented in fig. 3. By decreasing the cut-off frequency *fc* of the low-pass filter, an improvement in the total harmonic distortion ratio *Thd* results. However the regulator's performance decreases (see the voltage variation ΔV_S and the settling time Δt).

The regulator parameters are chosen to obtain a better harmonic distortion ratio, i.e. with low-pass filter reducing at least 50dB the voltage fluctuations.

The regulator stability is verified by using the open loop Nichols diagram (fig. 4). The gain margin G_m is equal to 100dB and the phase margin P_m is equal to 90°.

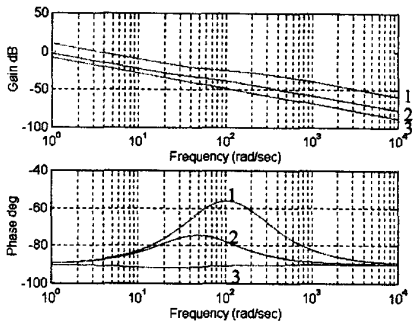


Fig. 3. IP regulator Bode diagram (1-*fc*=31Hz, 2-*fc*=10Hz, 3-*fc*=3.1Hz)

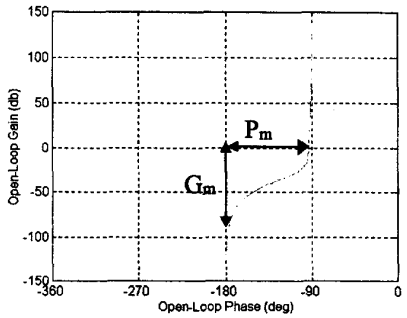


Fig. 4. Nichols diagram of the open loop (*fc*=10Hz)

A. RST controller

The regulation process (fig. 5) is based on the robust pole placement strategy, and is described by polynomials *R(s)*, *S(s)* and *T(s)*. The calculation of polynomials depends on the constraint rejecting the effect of disturbance *dE*.

First, we calculate the closed loop transfer function:

$$V_S^2(s) = \frac{B(s)T(s)}{A(s)S(s)+B(s)R(s)}V_0^2(s) - \frac{B(s)R(s)}{A(s)S(s)+B(s)R(s)}dE(s) \quad (8)$$

An integral effect is imposed in order to cancel the error ($V_0^2(s)$-$V_S^2(s)$) during steady state by the condition: *S(0)=0*. The polynomial *T(s)* is chosen to ensure a unit static gain: *T(s)=R(0)*.

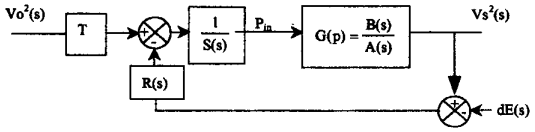


Fig. 5. DC voltage control using RST regulator

Objectives of control are translated into constraints on polynomial *R(s)* and *S(s)*. The constraint on *dE(s)* imposes a pole in the polynomial R(s) corresponding to ripple frequency f_e=100Hz. Therefore, *R(s)* can be split up into two parts:

$$R(s)=R_C(s)R_F(s) \text{ with } R_C(s)=s^2+(2\pi f_e)^2$$

$R_C(s)$ and $R_F(s)$ are called the constraint polynomial and the free polynomial respectively. $R_F(s)$ and *S(s)* are computed by solving the following Bezout equation:

$$D(s)=A(s)S(s)+B(s)R(s) \qquad (9)$$

where, *D(s)* is the closed loop characteristic polynomial.

The poles of *D(s)* are chosen with the following objectives in mind: robustness, performance and stability. The system is fifth order, so as to have a strictly proper regulator (deg(*S*)=deg(*R*)+1). Therefore, we impose:

$$D(s)=(s-s_0)^5$$

The robust poles is placed at: $s_0=-\pi f_e$ to obtain specified gain and phase margins.

The Bode diagram of the regulator ($H_2(s)=\frac{R(s)}{S(s)}$) shows its effect on the frequency f_e of the disturbance *dE*. The voltage ripple is attenuated by 50dB (fig. 7). The stability of the system is checked by a Nichols diagram which gives a gain margin G_m of 10dB and a phase margin P_m of 45° (fig. 10).

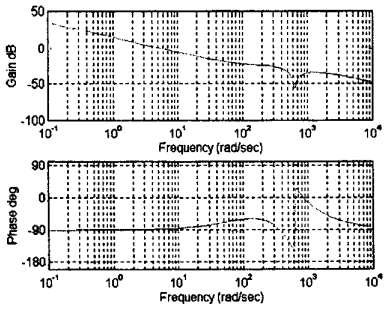


Fig. 6. RST regulator Bode diagram

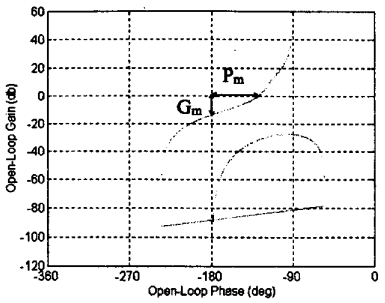


Fig. 7. Nichols diagram of the open loop

With these parameters, the *Thd* of the input current is equal to 2.7% less than 93.8% without PFC, the output voltage variation ΔV_S is equal to 40V and the time response Δt is equal to 0.05s.

B. Comparison of IP & RST controllers

Comparison tests were obtained by simulation using MatLab-Simulink software. The current loop used is a classic hysteresis control. To compare for the same conditions, the low-pass filter of the IP controller is tuned to realise the same ripple attenuation. Throughout the test, the resistive load was switching between 80Ω and 40Ω, the output reference voltage was maintained at V_{ref}=400V, the inductance *L* and the dc capacitor value *C* were equal to 1mH and to 1000µF respectively. Results are summarised in table 2.

Table 2: Performances of IP and RST controllers

	IP		RST
C	1000µF	3000µF	1000µF
ΔV_S	60V	40V	40V
Settling time	0.2	0.14s	0.04s

Waveforms obtained for output dc capacitor voltage ($V_S(t)$), and input line current ($I_e(t)$) during load transients are shown in figs. 8-9.

The voltage drop and time response are higher with the PI controller than with the RST controller. The RST controller allows us to reduce the capacitor value for a given voltage drop. To achieve the same ΔV_S, with the IP controller as with the RST controller, the dc capacitor value *C* must be multiplied by three. However the settling time remains higher (0.14s instead of 0.2s) [6]. We can also note that for both controllers, the input current is quasi sinusoidal and in phase with the supply voltage.

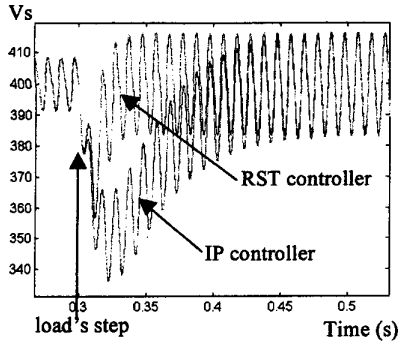


Fig. 8. DC voltage variation under load step

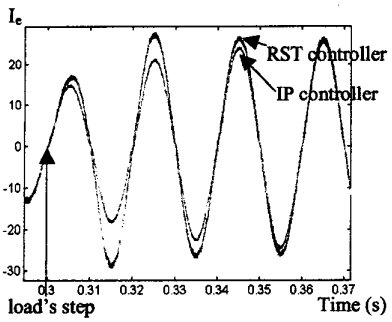


Fig. 9. Input current under load step

IV. Current loop

The current loop model can be represented as shown in fig. 10. The sensor measures the input current or current in the inductance and the control strategy drives this current to follow a sinusoidal reference.

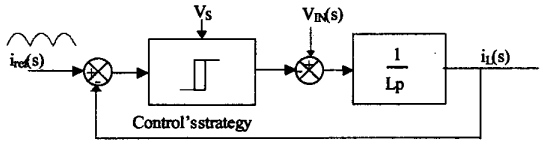


Fig. 10. Current control loop

Three principles are often used for the current control strategy:

- Maximum current control allowing fixed frequency driver and variable ripple.
- Average current-mode control obtained by comparing the error with a fixed frequency triangular signal.
- Hysteresis control involving controlled ripple band and highly variable frequency driver.

These three classical control methods have advantages and disadvantages function of their use. The hysteresis control is easy to use, but if system parameters vary, the switching frequency can change dramatically and overshoot technological limits.

The instantaneous current control has the advantage of a fast dynamic and fixed frequency, but presents a static error. Furthermore, a compensation slope is necessary to ensure its stability. For higher operating frequencies the compensation slope has not a visible effect. However, for lower frequencies, deformations of the reference current appear which results in an increased total harmonic distortion ratio.

Average current control is a simple and a stable method, which has the advantage of operating at a fixed frequency. However, this control has dynamics lower than the two other methods. Therefore, the power factor is lower.

The choice of current control method is dependent on the objectives of the application.

In our case, for testing the voltage loop, a simple hysteresis current control principle is used (fig. 13). The instantaneous switching frequency (*fsw*) with respect to the designed power level of the PFC is given by [7] :

$$fsw(t) = \frac{\left(V_e(t) - L\frac{dI_{ref}}{dt}\right)\left(L\frac{dI_{ref}}{dt} + V_S\right)}{\Delta i\, I_{refmax} L V_S} \qquad (10)$$

where, Δi is the hysteresis band (Δi=10%).

Note that the power gets higher, as the maximum frequency reduces, for a given inductor and a given hysteresis band.

V. PFC application at variable power

Functioning of the PFC at different power levels dramatically modifies quality of the line current. The inductance, the capacitor and the switching frequency are determined so as to minimise distortion of the input current and output voltage ripples. Once these parameters are fixed, the current fluctuation is constant whatever the power used. Therefore, PFC designed for a 4 kW system, for example, creates a distortion ratio, which tend to increase at lower power operation (such as the 1kW system shown in table 3).

Table 3:Evolution of *Thd* of a PFC designed for 4Kw

P_{used} (W)	P_{max}	$P_{max}/2$	$P_{max}/4$
Thd of I_{IN}	2.7	4.8	9.7

Besides, it would be tedious to have a variety of designs for different power levels. Therefore as a solution we propose to keep a lower input current distortion whatever the power used. Thus to increase PFC performances, one solution consists of adding a second parallel PFC stage to compensate the residual

power which the first PFC stage cannot absorb. Thus, the switching stress can be decreased by reducing the switching frequency of the first PFC system . To obtain a quasi-sinusoidal current, the second unit has a lower residual power and a higher switching frequency (fig. 11) [7].

The second current reference is easily obtained by finding the difference between the obtained real current and the reference of the first stage. The operation's result is that the second unit's current reference is triangular. References and obtained unfiltered input currents for every PFC system have the shapes presented in fig. 12.

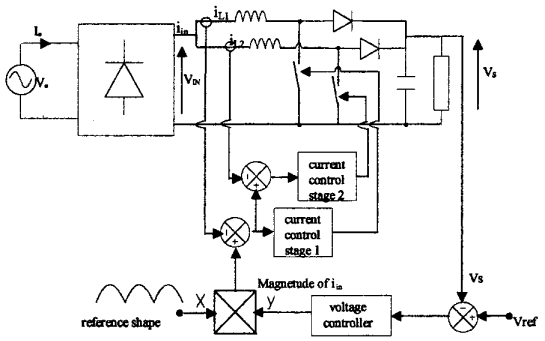


Fig. 11. Generic topology of Multi-BOOST
PFC1: P=Pmax/4=1kW, fswmax=10kHz, L1=3.5mH
PFC2: P=250W, fswmax=100kHz, L2=0.9mH

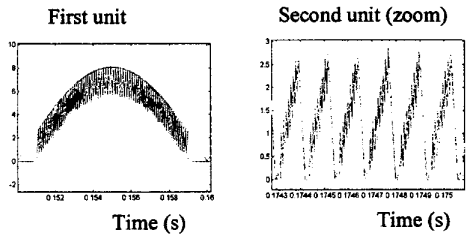


Fig. 12. Currents distribution on two PFC units

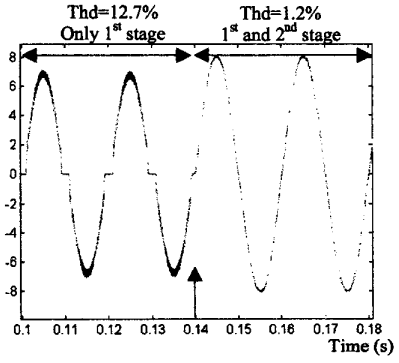


Fig. 13. Input line current

The resulting line current, initially with only the first PFC stage and then with two PFC systems operating in parallel, is presented in fig.13. A unity power factor and very low harmonic distortion along with good output voltage regulation is achieved. The total harmonic distortion ratio *Thd* of the line current decreases from 12.7% to less than 1.2.%.

VI. Conclusion

We have proposed an improvement for dynamic performances of the voltage loop of power factor correction systems. The RST controller seems more adapted to minimise the output voltage drop and restore a faster steady state. This controller also has good performances for variable power applications.

We have managed to keep the harmonic distortion ratio very low by placing, in parallel, two boost circuits operating at different power levels. This solution allows a system to operate at any applied power level with equivalent performance. A unity power factor and very low harmonic distortion along with good output voltage regulation is achieved.

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