

74HC4053; 74HCT4053

Triple 2-channel analog multiplexer/demultiplexer

Rev. 7 — 13 December 2011

Product data sheet

1. General description

The 74HC4053; 74HCT4053 is a high-speed Si-gate CMOS device and is pin compatible with the HEF4053B. It is specified in compliance with JEDEC standard no. 7A.

The 74HC4053; 74HCT4053 is triple 2-channel analog multiplexer/demultiplexer with a common enable input (\bar{E}). Each multiplexer/demultiplexer has two independent inputs/outputs (nY0 and nY1), a common input/output (nZ) and three digital select inputs (S_n). With \bar{E} LOW, one of the two switches is selected (low-impedance ON-state) by S₁ to S₃. With \bar{E} HIGH, all switches are in the high-impedance OFF-state, independent of S₁ to S₃.

V_{CC} and GND are the supply voltage pins for the digital control inputs (S₀ to S₂, and \bar{E}). The V_{CC} to GND ranges are 2.0 V to 10.0 V for 74HC4053 and 4.5 V to 5.5 V for 74HCT4053. The analog inputs/outputs (nY0 to nY1, and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. V_{CC} – V_{EE} may not exceed 10.0 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

2. Features and benefits

- Wide analog input voltage range from –5 V to +5 V
- Low ON resistance:
 - ◆ 80 Ω (typical) at V_{CC} – V_{EE} = 4.5 V
 - ◆ 70 Ω (typical) at V_{CC} – V_{EE} = 6.0 V
 - ◆ 60 Ω (typical) at V_{CC} – V_{EE} = 9.0 V
- Logic level translation: to enable 5 V logic to communicate with ±5 V analog signals
- Typical ‘break before make’ built-in
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +85 °C and –40 °C to +125 °C

3. Applications

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating



4. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|-------------|-------------------|----------|--|----------|
| | Temperature range | Name | Description | Version |
| 74HC4053N | −40 °C to +125 °C | DIP16 | plastic dual in-line package; 16 leads (300 mil) | SOT38-4 |
| 74HCT4053N | | | | |
| 74HC4053D | −40 °C to +125 °C | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| 74HCT4053D | | | | |
| 74HC4053DB | −40 °C to +125 °C | SSOP16 | plastic shrink small outline package; 16 leads; body width 5.3 mm | SOT338-1 |
| 74HCT4053DB | | | | |
| 74HC4053PW | −40 °C to +125 °C | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |
| 74HCT4053PW | | | | |
| 74HC4053BQ | −40 °C to +125 °C | DHVQFN16 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm | SOT763-1 |
| 74HCT4053BQ | | | | |

5. Functional diagram

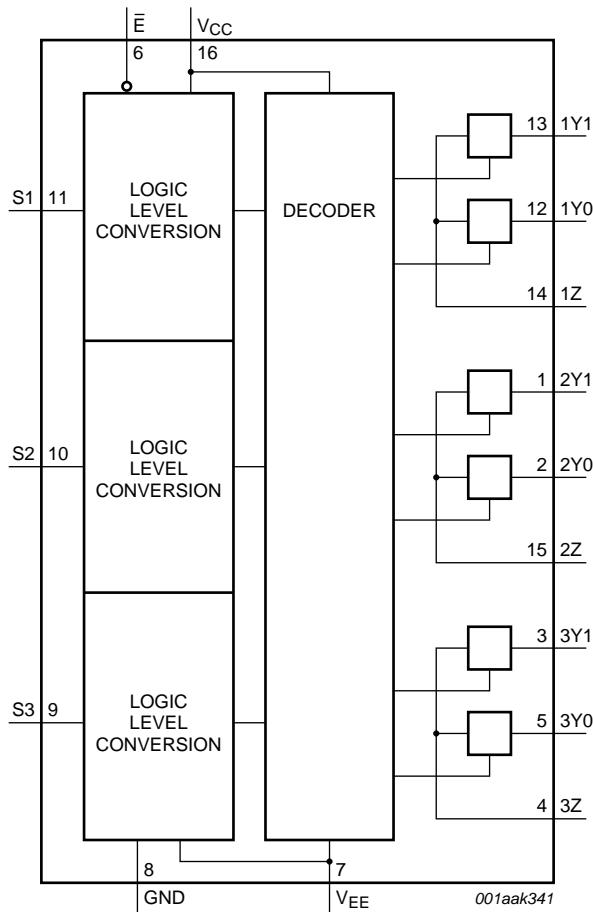


Fig 1. Functional diagram

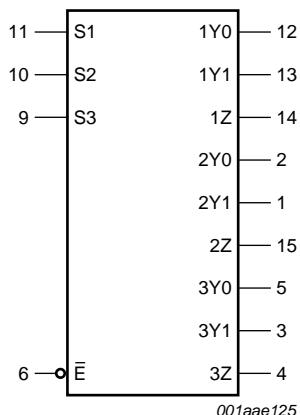


Fig 2. Logic symbol

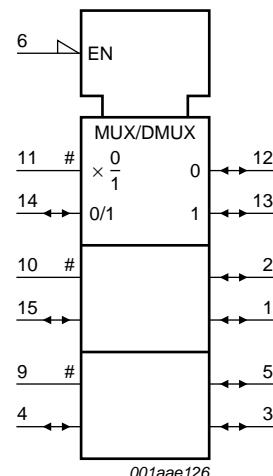
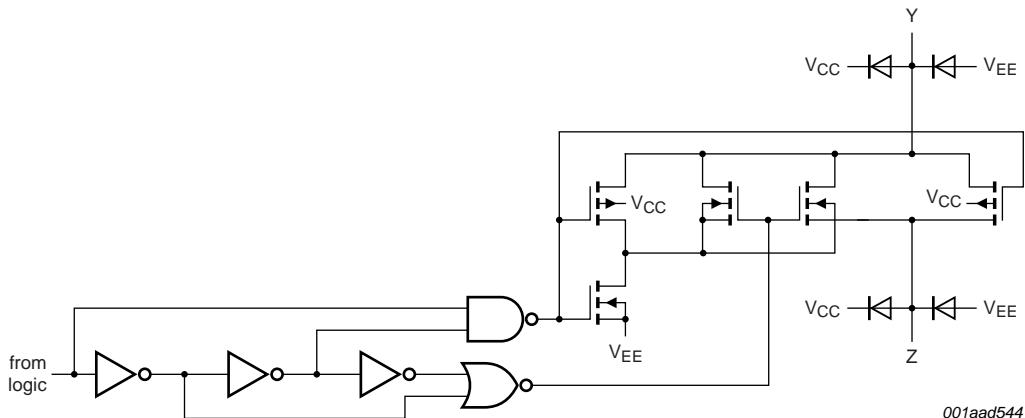


Fig 3. IEC logic symbol

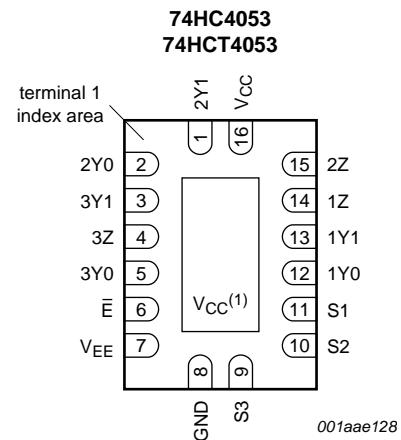
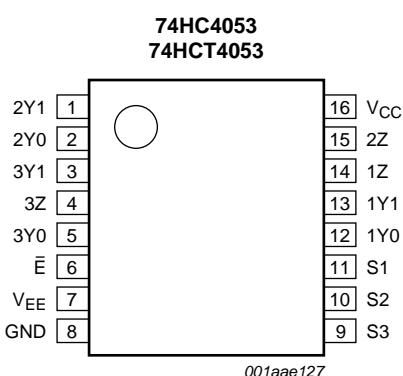


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Fig 4. Schematic diagram (one switch)

6. Pinning information

6.1 Pinning



Transparent top view

- (1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to V_{CC}.

Fig 5. Pin configuration DIP16, SO16, and (T)SSOP16

Fig 6. Pin configuration DHVQFN16

6.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|---------------|-----------|-----------------------------|
| \bar{E} | 6 | enable input (active LOW) |
| V_{EE} | 7 | supply voltage |
| GND | 8 | ground supply voltage |
| S1, S2, S3 | 11, 10, 9 | select input |
| 1Y0, 2Y0, 3Y0 | 12, 2, 5 | independent input or output |
| 1Y1, 2Y1, 3Y1 | 13, 1, 3 | independent input or output |
| 1Z, 2Z, 3Z | 14, 15, 4 | common output or input |
| V_{CC} | 16 | supply voltage |

7. Functional description

Table 3. Function table [1]

| Inputs | | Channel on |
|-----------|-------|--------------|
| \bar{E} | S_n | |
| L | L | nY0 to nZ |
| L | H | nY1 to nZ |
| H | X | switches off |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to $V_{SS} = 0$ V (ground).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|--|----------|----------|------|
| V_{CC} | supply voltage | | [1] -0.5 | +11.0 | V |
| I_{IK} | input clamping current | $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V | - | ± 20 | mA |
| I_{SK} | switch clamping current | $V_{SW} < -0.5$ V or $V_{SW} > V_{CC} + 0.5$ V | - | ± 20 | mA |
| I_{SW} | switch current | -0.5 V < V_{SW} < $V_{CC} + 0.5$ V | - | ± 25 | mA |
| I_{EE} | supply current | | - | ± 20 | mA |
| I_{CC} | supply current | | - | 50 | mA |
| I_{GND} | ground current | | - | -50 | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | DIP16 package | [2] - | 750 | mW |
| | | SO16, (T)SSOP16, and DHVQFN16 package | [3] - | 500 | mW |
| P | power dissipation | per switch | - | 100 | mW |

[1] To avoid drawing V_{CC} current out of terminal nZ, when switch current flows into terminals nYn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal nZ, no V_{CC} current will flow out of terminals nYn, and in this case there is no limit for the voltage drop across the switch, but the voltages at nYn and nZ may not exceed V_{CC} or V_{EE} .

[2] For DIP16 packages: above 70 °C the value of P_{tot} derates linearly with 12 mW/K.

- [3] For SO16 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
 For SSOP16 and TSSOP16 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
 For DHVQFN16 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

9. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | 74HC4053 | | | 74HCT4053 | | | Unit | |
|---------------------|-------------------------------------|---|-------------------|----------|----------|-----------|----------|-----|------|---|
| | | | Min | Typ | Max | Min | Typ | Max | | |
| V_{CC} | supply voltage | see Figure 7 and Figure 8 | $V_{CC} - GND$ | 2.0 | 5.0 | 10.0 | 4.5 | 5.0 | 5.5 | V |
| | | | $V_{CC} - V_{EE}$ | 2.0 | 5.0 | 10.0 | 2.0 | 5.0 | 10.0 | V |
| V_I | input voltage | GND | - | V_{CC} | GND | - | V_{CC} | V | | |
| V_{SW} | switch voltage | V_{EE} | - | V_{CC} | V_{EE} | - | V_{CC} | V | | |
| T_{amb} | ambient temperature | -40 | +25 | +125 | -40 | +25 | +125 | °C | | |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 2.0\text{ V}$ | - | - | 625 | - | - | - | ns/V | |
| | | $V_{CC} = 4.5\text{ V}$ | - | 1.67 | 139 | - | 1.67 | 139 | ns/V | |
| | | $V_{CC} = 6.0\text{ V}$ | - | - | 83 | - | - | - | ns/V | |
| | | $V_{CC} = 10.0\text{ V}$ | - | - | 31 | - | - | - | ns/V | |

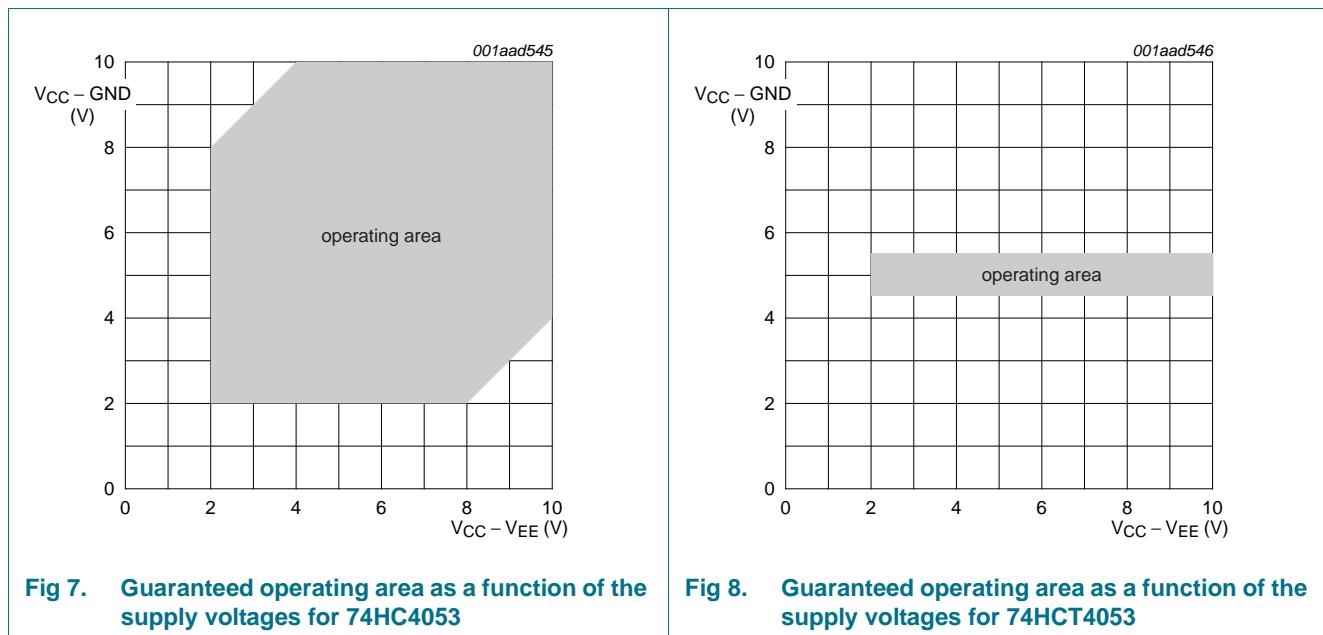


Fig 7. Guaranteed operating area as a function of the supply voltages for 74HC4053

Fig 8. Guaranteed operating area as a function of the supply voltages for 74HCT4053

10. Static characteristics

Table 6. R_{ON} resistance per switch for 74HC4053 and 74HCT4053

$V_I = V_{IH}$ or V_{IL} ; for test circuit see [Figure 9](#).

V_{IS} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.

V_{OS} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

For 74HC4053: $V_{CC} - GND$ or $V_{CC} - V_{EE} = 2.0\text{ V}, 4.5\text{ V}, 6.0\text{ V}$ and 9.0 V .

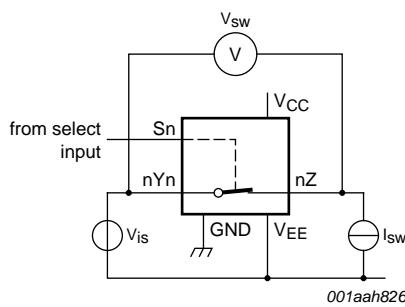
For 74HCT4053: $V_{CC} - GND = 4.5\text{ V}$ and 5.5 V , $V_{CC} - V_{EE} = 2.0\text{ V}, 4.5\text{ V}, 6.0\text{ V}$ and 9.0 V .

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|-----|-----|-----|------|
| $T_{amb} = 25\text{ }^{\circ}\text{C}$ | | | | | | |
| $R_{ON(peak)}$ | ON resistance (peak) | $V_{IS} = V_{CC}$ to V_{EE} $V_{CC} = 2.0\text{ V}; V_{EE} = 0\text{ V}; I_{SW} = 100\text{ }\mu\text{A}$ [1] - - - Ω $V_{CC} = 4.5\text{ V}; V_{EE} = 0\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$ - 100 180 Ω $V_{CC} = 6.0\text{ V}; V_{EE} = 0\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$ - 90 160 Ω $V_{CC} = 4.5\text{ V}; V_{EE} = -4.5\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$ - 70 130 Ω | | | | |
| $R_{ON(rail)}$ | ON resistance (rail) | $V_{IS} = V_{EE}$ $V_{CC} = 2.0\text{ V}; V_{EE} = 0\text{ V}; I_{SW} = 100\text{ }\mu\text{A}$ [1] - 150 - - Ω $V_{CC} = 4.5\text{ V}; V_{EE} = 0\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$ - 80 140 Ω $V_{CC} = 6.0\text{ V}; V_{EE} = 0\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$ - 70 120 Ω $V_{CC} = 4.5\text{ V}; V_{EE} = -4.5\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$ - 60 105 Ω | | | | |
| | | $V_{IS} = V_{CC}$ $V_{CC} = 2.0\text{ V}; V_{EE} = 0\text{ V}; I_{SW} = 100\text{ }\mu\text{A}$ [1] - 150 - - Ω $V_{CC} = 4.5\text{ V}; V_{EE} = 0\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$ - 90 160 Ω $V_{CC} = 6.0\text{ V}; V_{EE} = 0\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$ - 80 140 Ω $V_{CC} = 4.5\text{ V}; V_{EE} = -4.5\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$ - 65 120 Ω | | | | |
| ΔR_{ON} | ON resistance mismatch between channels | $V_{IS} = V_{CC}$ to V_{EE} $V_{CC} = 2.0\text{ V}; V_{EE} = 0\text{ V}$ [1] - - - Ω $V_{CC} = 4.5\text{ V}; V_{EE} = 0\text{ V}$ - 9 - - Ω $V_{CC} = 6.0\text{ V}; V_{EE} = 0\text{ V}$ - 8 - - Ω $V_{CC} = 4.5\text{ V}; V_{EE} = -4.5\text{ V}$ - 6 - - Ω | | | | |
| $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ | | | | | | |
| $R_{ON(peak)}$ | ON resistance (peak) | $V_{IS} = V_{CC}$ to V_{EE} $V_{CC} = 2.0\text{ V}; V_{EE} = 0\text{ V}; I_{SW} = 100\text{ }\mu\text{A}$ [1] - - - Ω $V_{CC} = 4.5\text{ V}; V_{EE} = 0\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$ - - 225 Ω $V_{CC} = 6.0\text{ V}; V_{EE} = 0\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$ - - 200 Ω $V_{CC} = 4.5\text{ V}; V_{EE} = -4.5\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$ - - 165 Ω | | | | |

Table 6. **R_{ON}** resistance per switch for 74HC4053 and 74HCT4053 ...continued $V_I = V_{IH}$ or V_{IL} ; for test circuit see [Figure 9](#). V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input. V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.For 74HC4053: $V_{CC} - GND$ or $V_{CC} - V_{EE} = 2.0\text{ V}, 4.5\text{ V}, 6.0\text{ V}$ and 9.0 V .For 74HCT4053: $V_{CC} - GND = 4.5\text{ V}$ and 5.5 V , $V_{CC} - V_{EE} = 2.0\text{ V}, 4.5\text{ V}, 6.0\text{ V}$ and 9.0 V .

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|----------------------|---|-----|-----|-----|----------|
| $R_{ON(rail)}$ | ON resistance (rail) | $V_{is} = V_{EE}$ | | | | |
| | | $V_{CC} = 2.0\text{ V}; V_{EE} = 0\text{ V}; I_{SW} = 100\text{ }\mu\text{A}$ | [1] | - | - | Ω |
| | | $V_{CC} = 4.5\text{ V}; V_{EE} = 0\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$ | - | - | 175 | Ω |
| | | $V_{CC} = 6.0\text{ V}; V_{EE} = 0\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$ | - | - | 150 | Ω |
| | | $V_{CC} = 4.5\text{ V}; V_{EE} = -4.5\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$ | - | - | 130 | Ω |
| | ON resistance (peak) | $V_{is} = V_{CC}$ | | | | |
| | | $V_{CC} = 2.0\text{ V}; V_{EE} = 0\text{ V}; I_{SW} = 100\text{ }\mu\text{A}$ | [1] | - | - | Ω |
| | | $V_{CC} = 4.5\text{ V}; V_{EE} = 0\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$ | - | - | 200 | Ω |
| | | $V_{CC} = 6.0\text{ V}; V_{EE} = 0\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$ | - | - | 175 | Ω |
| | | $V_{CC} = 4.5\text{ V}; V_{EE} = -4.5\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$ | - | - | 150 | Ω |
| | | $V_{is} = V_{CC}$ | | | | |
| $R_{ON(peak)}$ | ON resistance (peak) | $V_{is} = V_{CC}$ to V_{EE} | | | | |
| | | $V_{CC} = 2.0\text{ V}; V_{EE} = 0\text{ V}; I_{SW} = 100\text{ }\mu\text{A}$ | [1] | - | - | Ω |
| | | $V_{CC} = 4.5\text{ V}; V_{EE} = 0\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$ | - | - | 270 | Ω |
| | | $V_{CC} = 6.0\text{ V}; V_{EE} = 0\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$ | - | - | 240 | Ω |
| | | $V_{CC} = 4.5\text{ V}; V_{EE} = -4.5\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$ | - | - | 195 | Ω |
| | ON resistance (rail) | $V_{is} = V_{EE}$ | | | | |
| | | $V_{CC} = 2.0\text{ V}; V_{EE} = 0\text{ V}; I_{SW} = 100\text{ }\mu\text{A}$ | [1] | - | - | Ω |
| | | $V_{CC} = 4.5\text{ V}; V_{EE} = 0\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$ | - | - | 210 | Ω |
| | | $V_{CC} = 6.0\text{ V}; V_{EE} = 0\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$ | - | - | 180 | Ω |
| | | $V_{CC} = 4.5\text{ V}; V_{EE} = -4.5\text{ V}; I_{SW} = 1000\text{ }\mu\text{A}$ | - | - | 160 | Ω |
| | | $V_{is} = V_{CC}$ | | | | |

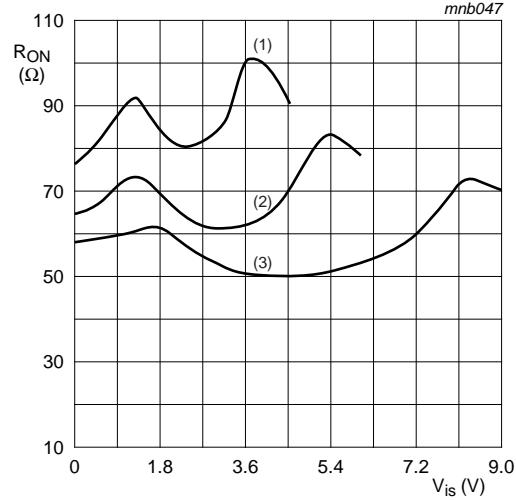
[1] When supply voltages ($V_{CC} - V_{EE}$) near 2.0 V the analog switch ON resistance becomes extremely non-linear. When using a supply of 2 V, it is recommended to use these devices only for transmitting digital signals.



$V_{is} = 0 \text{ V to } (V_{CC} - V_{EE})$.

$$R_{ON} = \frac{V_{sw}}{I_{sw}}$$

Fig 9. Test circuit for measuring R_{ON}



$V_{is} = 0 \text{ V to } (V_{CC} - V_{EE})$.

- (1) $V_{CC} = 4.5 \text{ V}$
- (2) $V_{CC} = 6 \text{ V}$
- (3) $V_{CC} = 9 \text{ V}$

Fig 10. Typical R_{ON} as a function of input voltage V_{is}

Table 7. Static characteristics for 74HC4053

Voltages are referenced to GND (ground = 0 V).

V_{is} is the input voltage at pins nYn or nZ , whichever is assigned as an input.

V_{os} is the output voltage at pins nZ or nYn , whichever is assigned as an output.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|---------------------------|---|------|-----|-----------|---------------|
| T_{amb} = 25 °C | | | | | | |
| V_{IH} | HIGH-level input voltage | $V_{CC} = 2.0 \text{ V}$ | 1.5 | 1.2 | - | V |
| | | $V_{CC} = 4.5 \text{ V}$ | 3.15 | 2.4 | - | V |
| | | $V_{CC} = 6.0 \text{ V}$ | 4.2 | 3.2 | - | V |
| | | $V_{CC} = 9.0 \text{ V}$ | 6.3 | 4.7 | - | V |
| V_{IL} | LOW-level input voltage | $V_{CC} = 2.0 \text{ V}$ | - | 0.8 | 0.5 | V |
| | | $V_{CC} = 4.5 \text{ V}$ | - | 2.1 | 1.35 | V |
| | | $V_{CC} = 6.0 \text{ V}$ | - | 2.8 | 1.8 | V |
| | | $V_{CC} = 9.0 \text{ V}$ | - | 4.3 | 2.7 | V |
| I_I | input leakage current | $V_{EE} = 0 \text{ V}; V_I = V_{CC} \text{ or } \text{GND}$ | | | | |
| | | $V_{CC} = 6.0 \text{ V}$ | - | - | ± 0.1 | μA |
| | | $V_{CC} = 10.0 \text{ V}$ | - | - | ± 0.2 | μA |
| $I_{S(OFF)}$ | OFF-state leakage current | $V_{CC} = 10.0 \text{ V}; V_{EE} = 0 \text{ V}; V_I = V_{IH} \text{ or } V_{IL}; V_{sw} = V_{CC} - V_{EE}; \text{ see Figure 11}$ | | | | |
| | | per channel | - | - | ± 0.1 | μA |
| | | all channels | - | - | ± 0.1 | μA |
| $I_{S(ON)}$ | ON-state leakage current | $V_I = V_{IH} \text{ or } V_{IL}; V_{sw} = V_{CC} - V_{EE}; V_{CC} = 10.0 \text{ V}; V_{EE} = 0 \text{ V}; \text{ see Figure 12}$ | - | - | ± 0.1 | μA |

Table 7. Static characteristics for 74HC4053 ...continued*Voltages are referenced to GND (ground = 0 V).* *V_{is} is the input voltage at pins nYn or nZ, whichever is assigned as an input.* *V_{os} is the output voltage at pins nZ or nYn, whichever is assigned as an output.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|---------------------------|--|------|-----|-----------|---------------|
| I_{CC} | supply current | $V_{EE} = 0 \text{ V}; V_I = V_{CC} \text{ or } \text{GND}; V_{is} = V_{EE} \text{ or } V_{CC};$ $V_{os} = V_{CC} \text{ or } V_{EE}$ | | | | |
| | | $V_{CC} = 6.0 \text{ V}$ | - | - | 8.0 | μA |
| | | $V_{CC} = 10.0 \text{ V}$ | - | - | 16.0 | μA |
| C_I | input capacitance | | - | 3.5 | - | pF |
| C_{sw} | switch capacitance | independent pins nYn | - | 5 | - | pF |
| | | common pins nZ | - | 8 | - | pF |
| $T_{amb} = -40^\circ\text{C to } +85^\circ\text{C}$ | | | | | | |
| V_{IH} | HIGH-level input voltage | $V_{CC} = 2.0 \text{ V}$ | 1.5 | - | - | V |
| | | $V_{CC} = 4.5 \text{ V}$ | 3.15 | - | - | V |
| | | $V_{CC} = 6.0 \text{ V}$ | 4.2 | - | - | V |
| | | $V_{CC} = 9.0 \text{ V}$ | 6.3 | - | - | V |
| V_{IL} | LOW-level input voltage | $V_{CC} = 2.0 \text{ V}$ | - | - | 0.5 | V |
| | | $V_{CC} = 4.5 \text{ V}$ | - | - | 1.35 | V |
| | | $V_{CC} = 6.0 \text{ V}$ | - | - | 1.8 | V |
| | | $V_{CC} = 9.0 \text{ V}$ | - | - | 2.7 | V |
| I_I | input leakage current | $V_{EE} = 0 \text{ V}; V_I = V_{CC} \text{ or } \text{GND}$ | | | | |
| | | $V_{CC} = 6.0 \text{ V}$ | - | - | ± 1.0 | μA |
| | | $V_{CC} = 10.0 \text{ V}$ | - | - | ± 2.0 | μA |
| $I_{S(OFF)}$ | OFF-state leakage current | $V_{CC} = 10.0 \text{ V}; V_{EE} = 0 \text{ V}; V_I = V_{IH} \text{ or } V_{IL};$ $ V_{SW} = V_{CC} - V_{EE};$ see Figure 11 | | | | |
| | | per channel | - | - | ± 1.0 | μA |
| | | all channels | - | - | ± 1.0 | μA |
| $I_{S(ON)}$ | ON-state leakage current | $V_I = V_{IH} \text{ or } V_{IL}; V_{SW} = V_{CC} - V_{EE};$ $V_{CC} = 10.0 \text{ V}; V_{EE} = 0 \text{ V};$ see Figure 12 | - | - | ± 1.0 | μA |
| I_{CC} | supply current | $V_{EE} = 0 \text{ V}; V_I = V_{CC} \text{ or } \text{GND}; V_{is} = V_{EE} \text{ or } V_{CC};$ $V_{os} = V_{CC} \text{ or } V_{EE}$ | | | | |
| | | $V_{CC} = 6.0 \text{ V}$ | - | - | 80.0 | μA |
| | | $V_{CC} = 10.0 \text{ V}$ | - | - | 160.0 | μA |
| $T_{amb} = -40^\circ\text{C to } +125^\circ\text{C}$ | | | | | | |
| V_{IH} | HIGH-level input voltage | $V_{CC} = 2.0 \text{ V}$ | 1.5 | - | - | V |
| | | $V_{CC} = 4.5 \text{ V}$ | 3.15 | - | - | V |
| | | $V_{CC} = 6.0 \text{ V}$ | 4.2 | - | - | V |
| | | $V_{CC} = 9.0 \text{ V}$ | 6.3 | - | - | V |
| V_{IL} | LOW-level input voltage | $V_{CC} = 2.0 \text{ V}$ | - | - | 0.5 | V |
| | | $V_{CC} = 4.5 \text{ V}$ | - | - | 1.35 | V |
| | | $V_{CC} = 6.0 \text{ V}$ | - | - | 1.8 | V |
| | | $V_{CC} = 9.0 \text{ V}$ | - | - | 2.7 | V |

Table 7. Static characteristics for 74HC4053 ...continued

Voltages are referenced to GND (ground = 0 V).

V_{is} is the input voltage at pins nYn or nZ, whichever is assigned as an input.

V_{os} is the output voltage at pins nZ or nYn, whichever is assigned as an output.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------|---------------------------|---|-----|-----|-----------|---------------|
| I_I | input leakage current | $V_{EE} = 0 \text{ V}; V_I = V_{CC} \text{ or } \text{GND}$ | | | | |
| | | $V_{CC} = 6.0 \text{ V}$ | - | - | ± 1.0 | μA |
| | | $V_{CC} = 10.0 \text{ V}$ | - | - | ± 2.0 | μA |
| $I_{S(OFF)}$ | OFF-state leakage current | $V_{CC} = 10.0 \text{ V}; V_{EE} = 0 \text{ V}; V_I = V_{IH} \text{ or } V_{IL}; V_{SW} = V_{CC} - V_{EE}; \text{ see } \text{Figure 11}$ | | | | |
| | | per channel | - | - | ± 1.0 | μA |
| | | all channels | - | - | ± 1.0 | μA |
| $I_{S(ON)}$ | ON-state leakage current | $V_I = V_{IH} \text{ or } V_{IL}; V_{SW} = V_{CC} - V_{EE}; V_{CC} = 10.0 \text{ V}; V_{EE} = 0 \text{ V}; \text{ see } \text{Figure 12}$ | - | - | ± 1.0 | μA |
| I_{CC} | supply current | $V_{EE} = 0 \text{ V}; V_I = V_{CC} \text{ or } \text{GND}; V_{is} = V_{EE} \text{ or } V_{CC}; V_{os} = V_{CC} \text{ or } V_{EE}$ | | | | |
| | | $V_{CC} = 6.0 \text{ V}$ | - | - | 160.0 | μA |
| | | $V_{CC} = 10.0 \text{ V}$ | - | - | 320.0 | μA |

Table 8. Static characteristics for 74HCT4053

Voltages are referenced to GND (ground = 0 V).

V_{is} is the input voltage at pins nYn or nZ, whichever is assigned as an input.

V_{os} is the output voltage at pins nZ or nYn, whichever is assigned as an output.

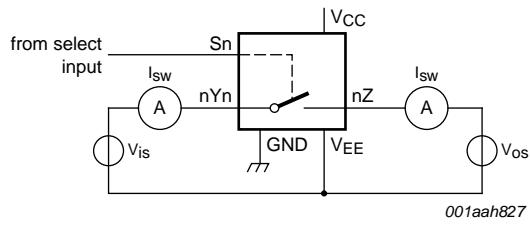
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------------|---------------------------|---|-----|-----|-----------|---------------|
| $T_{amb} = 25^\circ\text{C}$ | | | | | | |
| V_{IH} | HIGH-level input voltage | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ | 2.0 | 1.6 | - | V |
| V_{IL} | LOW-level input voltage | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ | - | 1.2 | 0.8 | V |
| I_I | input leakage current | $V_I = V_{CC} \text{ or } \text{GND}; V_{CC} = 5.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | ± 0.1 | μA |
| $I_{S(OFF)}$ | OFF-state leakage current | $V_{CC} = 10.0 \text{ V}; V_{EE} = 0 \text{ V}; V_I = V_{IH} \text{ or } V_{IL}; V_{SW} = V_{CC} - V_{EE}; \text{ see } \text{Figure 11}$ | | | | |
| | | per channel | - | - | ± 0.1 | μA |
| | | all channels | - | - | ± 0.1 | μA |
| $I_{S(ON)}$ | ON-state leakage current | $V_{CC} = 10.0 \text{ V}; V_{EE} = 0 \text{ V}; V_I = V_{IH} \text{ or } V_{IL}; V_{SW} = V_{CC} - V_{EE}; \text{ see } \text{Figure 12}$ | - | - | ± 0.1 | μA |
| I_{CC} | supply current | $V_I = V_{CC} \text{ or } \text{GND}; V_{is} = V_{EE} \text{ or } V_{CC}; V_{os} = V_{CC} \text{ or } V_{EE}$ | | | | |
| | | $V_{CC} = 5.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 8.0 | μA |
| | | $V_{CC} = 5.0 \text{ V}; V_{EE} = -5.0 \text{ V}$ | - | - | 16.0 | μA |
| ΔI_{CC} | additional supply current | per input; $V_I = V_{CC} - 2.1 \text{ V}$; other inputs at V_{CC} or GND ; $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | 50 | 180 | μA |
| C_I | input capacitance | | - | 3.5 | - | pF |
| C_{sw} | switch capacitance | independent pins nYn | - | 5 | - | pF |
| | | common pins nZ | - | 8 | - | pF |

Table 8. Static characteristics for 74HCT4053 ...continued

Voltages are referenced to GND (ground = 0 V).

 V_{is} is the input voltage at pins nY_n or nZ , whichever is assigned as an input. V_{os} is the output voltage at pins nZ or nY_n , whichever is assigned as an output.

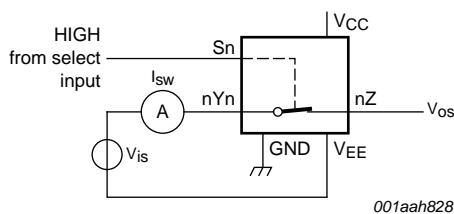
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|---------------------------|---|-----|-----|-----------|---------------|
| $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ | | | | | | |
| V_{IH} | HIGH-level input voltage | $V_{CC} = 4.5\text{ V}$ to 5.5 V | 2.0 | - | - | V |
| V_{IL} | LOW-level input voltage | $V_{CC} = 4.5\text{ V}$ to 5.5 V | - | - | 0.8 | V |
| I_I | input leakage current | $V_I = V_{CC}$ or GND; $V_{CC} = 5.5\text{ V}$; $V_{EE} = 0\text{ V}$ | - | - | ± 1.0 | μA |
| $I_{S(OFF)}$ | OFF-state leakage current | $V_{CC} = 10.0\text{ V}$; $V_{EE} = 0\text{ V}$; $V_I = V_{IH}$ or V_{IL} ; $ V_{sw} = V_{CC} - V_{EE}$; see Figure 11 | | | | |
| | | per channel | - | - | ± 1.0 | μA |
| | | all channels | - | - | ± 1.0 | μA |
| $I_{S(ON)}$ | ON-state leakage current | $V_{CC} = 10.0\text{ V}$; $V_{EE} = 0\text{ V}$; $V_I = V_{IH}$ or V_{IL} ; $ V_{sw} = V_{CC} - V_{EE}$; see Figure 12 | - | - | ± 1.0 | μA |
| I_{CC} | supply current | $V_I = V_{CC}$ or GND; $V_{is} = V_{EE}$ or V_{CC} ; $V_{os} = V_{CC}$ or V_{EE} | | | | |
| | | $V_{CC} = 5.5\text{ V}$; $V_{EE} = 0\text{ V}$ | - | - | 80.0 | μA |
| | | $V_{CC} = 5.0\text{ V}$; $V_{EE} = -5.0\text{ V}$ | - | - | 160.0 | μA |
| ΔI_{CC} | additional supply current | per input; $V_I = V_{CC} - 2.1\text{ V}$; other inputs at V_{CC} or GND; $V_{CC} = 4.5\text{ V}$ to 5.5 V ; $V_{EE} = 0\text{ V}$ | - | - | 225 | μA |
| $T_{amb} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ | | | | | | |
| V_{IH} | HIGH-level input voltage | $V_{CC} = 4.5\text{ V}$ to 5.5 V | 2.0 | - | - | V |
| V_{IL} | LOW-level input voltage | $V_{CC} = 4.5\text{ V}$ to 5.5 V | - | - | 0.8 | V |
| I_I | input leakage current | $V_I = V_{CC}$ or GND; $V_{CC} = 5.5\text{ V}$; $V_{EE} = 0\text{ V}$ | - | - | ± 1.0 | μA |
| $I_{S(OFF)}$ | OFF-state leakage current | $V_{CC} = 10.0\text{ V}$; $V_{EE} = 0\text{ V}$; $V_I = V_{IH}$ or V_{IL} ; $ V_{sw} = V_{CC} - V_{EE}$; see Figure 11 | | | | |
| | | per channel | - | - | ± 1.0 | μA |
| | | all channels | - | - | ± 1.0 | μA |
| $I_{S(ON)}$ | ON-state leakage current | $V_{CC} = 10.0\text{ V}$; $V_{EE} = 0\text{ V}$; $V_I = V_{IH}$ or V_{IL} ; $ V_{sw} = V_{CC} - V_{EE}$; see Figure 12 | - | - | ± 1.0 | μA |
| I_{CC} | supply current | $V_I = V_{CC}$ or GND; $V_{is} = V_{EE}$ or V_{CC} ; $V_{os} = V_{CC}$ or V_{EE} | | | | |
| | | $V_{CC} = 5.5\text{ V}$; $V_{EE} = 0\text{ V}$ | - | - | 160.0 | μA |
| | | $V_{CC} = 5.0\text{ V}$; $V_{EE} = -5.0\text{ V}$ | - | - | 320.0 | μA |
| ΔI_{CC} | additional supply current | per input; $V_I = V_{CC} - 2.1\text{ V}$; other inputs at V_{CC} or GND; $V_{CC} = 4.5\text{ V}$ to 5.5 V ; $V_{EE} = 0\text{ V}$ | - | - | 245 | μA |



$V_{is} = V_{CC}$ and $V_{os} = V_{EE}$.

$V_{is} = V_{EE}$ and $V_{os} = V_{CC}$.

Fig 11. Test circuit for measuring OFF-state current



$V_{is} = V_{CC}$ and $V_{os} = \text{open-circuit}$.

$V_{is} = V_{EE}$ and $V_{os} = \text{open-circuit}$.

Fig 12. Test circuit for measuring ON-state current

11. Dynamic characteristics

Table 9. Dynamic characteristics for 74HC4053

$GND = 0$ V; $t_r = t_f = 6$ ns; $C_L = 50$ pF; for test circuit see [Figure 15](#).

V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.

V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|-------------------|--|-----|-----|-----|------|
| T_{amb} = 25 °C | | | | | | |
| t_{pd} | propagation delay | V_{is} to V_{os} ; $R_L = \infty$ Ω; see Figure 13 | [1] | | | |
| | | $V_{CC} = 2.0$ V; $V_{EE} = 0$ V | - | 15 | 60 | ns |
| | | $V_{CC} = 4.5$ V; $V_{EE} = 0$ V | - | 5 | 12 | ns |
| | | $V_{CC} = 6.0$ V; $V_{EE} = 0$ V | - | 4 | 10 | ns |
| | | $V_{CC} = 4.5$ V; $V_{EE} = -4.5$ V | - | 4 | 8 | ns |

Table 9. Dynamic characteristics for 74HC4053 ...continued $GND = 0 \text{ V}$; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$; for test circuit see [Figure 15](#). V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input. V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|----------------------------------|---|-----|-----|-----|-----|------|
| t_{on} | turn-on time | \bar{E} to V_{os} ; $R_L = \infty \Omega$; see Figure 14 | [2] | | | | |
| | | $V_{CC} = 2.0 \text{ V}; V_{EE} = 0 \text{ V}$ | - | 60 | 220 | ns | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | 20 | 44 | ns | |
| | | $V_{CC} = 5.0 \text{ V}; V_{EE} = 0 \text{ V}; C_L = 15 \text{ pF}$ | - | 17 | - | ns | |
| | | $V_{CC} = 6.0 \text{ V}; V_{EE} = 0 \text{ V}$ | - | 16 | 37 | ns | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$ | - | 15 | 31 | ns | |
| | | S_n to V_{os} ; $R_L = \infty \Omega$; see Figure 14 | [2] | | | | |
| | | $V_{CC} = 2.0 \text{ V}; V_{EE} = 0 \text{ V}$ | - | 75 | 220 | ns | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | 25 | 44 | ns | |
| | | $V_{CC} = 5.0 \text{ V}; V_{EE} = 0 \text{ V}; C_L = 15 \text{ pF}$ | - | 21 | - | ns | |
| t_{off} | turn-off time | \bar{E} to V_{os} ; $R_L = 1 \text{ k}\Omega$; see Figure 14 | [3] | | | | |
| | | $V_{CC} = 2.0 \text{ V}; V_{EE} = 0 \text{ V}$ | - | 63 | 210 | ns | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | 21 | 42 | ns | |
| | | $V_{CC} = 5.0 \text{ V}; V_{EE} = 0 \text{ V}; C_L = 15 \text{ pF}$ | - | 18 | - | ns | |
| | | $V_{CC} = 6.0 \text{ V}; V_{EE} = 0 \text{ V}$ | - | 17 | 36 | ns | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$ | - | 15 | 29 | ns | |
| | | S_n to V_{os} ; $R_L = 1 \text{ k}\Omega$; see Figure 14 | [3] | | | | |
| | | $V_{CC} = 2.0 \text{ V}; V_{EE} = 0 \text{ V}$ | - | 60 | 210 | ns | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | 20 | 42 | ns | |
| | | $V_{CC} = 5.0 \text{ V}; V_{EE} = 0 \text{ V}; C_L = 15 \text{ pF}$ | - | 17 | - | ns | |
| C_{PD} | power dissipation capacitance | per switch; $V_I = GND$ to V_{CC} | [4] | - | 36 | - | pF |
| | | | | | | | |
| $T_{amb} = -40 \text{ }^{\circ}\text{C}$ to $+85 \text{ }^{\circ}\text{C}$ | | | | | | | |
| t_{pd} | propagation delay | V_{is} to V_{os} ; $R_L = \infty \Omega$; see Figure 13 | [1] | | | | |
| | | $V_{CC} = 2.0 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 75 | ns | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 15 | ns | |
| | | $V_{CC} = 6.0 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 13 | ns | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$ | - | - | 10 | ns | |

Table 9. Dynamic characteristics for 74HC4053 ...continued $GND = 0 \text{ V}$; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$; for test circuit see [Figure 15](#). V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input. V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|-------------------|---|-----|-----|-----|------|
| t_{on} | turn-on time | \bar{E} to V_{os} ; $R_L = \infty \Omega$; see Figure 14 | [2] | | | |
| | | $V_{CC} = 2.0 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 275 | ns |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 55 | ns |
| | | $V_{CC} = 6.0 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 47 | ns |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$ | - | - | 39 | ns |
| | turn-off time | S_n to V_{os} ; $R_L = \infty \Omega$; see Figure 14 | [2] | | | |
| | | $V_{CC} = 2.0 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 275 | ns |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 55 | ns |
| | | $V_{CC} = 6.0 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 47 | ns |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$ | - | - | 39 | ns |
| t_{off} | turn-on time | \bar{E} to V_{os} ; $R_L = 1 \text{ k}\Omega$; see Figure 14 | [3] | | | |
| | | $V_{CC} = 2.0 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 265 | ns |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 53 | ns |
| | | $V_{CC} = 6.0 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 45 | ns |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$ | - | - | 36 | ns |
| | turn-off time | S_n to V_{os} ; $R_L = 1 \text{ k}\Omega$; see Figure 14 | [3] | | | |
| | | $V_{CC} = 2.0 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 265 | ns |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 53 | ns |
| | | $V_{CC} = 6.0 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 45 | ns |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$ | - | - | 36 | ns |
| $T_{amb} = -40 \text{ }^{\circ}\text{C to } +125 \text{ }^{\circ}\text{C}$ | | | | | | |
| t_{pd} | propagation delay | V_{is} to V_{os} ; $R_L = \infty \Omega$; see Figure 13 | [1] | | | |
| | | $V_{CC} = 2.0 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 90 | ns |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 18 | ns |
| | | $V_{CC} = 6.0 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 15 | ns |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$ | - | - | 12 | ns |
| t_{on} | turn-on time | \bar{E} to V_{os} ; $R_L = \infty \Omega$; see Figure 14 | [2] | | | |
| | | $V_{CC} = 2.0 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 330 | ns |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 66 | ns |
| | | $V_{CC} = 6.0 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 56 | ns |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$ | - | - | 47 | ns |
| | turn-off time | S_n to V_{os} ; $R_L = \infty \Omega$; see Figure 14 | [2] | | | |
| | | $V_{CC} = 2.0 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 330 | ns |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 66 | ns |
| | | $V_{CC} = 6.0 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 56 | ns |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$ | - | - | 47 | ns |

Table 9. Dynamic characteristics for 74HC4053 ...continued*GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$; for test circuit see [Figure 15](#).* *V_{IS} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.* *V_{OS} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|---------------|---|-----|-----|-----|------|
| t_{off} | turn-off time | \bar{E} to V_{OS} ; $R_L = 1 \text{ k}\Omega$; see Figure 14 | [3] | | | |
| | | $V_{CC} = 2.0 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 315 | ns |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 63 | ns |
| | | $V_{CC} = 6.0 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 54 | ns |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$ | - | - | 44 | ns |
| | | S_n to V_{OS} ; $R_L = 1 \text{ k}\Omega$; see Figure 14 | [3] | | | |
| | | $V_{CC} = 2.0 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 315 | ns |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 63 | ns |
| | | $V_{CC} = 6.0 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 54 | ns |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$ | - | - | 44 | ns |

[1] t_{pd} is the same as t_{PHL} and t_{PLH} .[2] t_{on} is the same as t_{PZH} and t_{PZL} .[3] t_{off} is the same as t_{PHZ} and t_{PLZ} .[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma \{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\} \text{ where:}$$

 f_i = input frequency in MHz; f_o = output frequency in MHz;

N = number of inputs switching;

 $\Sigma \{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$ = sum of outputs; C_L = output load capacitance in pF; C_{sw} = switch capacitance in pF; V_{CC} = supply voltage in V.**Table 10. Dynamic characteristics for 74HCT4053***GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$; for test circuit see [Figure 15](#).* *V_{IS} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.* *V_{OS} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|-------------------|---|-----|-----|-----|------|
| $T_{amb} = 25^\circ\text{C}$ | | | | | | |
| t_{pd} | propagation delay | V_{IS} to V_{OS} ; $R_L = \infty \Omega$; see Figure 13 | [1] | | | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | 5 | 12 | ns |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$ | - | 4 | 8 | ns |
| t_{on} | turn-on time | \bar{E} to V_{OS} ; $R_L = 1 \text{ k}\Omega$; see Figure 14 | [2] | | | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | 27 | 48 | ns |
| | | $V_{CC} = 5.0 \text{ V}; V_{EE} = 0 \text{ V}; C_L = 15 \text{ pF}$ | - | 23 | - | ns |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$ | - | 16 | 34 | ns |
| | | S_n to V_{OS} ; $R_L = 1 \text{ k}\Omega$; see Figure 14 | [2] | | | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | 25 | 48 | ns |
| | | $V_{CC} = 5.0 \text{ V}; V_{EE} = 0 \text{ V}; C_L = 15 \text{ pF}$ | - | 21 | - | ns |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$ | - | 16 | 34 | ns |

Table 10. Dynamic characteristics for 74HCT4053 ...continued $GND = 0 \text{ V}$; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$; for test circuit see [Figure 15](#). V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input. V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|--|--|---|-----|-----|-----|------|----|
| t_{off} | turn-off time | \bar{E} to V_{os} ; $R_L = 1 \text{ k}\Omega$; see Figure 14 | [3] | | | | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | 24 | 44 | ns | |
| | | $V_{CC} = 5.0 \text{ V}; V_{EE} = 0 \text{ V}; C_L = 15 \text{ pF}$ | - | 20 | - | ns | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$ | - | 15 | 31 | ns | |
| | Sn to V_{os} ; $R_L = 1 \text{ k}\Omega$; see Figure 14 | | [3] | | | | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | 22 | 44 | ns | |
| | | $V_{CC} = 5.0 \text{ V}; V_{EE} = 0 \text{ V}; C_L = 15 \text{ pF}$ | - | 19 | - | ns | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$ | - | 15 | 31 | ns | |
| C_{PD} | power dissipation capacitance | per switch; $V_I = GND$ to $V_{CC} - 1.5 \text{ V}$ | [4] | - | 36 | - | pF |
| $T_{amb} = -40 \text{ }^{\circ}\text{C to } +85 \text{ }^{\circ}\text{C}$ | | | | | | | |
| t_{pd} | propagation delay | V_{is} to V_{os} ; $R_L = \infty \Omega$; see Figure 13 | [1] | | | | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 15 | ns | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$ | - | - | 10 | ns | |
| | turn-on time | \bar{E} to V_{os} ; $R_L = 1 \text{ k}\Omega$; see Figure 14 | [2] | | | | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 60 | ns | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$ | - | - | 43 | ns | |
| t_{on} | Sn to V_{os} ; $R_L = 1 \text{ k}\Omega$; see Figure 14 | | [2] | | | | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 60 | ns | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$ | - | - | 43 | ns | |
| | | | [2] | | | | |
| | turn-off time | V_{is} to V_{os} ; $R_L = \infty \Omega$; see Figure 13 | [3] | | | | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 55 | ns | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$ | - | - | 39 | ns | |
| | | | [3] | | | | |
| t_{pd} | propagation delay | V_{is} to V_{os} ; $R_L = \infty \Omega$; see Figure 13 | [1] | | | | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 18 | ns | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$ | - | - | 12 | ns | |
| | turn-on time | \bar{E} to V_{os} ; $R_L = 1 \text{ k}\Omega$; see Figure 14 | [2] | | | | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 72 | ns | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$ | - | - | 51 | ns | |
| t_{on} | Sn to V_{os} ; $R_L = 1 \text{ k}\Omega$; see Figure 14 | | [2] | | | | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 72 | ns | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$ | - | - | 51 | ns | |
| | turn-off time | V_{is} to V_{os} ; $R_L = \infty \Omega$; see Figure 13 | [2] | | | | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 72 | ns | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$ | - | - | 51 | ns | |
| $T_{amb} = -40 \text{ }^{\circ}\text{C to } +125 \text{ }^{\circ}\text{C}$ | | | | | | | |

Table 10. Dynamic characteristics for 74HCT4053 ...continued

$GND = 0 \text{ V}$; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$; for test circuit see [Figure 15](#).

V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.

V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|---------------|---|-----|-----|-----|------|
| t_{off} | turn-off time | \bar{E} to V_{os} ; $R_L = 1 \text{ k}\Omega$; see Figure 14 | [3] | | | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 66 | ns |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$ | - | - | 47 | ns |
| | | S_n to V_{os} ; $R_L = 1 \text{ k}\Omega$; see Figure 14 | [3] | | | |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = 0 \text{ V}$ | - | - | 66 | ns |
| | | $V_{CC} = 4.5 \text{ V}; V_{EE} = -4.5 \text{ V}$ | - | - | 47 | ns |

[1] t_{pd} is the same as t_{PHL} and t_{PLH} .

[2] t_{on} is the same as t_{PZH} and t_{PZL} .

[3] t_{off} is the same as t_{PHZ} and t_{PLZ} .

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L + C_{sw}) \times V_{CC}^2 \times f_o$$
 where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

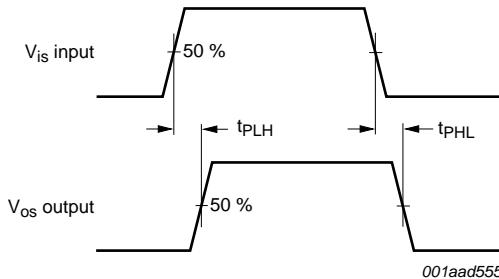
N = number of inputs switching;

$$\sum(C_L + C_{sw}) \times V_{CC}^2 \times f_o = \text{sum of outputs};$$

C_L = output load capacitance in pF;

C_{sw} = switch capacitance in pF;

V_{CC} = supply voltage in V.

**Fig 13. Input (V_{is}) to output (V_{os}) propagation delays**

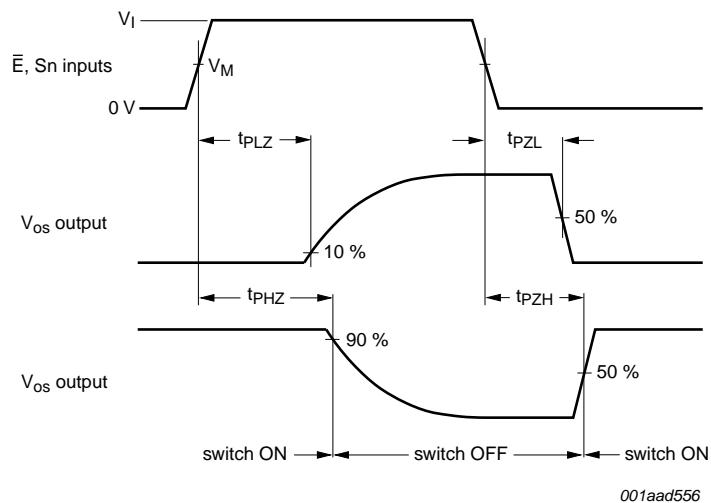
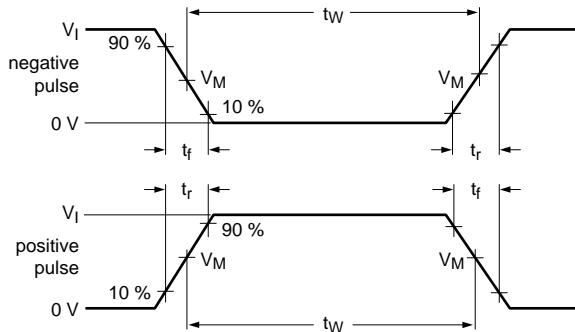


Fig 14. Turn-on and turn-off times



Definitions for test circuit; see [Table 11](#):

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

R_L = load resistance.

$S1$ = Test selection switch.

Fig 15. Test circuit for measuring AC performance

Table 11. Test data

| Test | Input | | | | Load | | S1 position |
|-------------------------------------|-------|---------------------|------------|----------------|----------------|------|-----------------|
| | V_I | V_{IS} | t_r, t_f | C _L | R _L | | |
| | | at f _{max} | other[1] | | | | |
| t _{PHL} , t _{PLH} | [2] | pulse | < 2 ns | 6 ns | 50 pF | 1 kΩ | open |
| t _{PZH} , t _{PHZ} | [2] | V _{CC} | < 2 ns | 6 ns | 50 pF | 1 kΩ | V _{EE} |
| t _{PZL} , t _{PLZ} | [2] | V _{EE} | < 2 ns | 6 ns | 50 pF | 1 kΩ | V _{CC} |

[1] t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint to t_r and t_f with 50 % duty factor.

[2] V_I values:

- a) For 74HC4053: V_I = V_{CC}
- b) For 74HCT4053: V_I = 3 V

11.1 Additional dynamic characteristics

Table 12. Additional dynamic characteristics

Recommended conditions and typical values; GND = 0 V; T_{amb} = 25 °C; C_L = 50 pF.

V_{IS} is the input voltage at pins nYn or nZ, whichever is assigned as an input.

V_{OS} is the output voltage at pins nYn or nZ, whichever is assigned as an output.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|---------------------|--------------------------|--|-----|------|-----|------|-----|
| d _{sin} | sine-wave distortion | f _i = 1 kHz; R _L = 10 kΩ; see Figure 16 | | | | | |
| | | V _{IS} = 4.0 V (p-p); V _{CC} = 2.25 V; V _{EE} = -2.25 V | - | 0.04 | - | % | |
| | | V _{IS} = 8.0 V (p-p); V _{CC} = 4.5 V; V _{EE} = -4.5 V | - | 0.02 | - | % | |
| | | f _i = 10 kHz; R _L = 10 kΩ; see Figure 16 | | | | | |
| | | V _{IS} = 4.0 V (p-p); V _{CC} = 2.25 V; V _{EE} = -2.25 V | - | 0.12 | - | % | |
| | | V _{IS} = 8.0 V (p-p); V _{CC} = 4.5 V; V _{EE} = -4.5 V | - | 0.06 | - | % | |
| α _{iso} | isolation (OFF-state) | R _L = 600 Ω; f _i = 1 MHz; see Figure 17 | | | | | |
| | | V _{CC} = 2.25 V; V _{EE} = -2.25 V | [1] | - | -50 | - | dB |
| | | V _{CC} = 4.5 V; V _{EE} = -4.5 V | [1] | - | -50 | - | dB |
| Xtalk | crosstalk | between two switches/multiplexers; R _L = 600 Ω; f _i = 1 MHz; see Figure 18 | | | | | |
| | | V _{CC} = 2.25 V; V _{EE} = -2.25 V | [1] | - | -60 | - | dB |
| | | V _{CC} = 4.5 V; V _{EE} = -4.5 V | [1] | - | -60 | - | dB |
| V _{ct} | crosstalk voltage | peak-to-peak value; between control and any switch; R _L = 600 Ω; f _i = 1 MHz; E or Sn square wave between V _{CC} and GND; t _r = t _f = 6 ns; see Figure 19 | | | | | |
| | | V _{CC} = 4.5 V; V _{EE} = 0 V | - | 110 | - | mV | |
| | | V _{CC} = 4.5 V; V _{EE} = -4.5 V | - | 220 | - | mV | |
| f _(-3dB) | -3 dB frequency response | R _L = 50 Ω; see Figure 20 | | | | | |
| | | V _{CC} = 2.25 V; V _{EE} = -2.25 V | [2] | - | 160 | - | MHz |
| | | V _{CC} = 4.5 V; V _{EE} = -4.5 V | [2] | - | 170 | - | MHz |

[1] Adjust input voltage V_{IS} to 0 dBm level (0 dBm = 1 mW into 600 Ω).

[2] Adjust input voltage V_{IS} to 0 dBm level at V_{OS} for 1 MHz (0 dBm = 1 mW into 50 Ω).

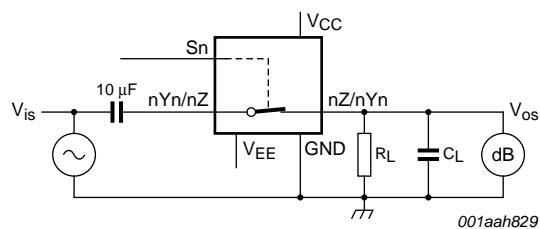
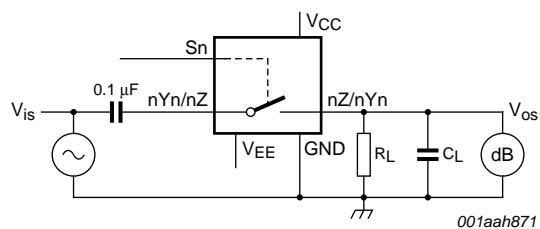
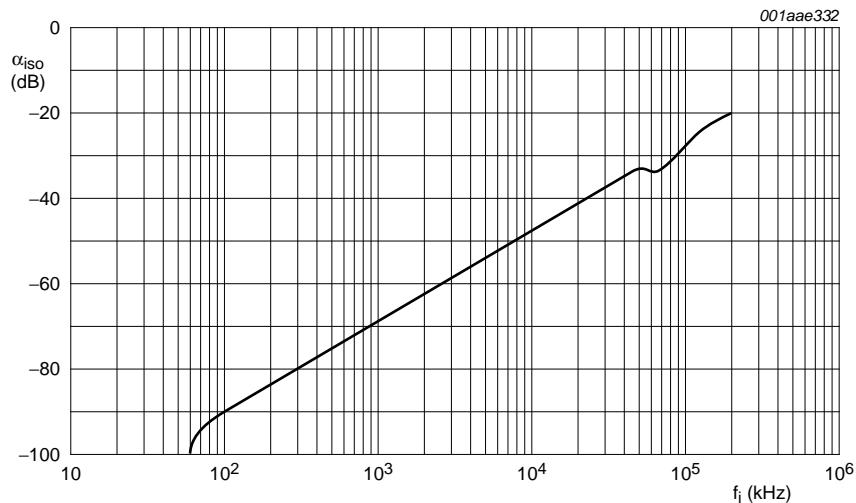


Fig 16. Test circuit for measuring sine-wave distortion



$V_{CC} = 4.5\text{ V}$; $GND = 0\text{ V}$; $V_{EE} = -4.5\text{ V}$; $R_L = 600\ \Omega$; $R_S = 1\text{ k}\Omega$.

a. Test circuit



b. Isolation (OFF-state) as a function of frequency

Fig 17. Test circuit for measuring isolation (OFF-state)

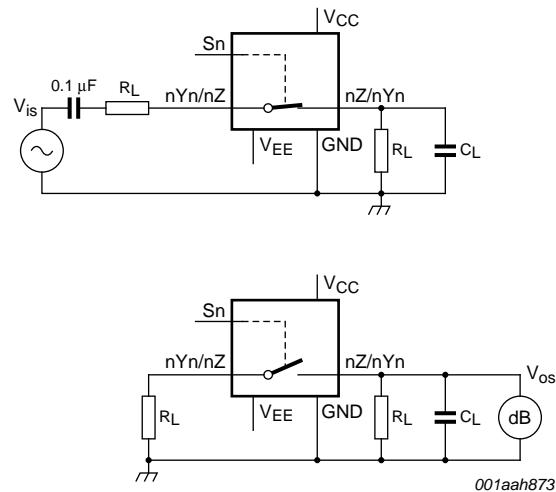


Fig 18. Test circuits for measuring crosstalk between any two switches/multiplexers

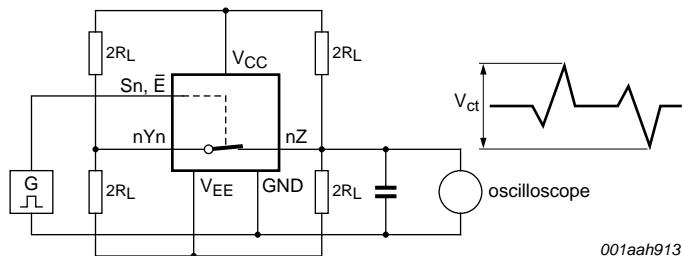
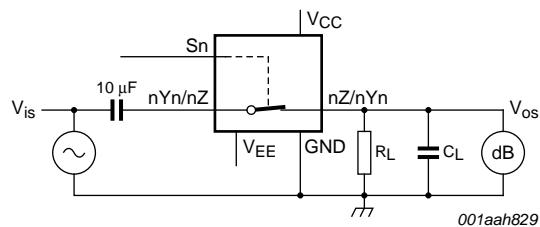
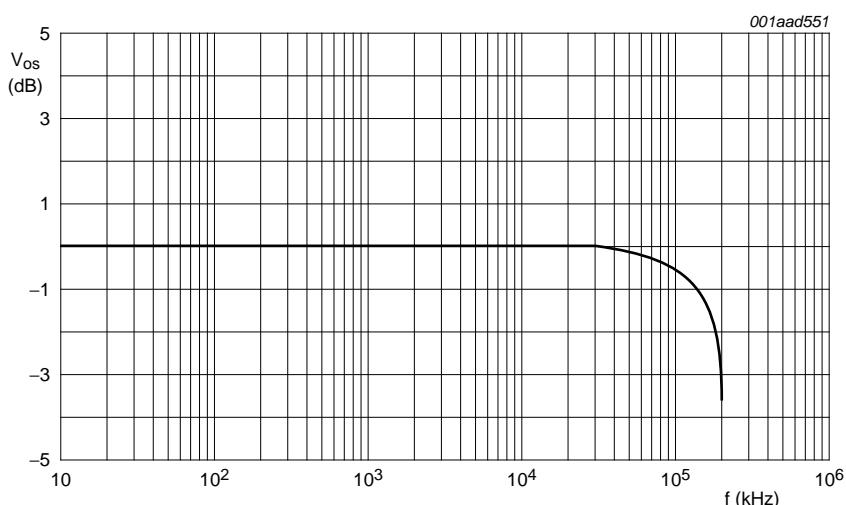


Fig 19. Test circuit for measuring crosstalk between control input and any switch



$V_{CC} = 4.5 \text{ V}$; $GND = 0 \text{ V}$; $V_{EE} = -4.5 \text{ V}$; $R_L = 50 \Omega$; $R_S = 1 \text{ k}\Omega$.

a. Test circuit



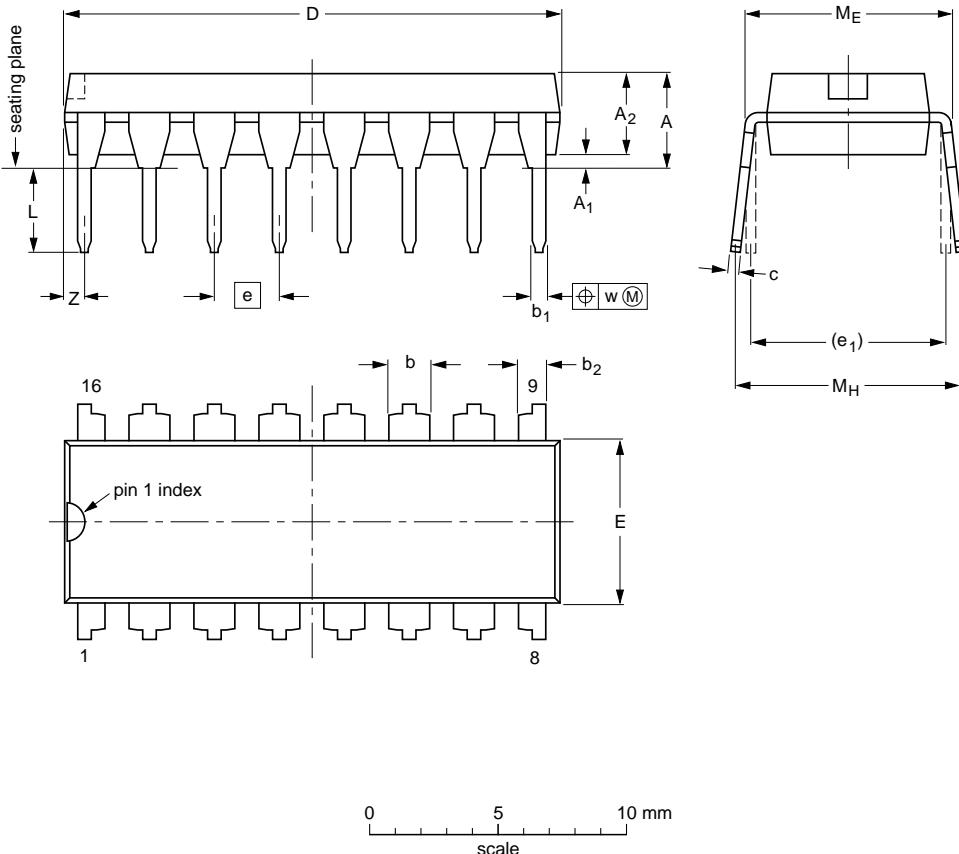
b. Typical frequency response

Fig 20. Test circuit for frequency response

12. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ min. | A ₂ max. | b | b ₁ | b ₂ | c | D ⁽¹⁾ | E ⁽¹⁾ | e | e ₁ | L | M _E | M _H | w | Z ⁽¹⁾ max. |
|--------|-----------|------------------------|------------------------|----------------|----------------|----------------|----------------|------------------|------------------|------|----------------|--------------|----------------|----------------|-------|--------------------------|
| mm | 4.2 | 0.51 | 3.2 | 1.73 1.30 | 0.53 0.38 | 1.25 0.85 | 0.36 0.23 | 19.50 18.55 | 6.48 6.20 | 2.54 | 7.62 | 3.60 3.05 | 8.25 7.80 | 10.0 8.3 | 0.254 | 0.76 |
| inches | 0.17 | 0.02 | 0.13 | 0.068 0.051 | 0.021 0.015 | 0.049 0.033 | 0.014 0.009 | 0.77 0.73 | 0.26 0.24 | 0.1 | 0.3 | 0.14 0.12 | 0.32 0.31 | 0.39 0.33 | 0.01 | 0.03 |

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|--------------------|------------|-------|-------|--|------------------------|----------------------|
| | IEC | JEDEC | JEITA | | | |
| SOT38-4 | | | | | | 95-01-14 03-02-13 |

Fig 21. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

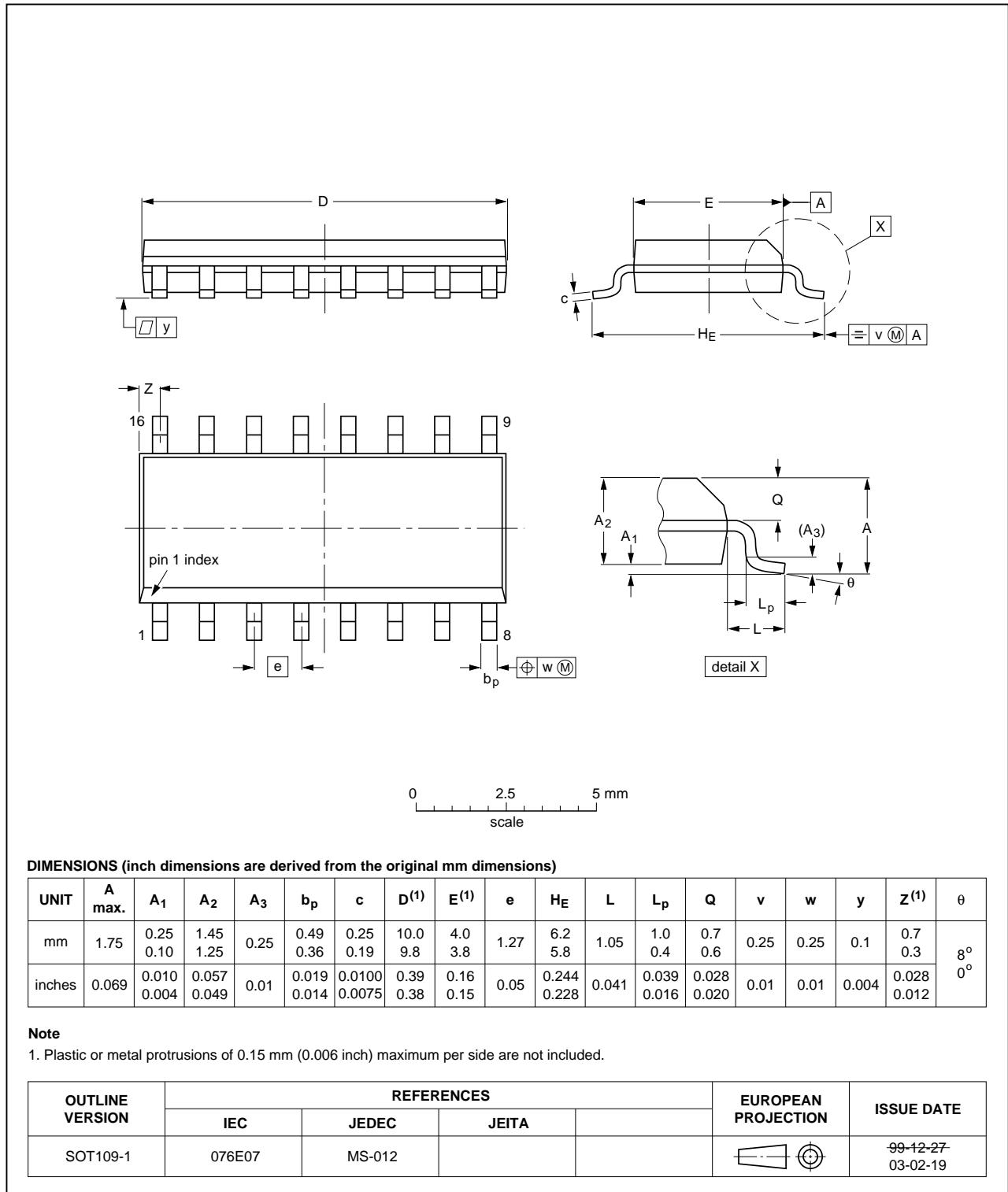


Fig 22. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

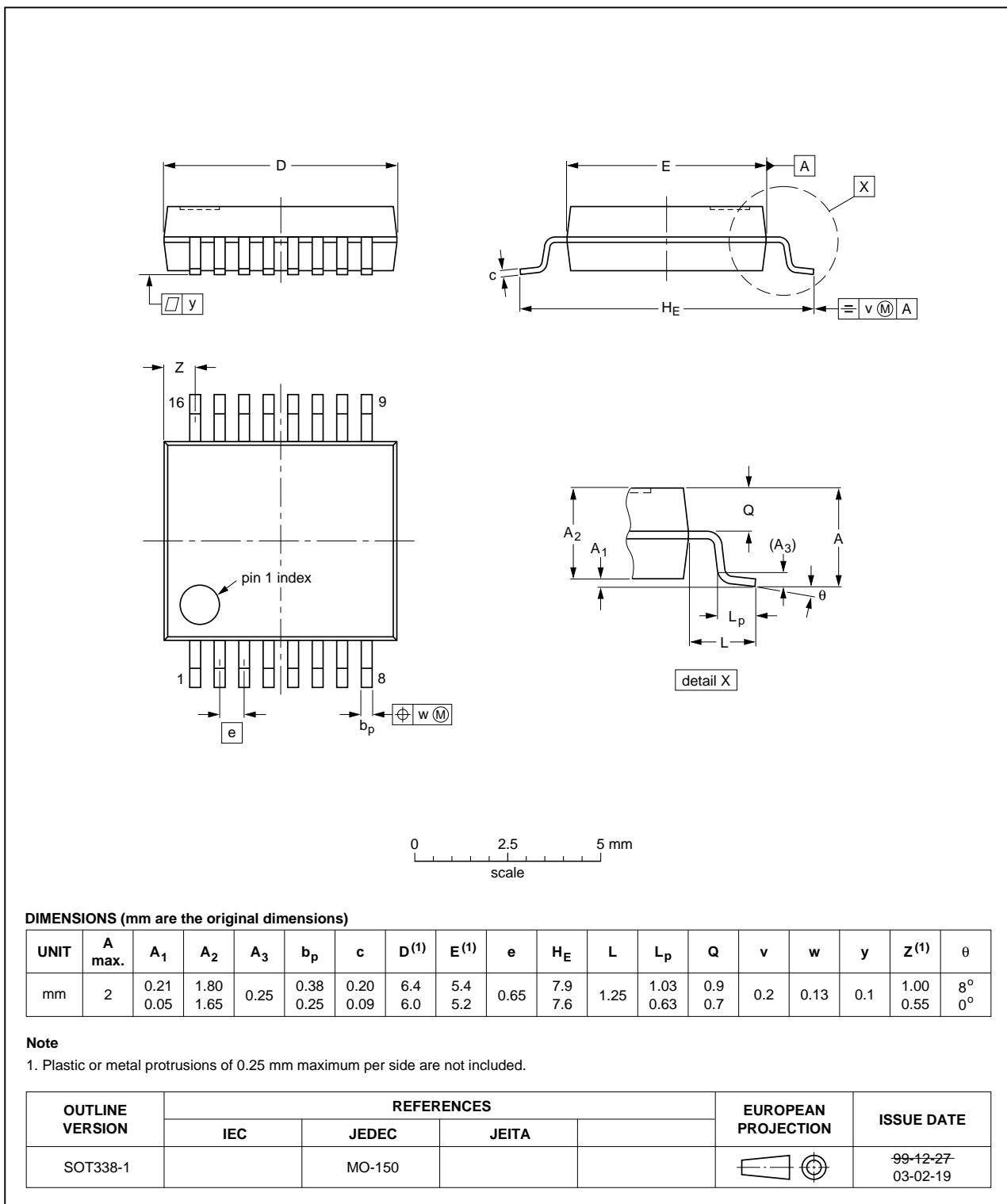


Fig 23. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

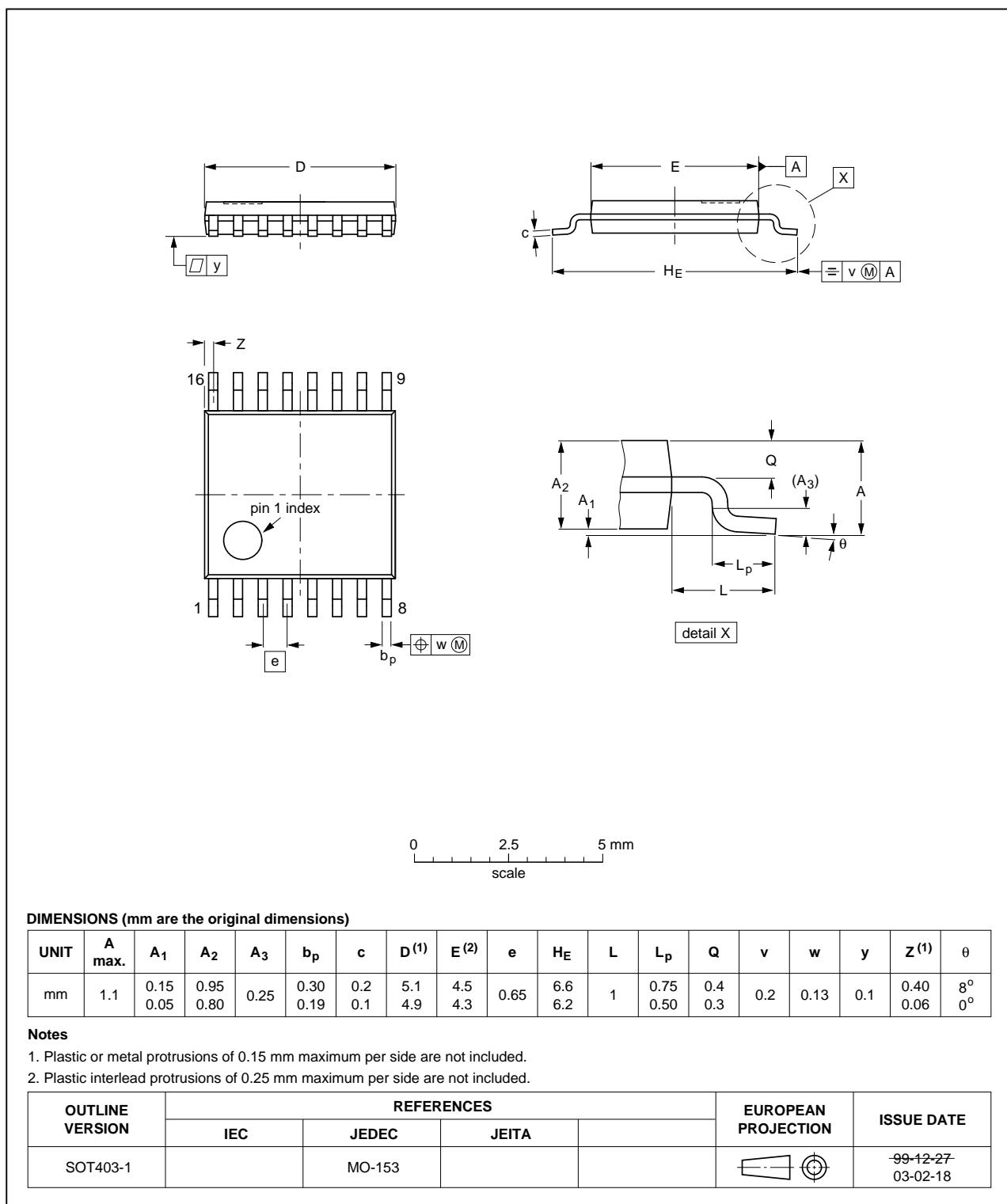


Fig 24. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

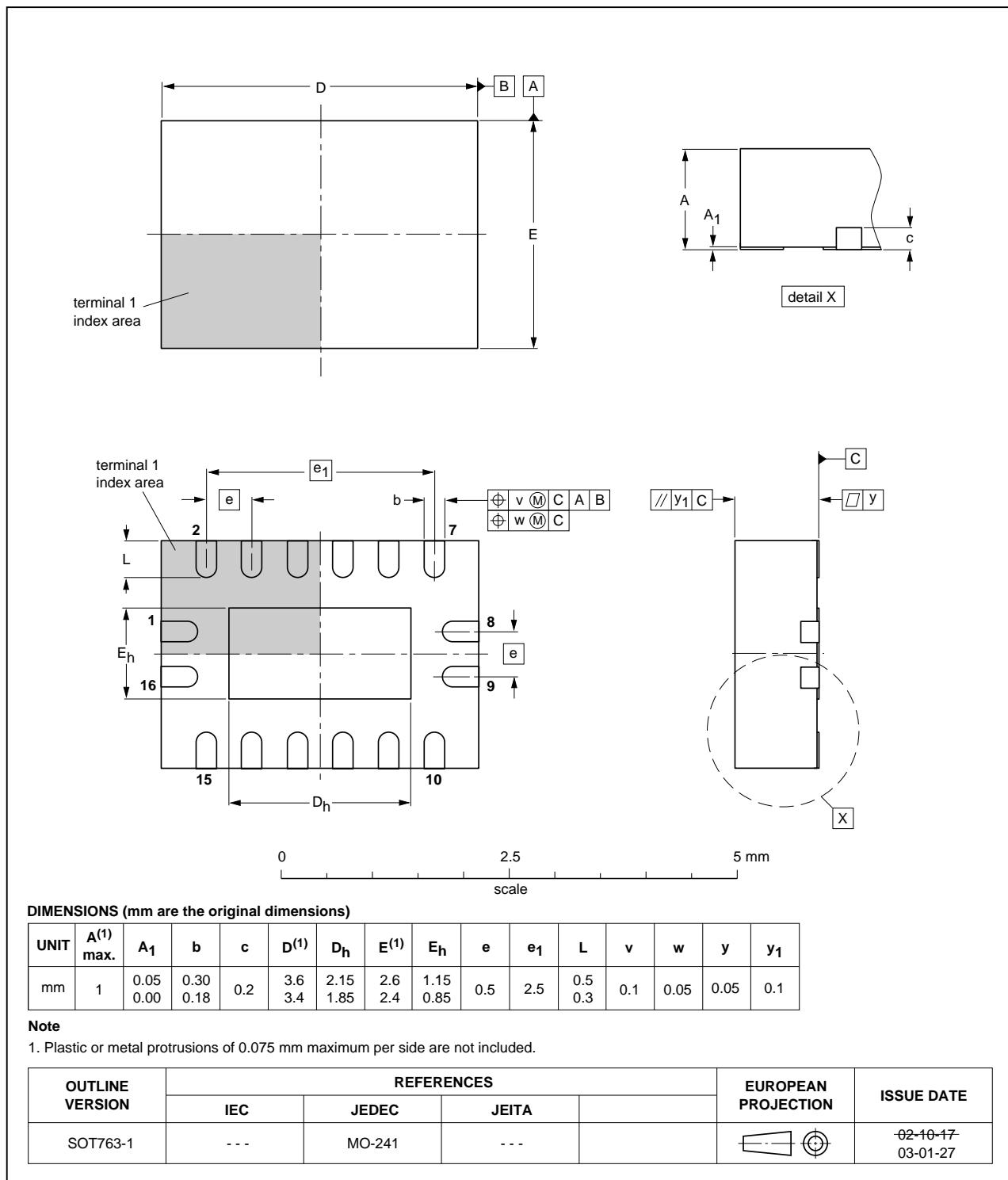


Fig 25. Package outline SOT763-1 (DHVQFN16)

13. Abbreviations

Table 13. Abbreviations

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal-Oxide Semiconductor |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |

14. Revision history

Table 14. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------------|--------------|------------------------|---------------|----------------------|
| 74HC_HCT4053 v.7 | 20111213 | Product data sheet | - | 74HC_HCT4053 v.6 |
| Modifications: | | • Legal pages updated. | | |
| 74HC_HCT4053 v.6 | 20110511 | Product data sheet | - | 74HC_HCT4053 v.5 |
| 74HC_HCT4053 v.5 | 20110118 | Product data sheet | - | 74HC_HCT4053 v.4 |
| 74HC_HCT4053 v.4 | 20060509 | Product data sheet | - | 74HC_HCT4053 v.3 |
| 74HC_HCT4053 v.3 | 20060315 | Product data sheet | - | 74HC_HCT4053_CNV v.2 |
| 74HC_HCT4053_CNV v.2 | 19901201 | Product specification | - | - |

15. Legal information

15.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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17. Contents

| | | |
|------|--|----|
| 1 | General description..... | 1 |
| 2 | Features and benefits | 1 |
| 3 | Applications | 1 |
| 4 | Ordering information..... | 2 |
| 5 | Functional diagram | 3 |
| 6 | Pinning information..... | 4 |
| 6.1 | Pinning | 4 |
| 6.2 | Pin description | 5 |
| 7 | Functional description | 5 |
| 8 | Limiting values..... | 5 |
| 9 | Recommended operating conditions..... | 6 |
| 10 | Static characteristics..... | 7 |
| 11 | Dynamic characteristics | 13 |
| 11.1 | Additional dynamic characteristics | 20 |
| 12 | Package outline | 24 |
| 13 | Abbreviations..... | 29 |
| 14 | Revision history..... | 29 |
| 15 | Legal information..... | 30 |
| 15.1 | Data sheet status | 30 |
| 15.2 | Definitions..... | 30 |
| 15.3 | Disclaimers..... | 30 |
| 15.4 | Trademarks..... | 31 |
| 16 | Contact information..... | 31 |
| 17 | Contents | 32 |

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