

CMOS OR Gates

High-Voltage Types (20-Volt Rating)

CD4071B Quad 2-Input OR Gate

CD4072B Dual 4-Input OR Gate

CD4075B Triple 3-Input OR Gate

■ CD4071B, CD4072B, and CD4075B OR gates provide the system designer with direct implementation of the positive-logic OR function and supplement the existing family of CMOS gates.

The CD4071B, CD4072B, and CD4075B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

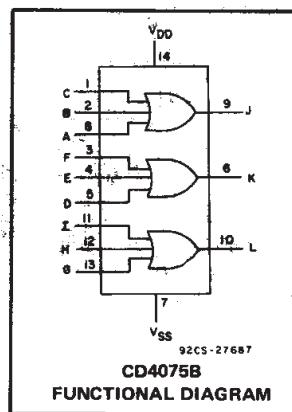
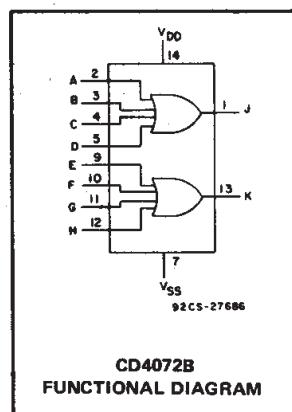
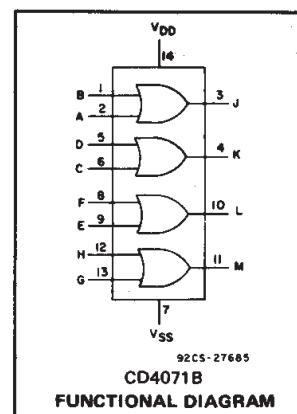
STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS	
	V_O (V)	V_{IN} (V)	V_{DD} (V)	+25				Min.	Typ.	Max.		
				-55	-40	+85	+125					
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA	
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5		
	–	0,15	15	1	1	30	30	–	0.01	1		
	–	0,20	20	5	5	150	150	–	0.02	5		
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA	
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–		
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–		
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	–	mA	
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	–		
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	–		
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	–		
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V	
	–	0,10	10	0.05				–	0	0.05		
	–	0,15	15	0.05				–	0	0.05		
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	V	
	–	0,10	10	9.95				9.95	10	–		
	–	0,15	15	14.95				14.95	15	–		
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V	
	1,9	–	10	3				–	–	3		
	1.5, 13.5	+	15	4				–	–	4		
Input High Voltage, V_{IH} Min.	4.5	–	5	3.5				3.5	–	–	V	
	9	–	10	7				7	–	–		
	13.5	–	15	11				11	–	–		
Input Current I_{IN} Max.		0,18	18	± 0.1	± 0.1	± 1	± 1	–	$\pm 10^{-5}$	± 0.1	μA	

CD4071B, CD4072B, CD4075B Types

Features:

- Medium-Speed Operation- t_{PLH} , $t_{PHL} = 60$ ns (typ.) at $V_{DD} = 10$ V
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Standardized, symmetrical output characteristics
- Noise margin (over full package temperature range)
 - 1 V at $V_{DD} = 5$ V
 - 2 V at $V_{DD} = 10$ V
 - 2.5 V at $V_{DD} = 15$ V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



CD4071B, CD4072B, CD4075B Types

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS

..... -0.5V to V_{DD} +0.5V

DC INPUT CURRENT, ANY ONE INPUT

..... $\pm 10\text{mA}$

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ 500mW

For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ Derate Linearity at $12\text{mW}/^\circ\text{C}$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$ 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55°C to +125°C

STORAGE TEMPERATURE RANGE (T_{STG}) -65°C to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ inch ($1.58 \pm 0.79\text{mm}$) from case for 10s max $+265^\circ\text{C}$

At distance $1/16 \pm 1/32$ inch ($1.58 \pm 0.79\text{mm}$) from case for 10s max $+265^\circ\text{C}$

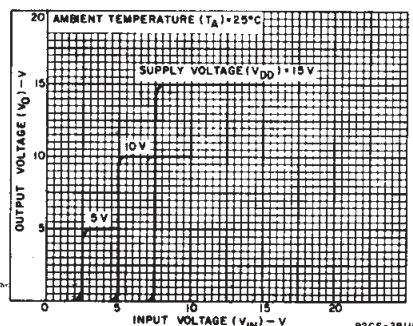


Fig. 1 — Typical voltage transfer characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20\text{ ns}$, and $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	V_{DD} VOLTS	ALL TYPES LIMITS		UNITS
			TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}		5	125	250	ns
		10	60	120	
		15	45	90	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input	—	5	7.5	pF

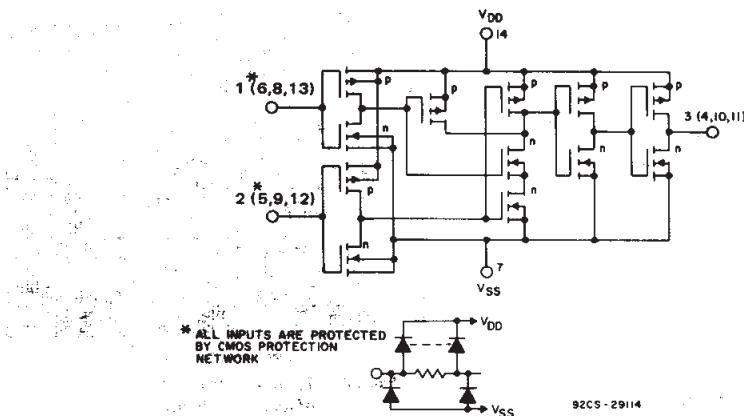


Fig. 3 — Schematic diagram for CD4071B (1 of 4 identical gates).

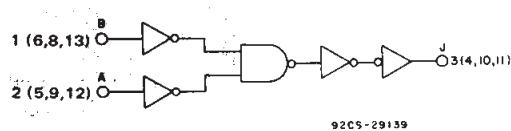


Fig. 5 — Logic diagram for CD4071B (1 of 4 identical gates).

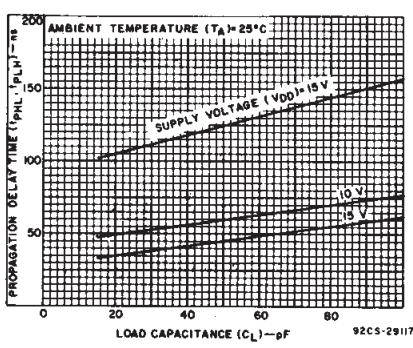


Fig. 2 — Typical propagation delay time as a function of load capacitance.

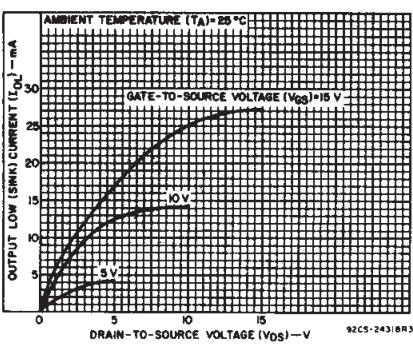


Fig. 4 — Typical output low (sink) current characteristics.

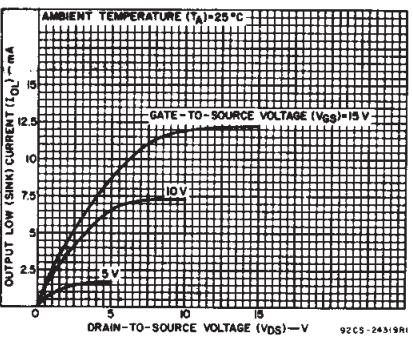


Fig. 6 — Minimum output low (sink) current characteristics.

CD4071B, CD4072B, CD4075B Types

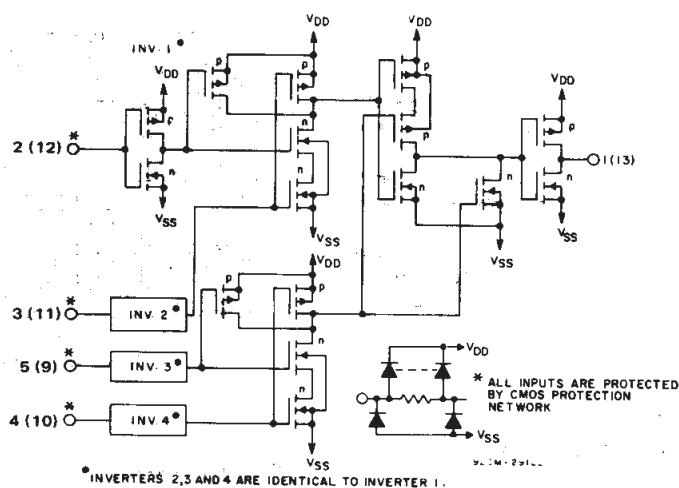


Fig. 7 – Schematic diagram for CD4072B (1 of 2 identical gates).

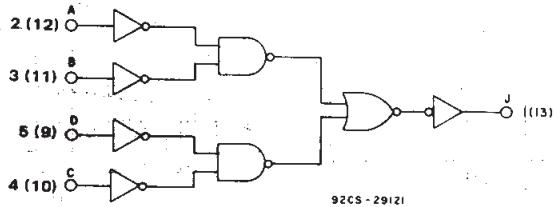


Fig. 9 – Logic diagram for CD4072B (1 of 2 identical gates).

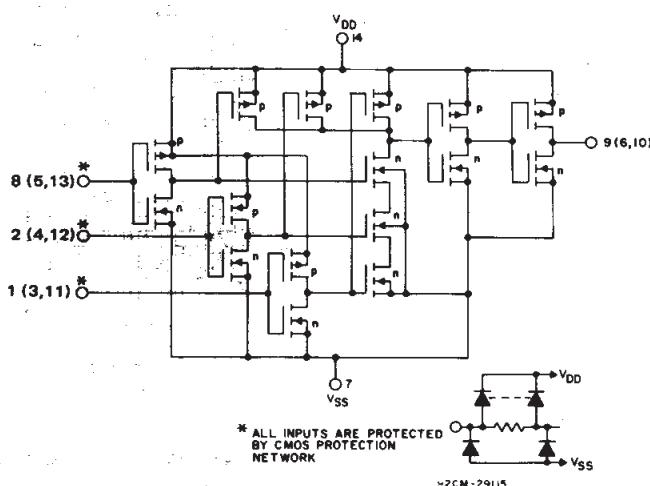


Fig. 11 – Schematic diagram for CD4075B (1 of 3 identical gates).

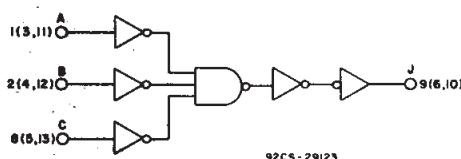


Fig. 13 – Logic diagram for CD4075B (1 of 3 identical gates).

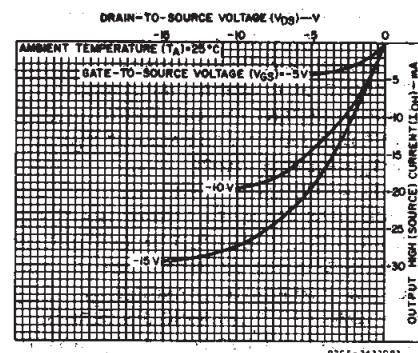


Fig. 8 – Typical output high (source) current characteristics.

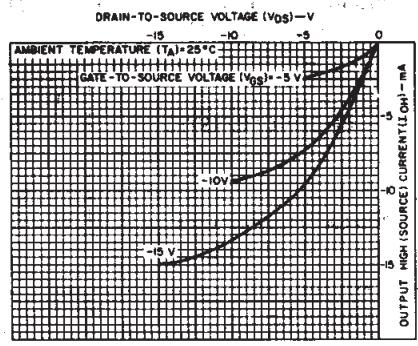


Fig. 10 – Minimum output high (source) current characteristics.

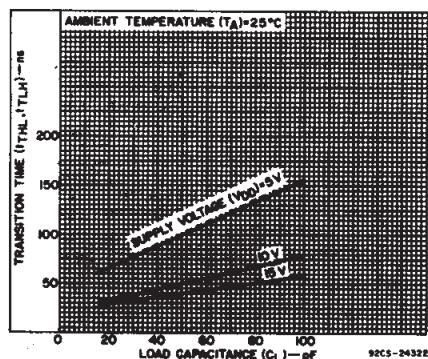


Fig. 12 – Typical transition time as a function of load capacitance.

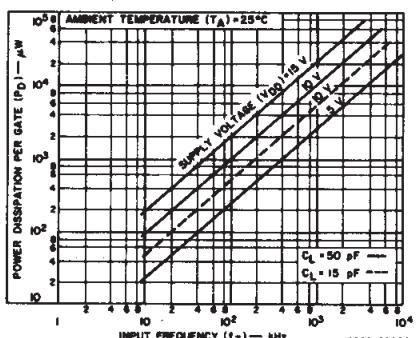


Fig. 14 – Typical dynamic power dissipation as a function of frequency.

CD4071B, CD4072B, CD4075B Types

TERMINAL ASSIGNMENTS (TOP VIEW)

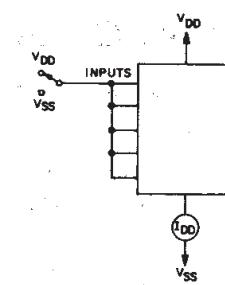
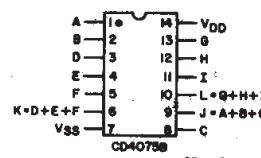
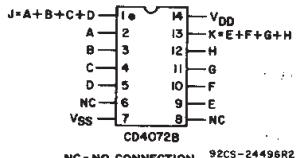
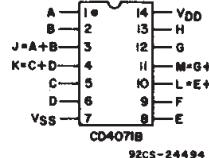


Fig. 15 — Quiescent device current test circuit.

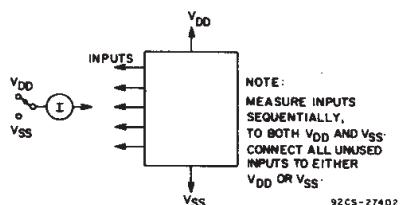


Fig. 16 — Input current test circuit.

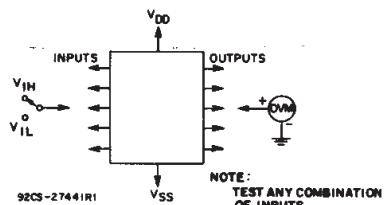
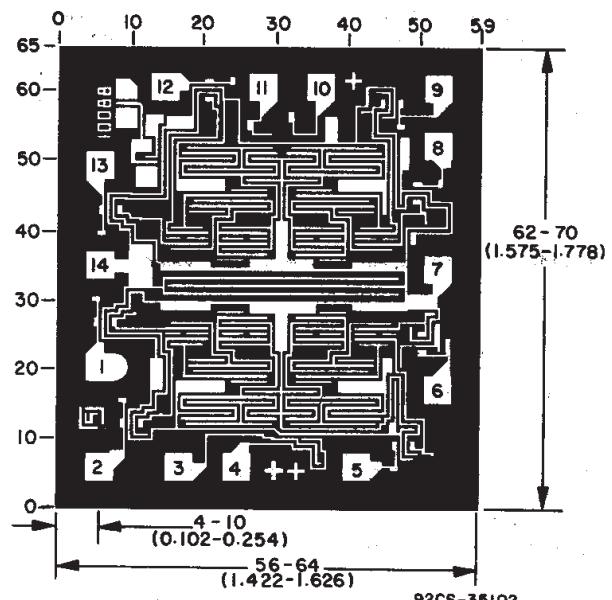
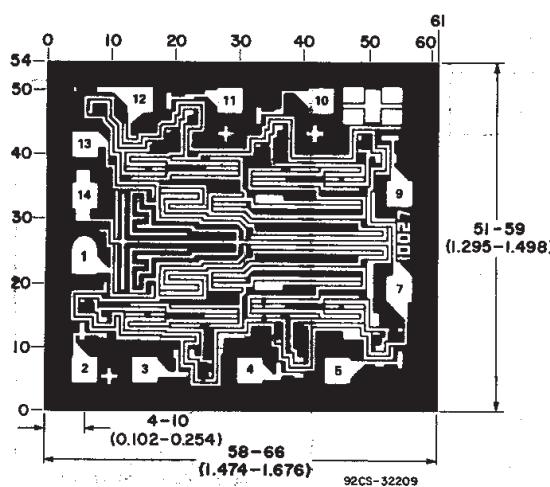


Fig. 17 — Input-voltage test circuit.

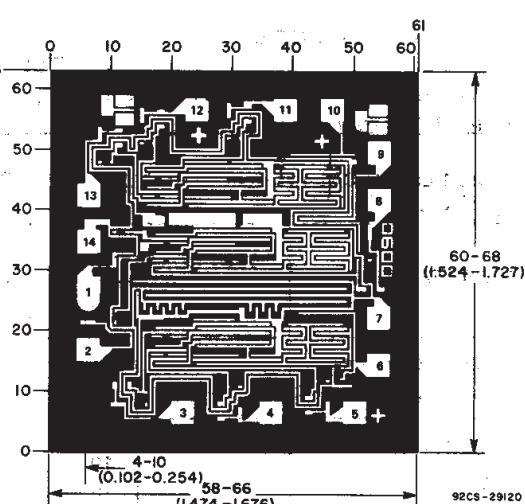
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).



Chip dimensions and pad layout for CD4071B.



Chip dimensions and pad layout for CD4072B.



Chip dimensions and pad layout for CD4075B.

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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
7706002CA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
CD4071BE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4071BEE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4071BF	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
CD4071BF3A	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
CD4071BF3AS2534	OBsolete	CDIP	J	14		TBD	Call TI	Call TI
CD4071BM	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4071BM96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4071BM96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4071BM96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4071BME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4071BMG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4071BMT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4071BMTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4071BMTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4071BNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4071BNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4071BNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4071BPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4071BPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4071BPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4071BPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4071BPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4071BPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4072BE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4072BEE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4072BF	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD4072BF3A	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
CD4072BM	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4072BM96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4072BM96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4072BM96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4072BME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4072BMG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4072BMT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4072BMTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4072BMTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4072BNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4072BNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4072BNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4072BPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4072BPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4072BPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4072BPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4072BPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4072BPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4075BE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4075BEE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4075BF	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
CD4075BF3A	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
CD4075BM	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4075BM96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4075BM96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4075BM96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD4075BME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4075BMG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4075BMT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4075BMTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4075BMTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4075BNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4075BNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4075BNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4075BPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4075BPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4075BPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4075BPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4075BPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4075BPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
JM38510/17101BCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/17103BCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

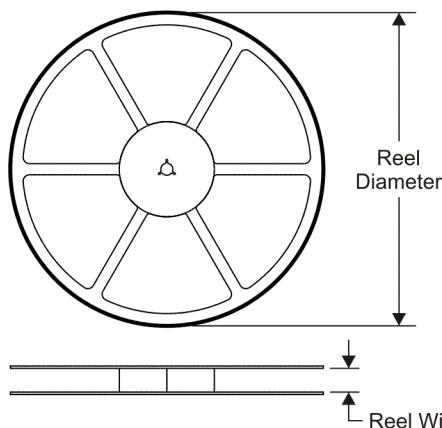
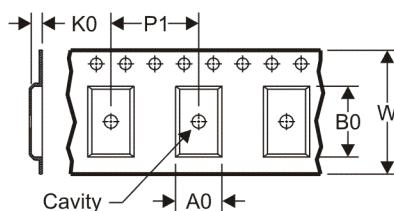
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

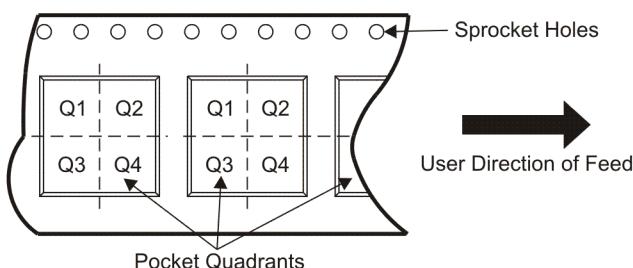
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


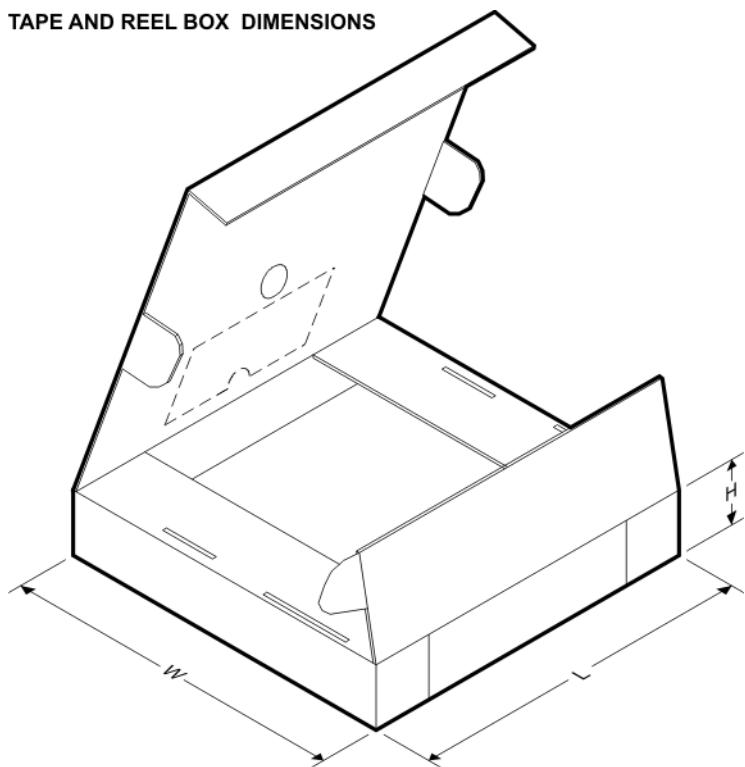
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4071BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4071BNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4071BPWR	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
CD4072BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4072BNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4072BPWR	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
CD4075BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4075BNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4075BPWR	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

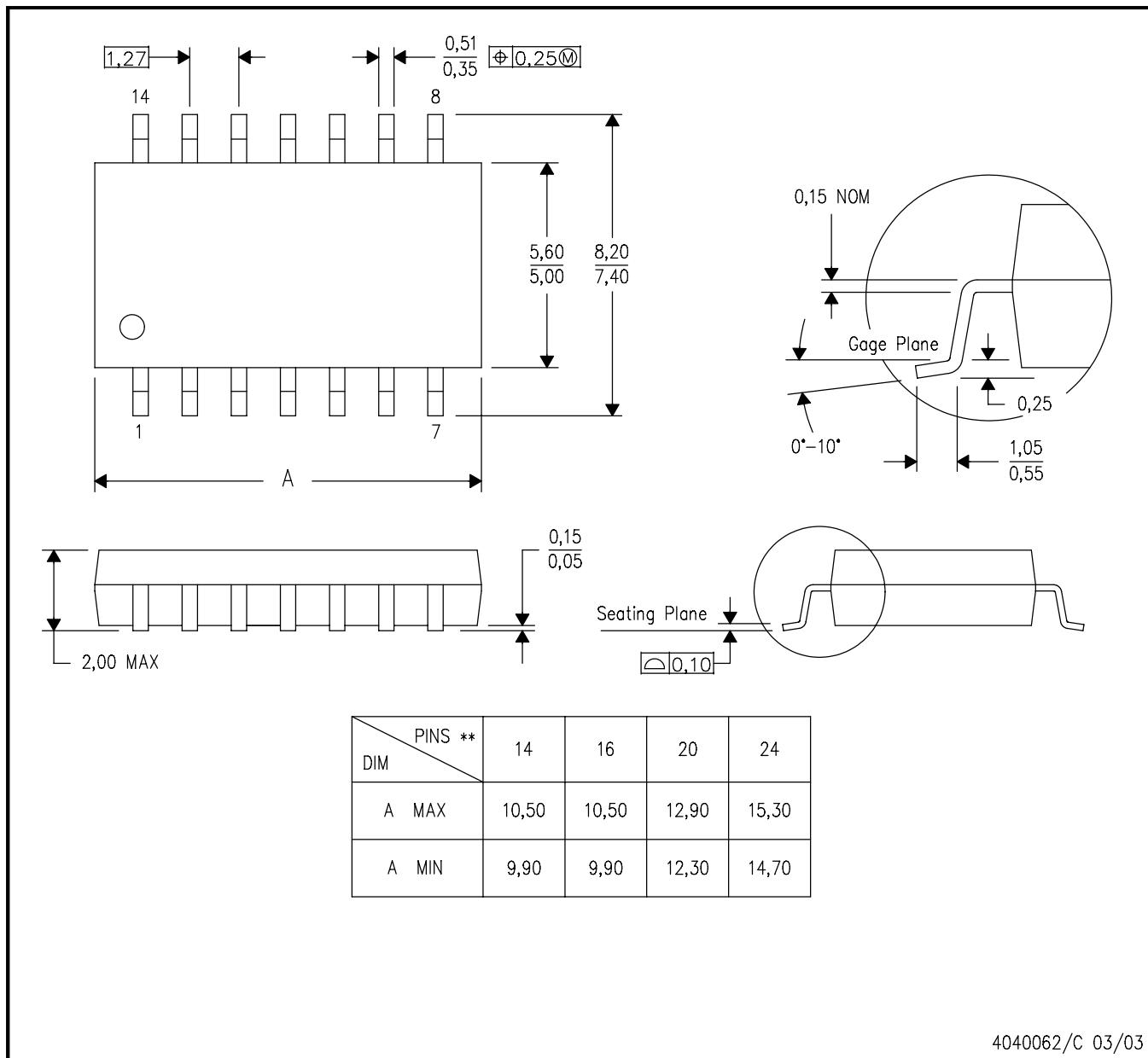
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4071BM96	SOIC	D	14	2500	346.0	346.0	33.0
CD4071BNSR	SO	NS	14	2000	346.0	346.0	33.0
CD4071BPWR	TSSOP	PW	14	2000	346.0	346.0	29.0
CD4072BM96	SOIC	D	14	2500	346.0	346.0	33.0
CD4072BNSR	SO	NS	14	2000	346.0	346.0	33.0
CD4072BPWR	TSSOP	PW	14	2000	346.0	346.0	29.0
CD4075BM96	SOIC	D	14	2500	346.0	346.0	33.0
CD4075BNSR	SO	NS	14	2000	346.0	346.0	33.0
CD4075BPWR	TSSOP	PW	14	2000	346.0	346.0	29.0

MECHANICAL DATA

NS (R-PDSO-G)**

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE

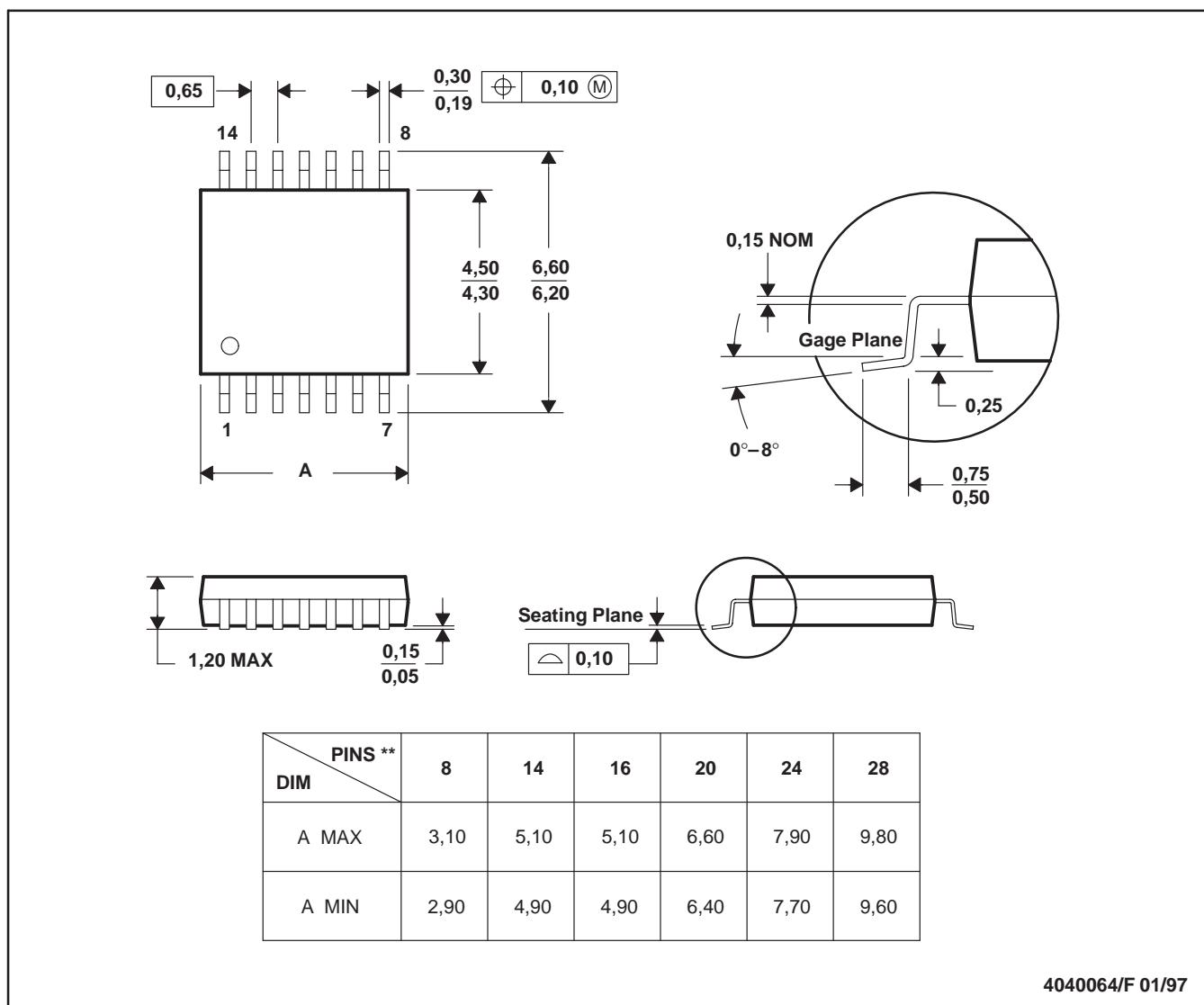


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

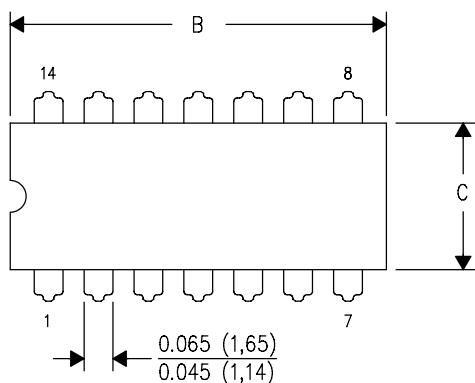


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - Falls within JEDEC MO-153

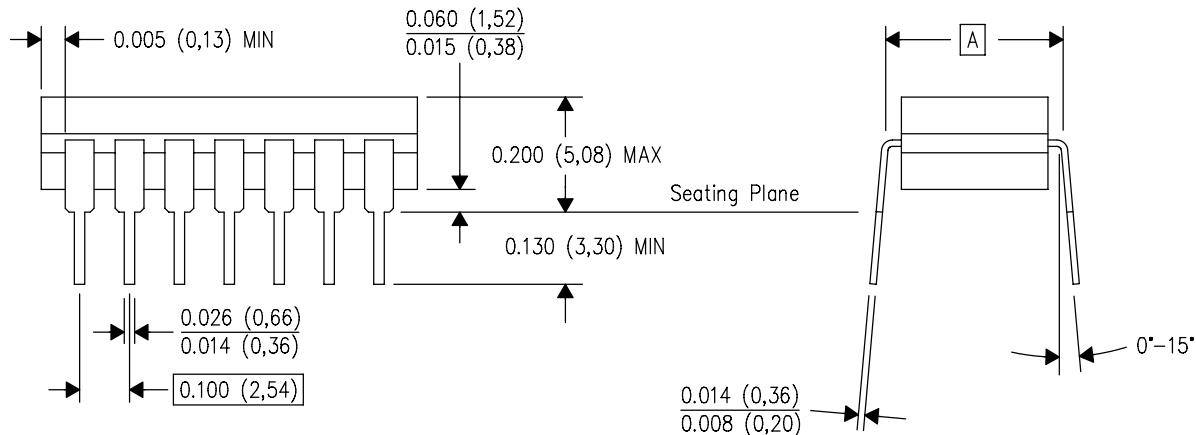
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

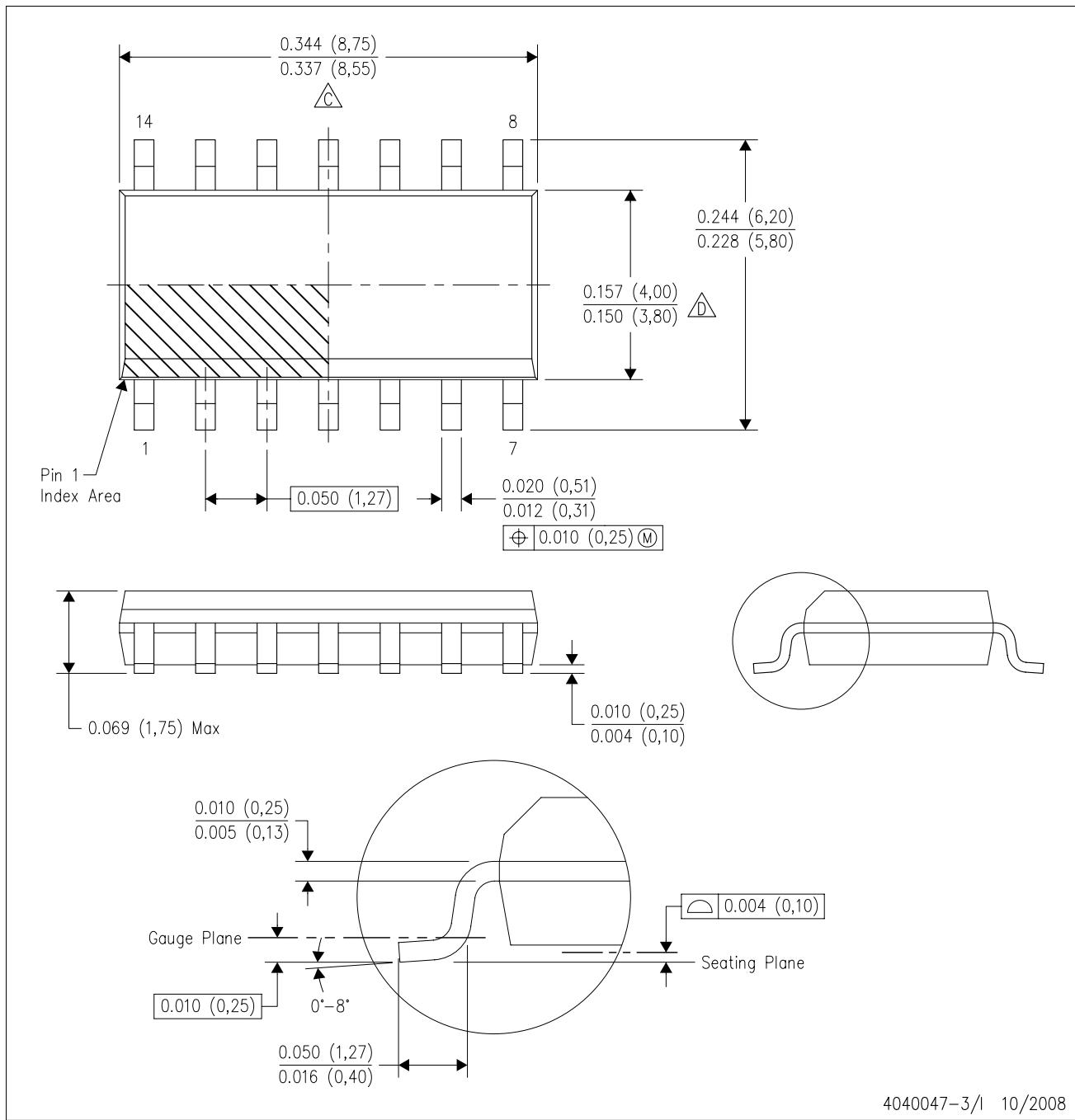


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.

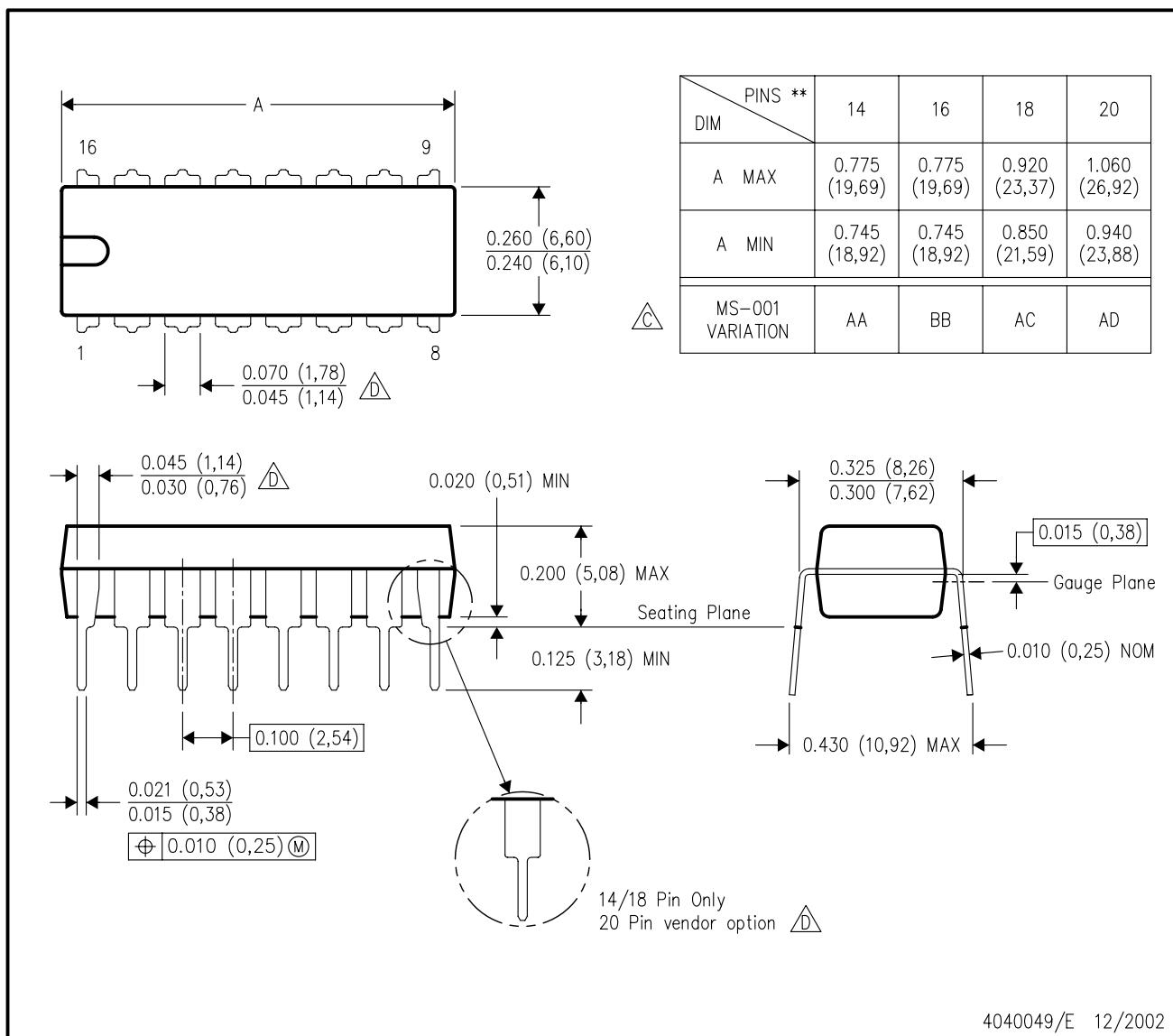
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.

E. Reference JEDEC MS-012 variation AB.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

D. The 20 pin end lead shoulder width is a vendor option, either half or full width.